EG&G RETICON

P Series Tapped 1024- and 2048-Element High Speed, Photodiode Linear Array

General Description

The P Series linear image sensors offer a high performance solution to the increasing demands of high speed imaging applications. This product family provides unparalleled performance in terms of resolution, speed, spectral response and sensitivity. Based on EG&G Reticon's advanced Charge Coupled Device (CCD) Technology, these imagers feature data rates to 80 MHz, 5V clocking, and lag-free blue response in a convenient center split dual channel architecture. Sensors are available in array lengths of 1024- and 2048-elements, and provide linescan rates to 70 kHz.

Potential applications include high speed document reading, mail sorting, web inspection, manufacturing quality and process control, precision optical measurement and gauging, and many other industrial applications which require state-of-the-art performance.

Note: While the P Series imagers have been designed to resist electro-static discharge (ESD), they can be damaged from such discharges. ESD precautions should always be observed when handling and storing this device.

Key Features

- 14 µm square pixels
- Array lengths of 1024- and 2048-elements
- Maximum line rates to 70 kHz
- Center split dual channel readout architecture
- 20V/µJ/cm^2 peak responsivity
- 2500:1 dynamic range
- Wide spectral response (200 nm -1000 nm)
- Ultra low image lag
- Exposure control
- 100x antiblooming

Functional Description

Imaging Area

The imaging region is a linear array of pixels, spaced on a 14 µm pitch, and having a 100% active area. EG&G Reticon's advanced pixel design extends the blue sensitivity into the deep UV, yet offers extremely low image lag. The P Series imagers offer an exceptionally wide spectral range, spanning the wavelength range of 200 - 1000 nm.

Horizontal Registers

Integrated charge packets are read out in a serialized charge data stream using a buried channel CCD shift register. The BCCD shift register provides high charge transfer efficiency (typically 99.999% per shift) at shift frequencies exceeding 40 MHz. The design utilizes our 5V CCD process to enable low power, high speed operation.

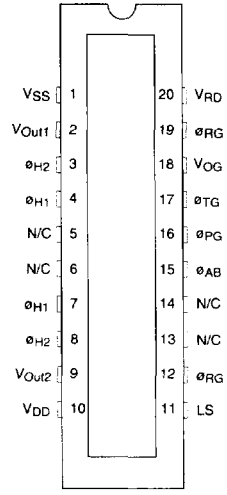

Figure 1. Pinout Configuration

The transfer gate ($ø_{TG}$) is the control interface between the pixels and the CCD shift register. During integration, this gate is held in its low state to isolate the photosites from the shift register. During line transfer, it is held in its high state to create a transfer channel between the pixels and the CCD shift register.

The line transfer sequence illustrated in Figure 4, is described as follows. After readout of a particular image line *(n)*, the horizontal CCD is empty of charge and is thus ready to accept charge packets from image line *(n+1)*. The transfer sequence begins by stopping the horizontal clocks; $ø_1$ is held in its high state and $ø_2$ in its low state. Clock phase $ø_{TG}$ is then pulsed high, to start the transfer of charge to the horizontal CCD shift register. Once the transfer gate reaches its clock-high state, the pixel storage gate ($ø_{PG}$) is clocked low, to complete the transfer process. It is recommended that the storage gate be held in the low state for at least 0.5 µs to ensure complete transfer. The pixel storage gate is then clocked high to its integrating state, and the transfer gate is clocked low to isolate the pixel from the shift register. The low state of $ø_{TG}$ marks the start of integration for line *(n+2)*. Simultaneously, readout of line *(n+1)* is started with the clocking of the horizontal CCD.

Output Amplifier

Signal charge in the CCD imager is converted to a voltage signal (video) by two output structures located at opposite ends of the CCD shift register. These structures include a charge integrator and video amplifier. The integrator is initially set to a DC reference voltage (V_{RD}), by pulsing of the reset transistor ($ø_{RS}$) to its clock-high state. When is $ø_{RS}$ pulsed low, the reset transistor is turned off, isolating the integrator from V_{RD}. Signal

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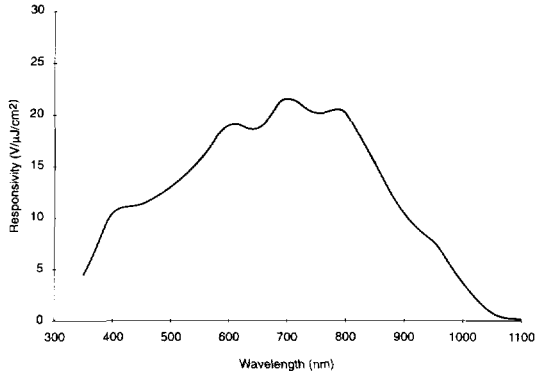


Figure 2. Typical Spectral Response Curve

charge which is clocked onto the integrator causes a voltage modulation proportional to the amplitude of the signal charge packet.

Transfer of charge to the integrator occurs with the $ø_1$ clock transition from high to low. The primary synchronization requirement is that the reset transistor reaches its clock-low state prior to the high-to-low transition of $ø_1$. An apparent clipping of the video signal will result if this condition is not satisfied. Figure 4 details the clock waveform requirements and overlap tolerances.

The video amplifier has limited ability to drive high capacitive or low impedance loads; its half power point into an external load of 10 pF is 150 MHz. It is recommended that the output video signal be buffered with a wide bandwidth emitter follower or other appropriate amplifier which will provide a large Z_{in} to the CCD. In addition, the external amplifier should be placed close to the output pins to minimize inductive and capacitive loading of the CCD amplifier.

Exposure Control and Antiblooming

An exposure control feature is provided which allows variable integration time. By clocking $ø_{AB}$ to its high state, charge is drained from the pixel storage gate to the exposure control drain, V_{AB}. During integration, $ø_{AB}$ is normally set to its low state value.

Timing Requirements

Timing details for the P Series arrays are specified in Figure 4. While the two-phase CCD architecture allows relaxed timing tolerances over those required in three- or four-phase designs, the optimum device performance is obtained when the overlap of the two-phase CCD clocks occurring between the 10-90% transition level. As the phase difference between clock signals $ø_1$ and $ø_2$ departs from 180°, a performance loss of full-well or transfer efficiency will begin to occur.

In high speed applications, it may be advantageous to utilize fast clock edges to allow maximum settling time of the output video. However, it is generally advisable to use the slowest rise and fall times which may be feasible in the particular situation. This is because fast clock edges tend to degrade the video waveform quality due to increased clock coupling and possible charge injection. If this occurs, shaping of the clock edges to obtain the optimum balance between speed and video quality is advised.

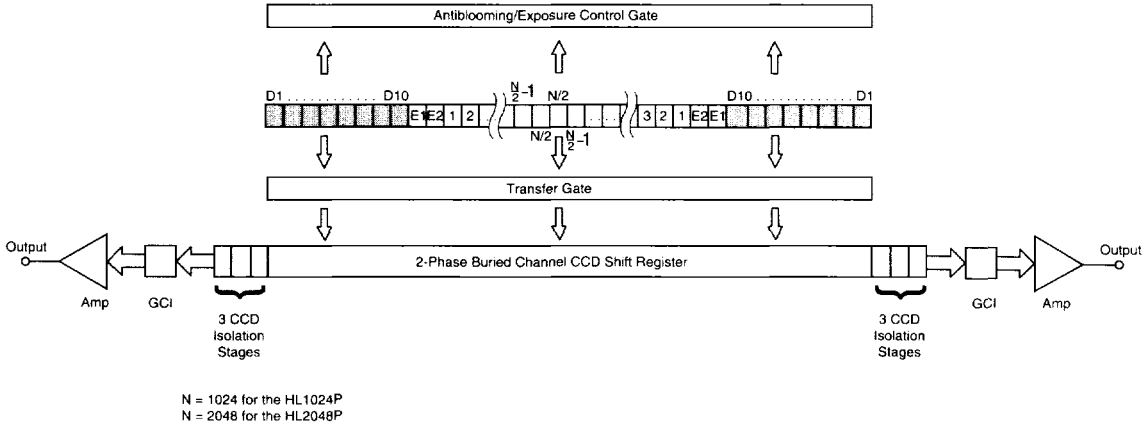
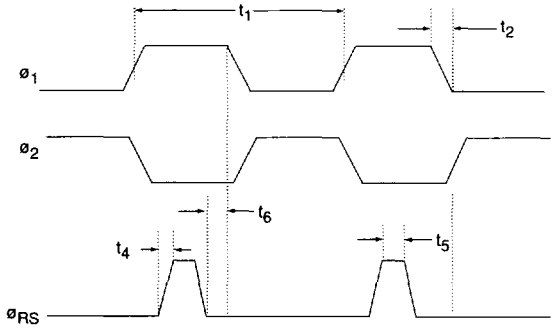


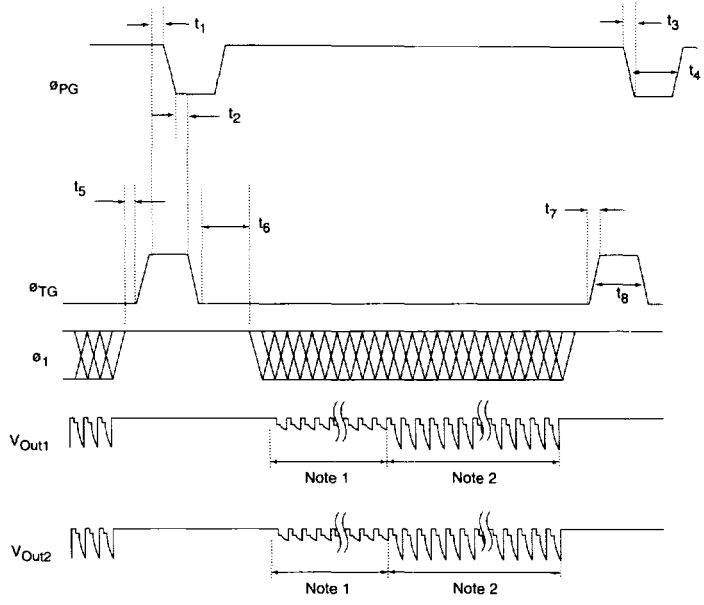
Figure 3. Functional Diagram



Item	Sym	Min	Typ	Max
$ø_1$, $ø_2$ clock period	t_1	25 ns	–	–
$ø_1$, $ø_2$ rise/fall time	t_2	–	5 ns	–
$ø_{RS}$ rise/fall time	t_4	–	5 ns	–
$ø_{RS}$ clock - high duration	t_5	5 ns	–	–
Delay of $ø_1$ high - low transition from $ø_{RG}$ low	t_6	0 ns	–	–

Note:
1. The cross over point for $ø_1$ and $ø_2$ clock transitions should occur within the 10 - 90% level of the clock amplitude.
2. Recommend t_5 and t_6 are kept as short as possible.

Figure 4a. Timing Requirements of the Readout CCD Shift Register



Item	Sym	Min	Typ	Max
$ø_{TG}$ high to start of $ø_{PG}$ low	t_1	0 ns	10 ns	–
Start of $ø_{TG}$ low transition from $ø_{PG}$ low	t_2	500 ns	500 ns	–
$ø_{PG}$ rise/fall time	t_3	10 ns	20 ns	–
$ø_{PG}$ pulse width	t_4	500 ns	1000 ns	–
Last $ø_1$ high to start of $ø_{TG}$ low to high transition	t_5	0 ns	10 ns	–
$ø_{TG}$ low to start of $ø_1$ clock	t_6	0 ns	10 ns	–
$ø_{TG}$ rise/fall time	t_7	10 ns	20 ns	–
$ø_{TG}$ pulse width	t_8	100 ns	500 ns	–

Note:
1. 3 isolation pixels, 10 dark pixels
2. 2 extra pixels, N/2 active

Figure 4b. Timing Detail for Line Transfer

Table 1. Pinout Description and Capacitance Values of Clocked Phases

Pin	Sym	Function	Capacitance (pF) 2048	1024
1	V_{SS}	Amplifier return	50	30
2	V_{Out1}	Signal output	75	45
3	$ø_{H2}$	CCD horizontal phase 2	75	40
4	$ø_{H1}$ [1]	CCD horizontal phase 1	200	120
5	N/C	No connection		
6	N/C	No connection		
7	$ø_{H1}$ [1]	CCD horizontal phase 1	200	120
8	$ø_{H2}$	CCD horizontal phase 2	75	40
9	V_{Out2}	Signal output		
10	V_{DD}	Amplifier drain supply		
11	LS	Light shield/die attach		
12	$ø_{RG}$	Reset gate	20	20
13	N/C	No connection		
14	N/C	No connection		
15	$ø_{AB}$	Antiblooming gate		
16	$ø_{PG}$	Pixel storage gate	150	80
17	$ø_{TG}$	Transfer gate	150	80
18	V_{OG}	Output gate		
19	$ø_{RG}$	Reset gate	20	20
20	V_{RD}	Reset drain		

Note:
[1] $ø_{H1}$ signals electrically connected on-chip

Table 2. Specifications

Pixel count	1024 elements (HL1024P) 2048 elements (HL2048P)
Pixel pitch	14 µm
Exposure control	yes
Horizontal clocking	2ø (5V clock amplitude)
Number of outputs	2
Dynamic range [1]	2500:1
Readout noise (rms)	
amplifier	25 electrons
reset transistor	55 electrons
total noise without CDS	60 electrons
Saturation exposure [2]	0.03 µJ/cm^2
rms noise equivalent exposure [2]	12 pJ/cm^2
Amplifier sensitivity	4 µV/electrons
Saturation output voltage	600 mV
Saturation charge capacity	150,000 electrons
Charge transfer efficiency	0.99995
Peak responsivity [2]	20V/µJ/cm^2
PRNU	
match across array	±10%
Gain and offset uniformity (tap-to-tap)	±10%
Spectral response range	200 nm - 1000 nm
Data rate (per output)	40 MHz

Notes:
[1] Defined as V_{sat}:rms noise. Noise includes amplifier thermal noise contribution and reset noise.
[2] For illumination at 700 nm

Table 3. Recommended Operating Conditions

Sym	Function		Low	Typ	High
$ø_1$	Phase 1 [1]	Clock High	4.5	5.0	8.0
		Clock Low	-0.3	0.0	0.5
$ø_2$	Phase 2 [1]	Clock High	4.5	5.0	8.0
		Clock Low	-0.3	0.0	0.5
$ø_{RG}$	Reset gate [2]	Clock High	V_{RD} - 2.0	V_{RD} - 1.5	V_{RD}
		Clock Low	-0.3	5.0	5.0
$ø_{AB}$	AB/exposure control gate	Clock High	7.7	8.0	10.0
		Clock Low	-0.3	0.0	1.0
$ø_{TG}$	Vertical transfer gate	Clock High	7.7	8.0	10.0
		Clock Low	-0.3	0.0	0.5
$ø_{PG}$	Pixel storage gate	Clock High	7.5	8.0	8.5
		Clock Low	-0.3	0.0	0.5
V_{OG}	Output gate bias		2.5	3	3.5
V_{DD}	Amplifier supply		10.0	12.0	14.0
V_{SS}	Ground		0	0	0
V_{RD}	Reset reference level		(V_{DD} - 1.5)	(V_{DD} - 1.5)	(V_{DD} - 1.0)
LS	Light shield		0	0	0

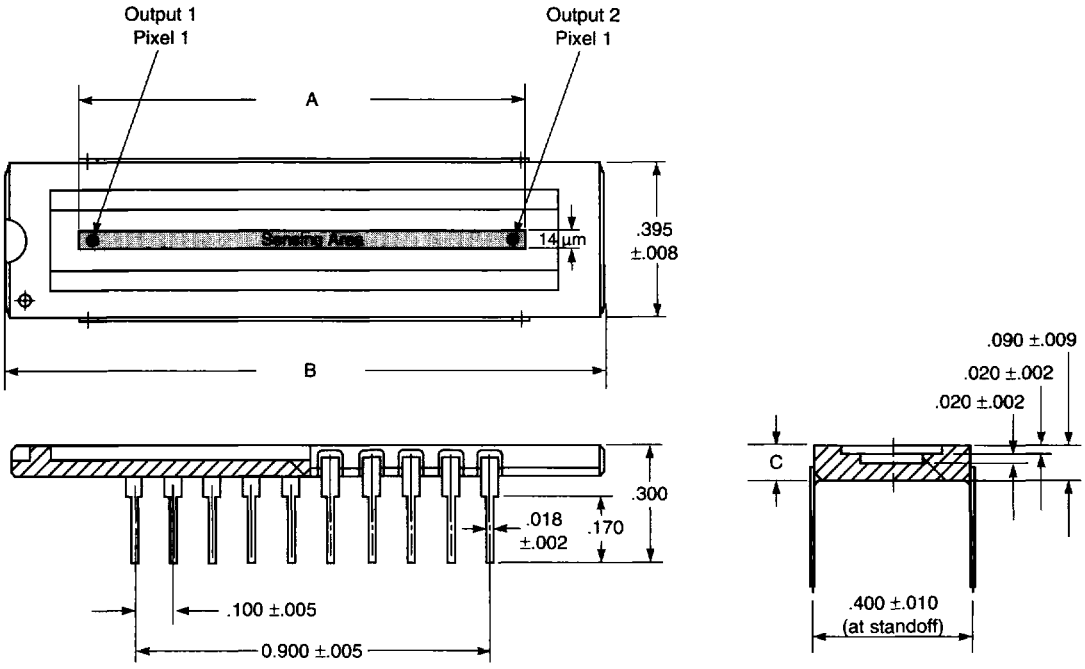
Note:
1 Clock amplitude should be 5.0V
2 Clock low can be higher than +5V, but must be individually tuned to prevent output signal clipping

Table 4. Absolute Maximum Ratings

Above which Useful Life May Be Impaired

	Min	Max	Units
Temperature			
Storage	-25	+85	°C
Operating	-25	+55	°C
Voltage (with respect to GND)			
Pins 3, 4, 7, 8, 12, 15 - 19	-0.3	+18	V
Pins 2, 9, 10, 20	-0.3	+18	V
Pins 1, 11	-0.3	+ 0	V

Precautionary Note:
The CCD output pins must never be shorted to either V_{SS} or V_{DD} while power is applied to the device. Catastophic device failure will result!



Device	A inches	A mm	B inches	C inches
HL1024PAQ-011	.566	14.392	1.500 ±.015	.090 ±.009
HL2048PAQ-011	1.131	28.728	1.500 ±.015	.090 ±.009

Figure 5. Package Dimensions

Ordering Information

Part Number
HL1024PAQ-011
HL2048PAQ-011