Standard Products

UT54LVDS032LV Low Voltage Quad Receiver

Data Sheet

December, 2003

FEATURES

- >400.0 Mbps (200 MHz) switching rates
- ±340mV differential signaling
- 3.3 V power supply
- TTL compatible outputs
- Cold spare all pins
- Ultra low power CMOS technology
- 4.0ns maximum propagation delay
- 0.35ns maximum differential skew
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si) and 1Mrad(Si)
  - Latchup immune (LET > 100 MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack (dual in-line)
- Standard Microcircuit Drawing 5962-98652
  - QML Q and V compliant part

INTRODUCTION

The UT54LVDS032LV Quad Receiver is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400.0 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The UT54LVDS032LV accepts low voltage (340mV) differential input signals and translates them to 3V CMOS output levels. The receiver supports a three-state function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100 Ω) input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

The UT54LVDS032LV and companion quad line driver UT54LVDS031LV provides new alternatives to high power pseudo-ECL devices for high speed point-to-point interface applications.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

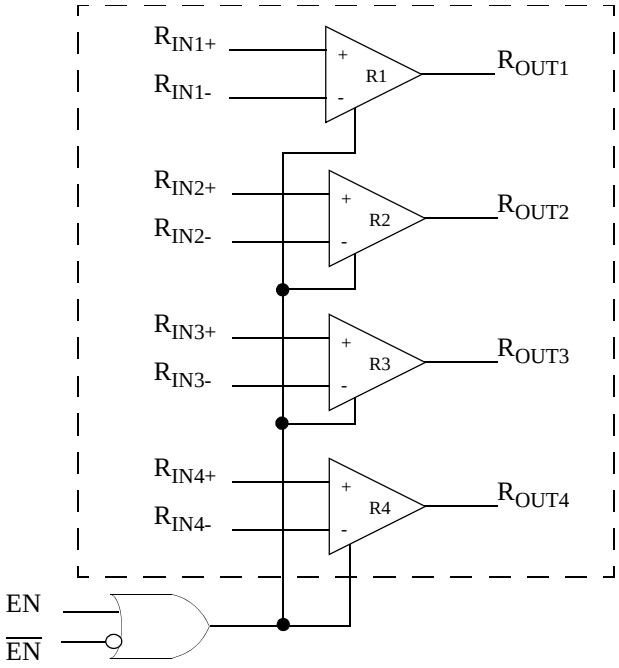


Figure 1. UT54LVDS032LV Quad Receiver Block Diagram

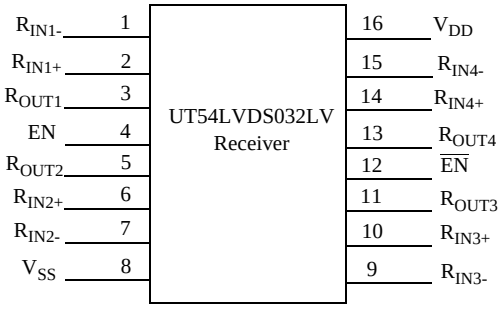


Figure 2. UT54LVDS032LV Pinout

TRUTH TABLE

Enables		Input	Output
EN	$\overline{EN}$	R_{IN+} - R_{IN-}	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

PIN DESCRIPTION

Pin No.	Name	Description
2, 6, 10, 14	R_{IN+}	Non-inverting receiver input pin
1, 7, 9, 15	R_{IN-}	Inverting receiver input pin
3, 5, 11, 13	R_{OUT}	Receiver output pin
4	EN	Active high enable pin, OR-ed with $\overline{EN}$
12	$\overline{EN}$	Active low enable pin, OR-ed with EN
16	V_{DD}	Power supply pin, +3.3 $\pm$ 0.3V
8	V_{SS}	Ground pin

APPLICATIONS INFORMATION

The UT54LVDS032LV receiver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Figure 3. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into voltages that are detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities, as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

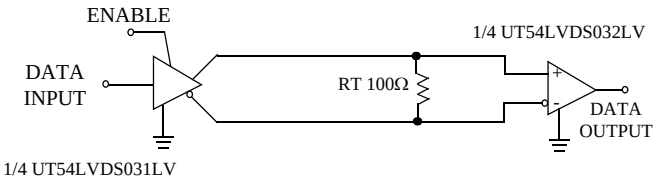


Figure 3. Point-to-Point Application

The UT54LVDS032LV differential line receiver is capable of detecting signals as low as 100mV, over a $\pm$ 1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift $\pm$1V around this center point. The $\pm$1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground).

Receiver Fail-Safe

The UT54LVDS032LV receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to TTL logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins**. The UT54LVDS032LV is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.
2. **Terminated Input**. If the driver is disconnected (cable unplugged), or if the driver is in a three-state or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.
3. **Shorted Inputs**. If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (V_{SS} to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin during operation	-0.3 to (V_{DD} + 0.3V)
	Voltage on any pin during cold spare	-.3 to 4.0V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.25 W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and life test.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage, receiver inputs DC input voltage, logic inputs	2.4V 0 to V_{DD} for EN, $\overline{EN}$

DC ELECTRICAL CHARACTERISTICS [1]

(V_{DD} = 3.3V ± 0.3V; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage	(TTL)	2.0		V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL}	Low-level output voltage	I_{OL} = 2mA, V_{DD} = 3.0V		0.25	V
V_{OH}	High-level output voltage	I_{OH} = -0.4mA, V_{DD} = 3.0V	2.7		V
I_{IN}	Logic input leakage current	Enables = EN/$\overline{EN}$ = 0 and 3.6V, V_{DD} = 3.6	-10	+10	µA
I_I	Receiver input Current	V_{IN} = 2.4V	-15	+15	µA
I_{CS}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
V_{TH}[3]	Differential Input High Threshold	V_{CM} = +1.2V		+100	mV
V_{TL}[3]	Differential Input Low Threshold	V_{CM} = +1.2V	-100		mV
I_{OZ}[3]	Output Three-State Current	Disabled, V_{OUT} = 0 V or V_{DD}	-10	+10	µA
V_{CL}	Input clamp voltage	I_{CL} = +18mA	-1.5		V
I_{OS}[2, 3]	Output Short Circuit Current	Enabled, V_{OUT} = 0 V[2]	-15	-130	mA
I_{CC}[3]	Supply current, receivers enabled	EN, $\overline{EN}$ = V_{DD} or V_{SS} Inputs Open		15	mA
I_{CCZ}[3]	Supply current, receivers disabled	EN = V_{SS}, $\overline{EN}$ = V_{DD} Inputs Open		4	mA

Notes:

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.

AC SWITCHING CHARACTERISTICS[1, 2, 3]
(V_{DD} = +3.3V ± 0.3V, T_A = -55 °C to +125 °C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{PHLD}[6]	Differential Propagation Delay High to Low CL = 10pf (figures 4 and 5)	1.0	4.0	ns
t_{PLHD}[6]	Differential Propagation Delay Low to High CL = 10pf (figures 4 and 5)	1.0	4.0	ns
t_{SKD}[4]	Differential Skew (t_{PHLD} - t_{PLHD}) (figures 4 and 5)	0	0.35	ns
t_{SK1}[4]	Channel-to-Channel Skew[1] (figures 4 and 5)	0	0.5	ns
t_{SK2}[4]	Chip-to-Chip Skew[5] (figures 4 and 5)		3.0	ns
t_{TLH}[4]	Rise Time (figures 4 and 5)		1.2	ns
t_{THL}[4]	Fall Time (figures 4 and 5)		1.2	ns
t_{PHZ}[4]	Disable Time High to Z (figures 6 and 7)		12	ns
t_{PLZ}[4]	Disable Time Low to Z (figures 6 and 7)		12	ns
t_{PZH}[4]	Enable Time Z to High (figures 6 and 7)		12	ns
t_{PZL}[4]	Enable Time Z to Low (figures 6 and 7)		12	ns

Notes:
1. Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_0 = 50Ω, t_r and t_f (0% - 100%) ≤ 1ns for R_{IN} and t_r and t_f ≤ 1ns for EN or $\overline{EN}$.
3. C_L includes probe and jig capacitance.
4. Guaranteed by characterization.
5. Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
6. May be tested at higher load capacitance and the limit interpolated from characterization data to guarantee this parameter.

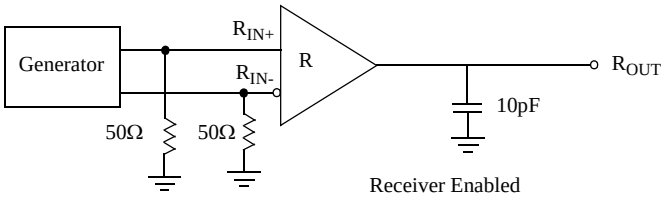


Figure 4. Receiver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit

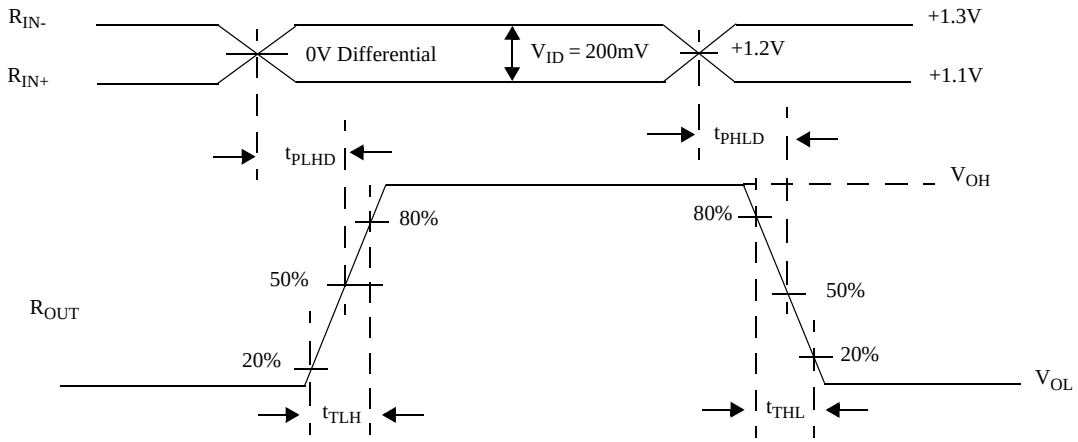


Figure 5. Receiver Propagation Delay and Transition Time Waveforms

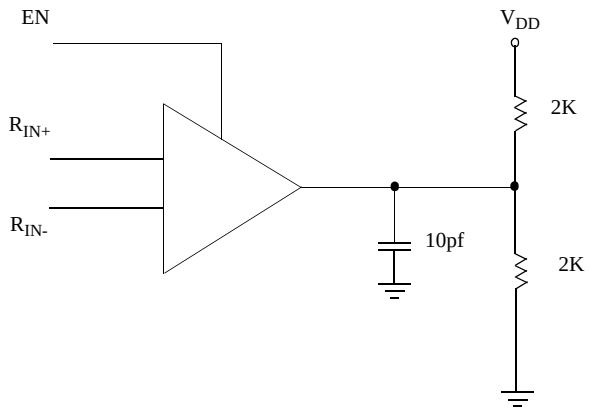


Figure 6. Receiver Three-State Delay Test Circuit or Equivalent Circuit

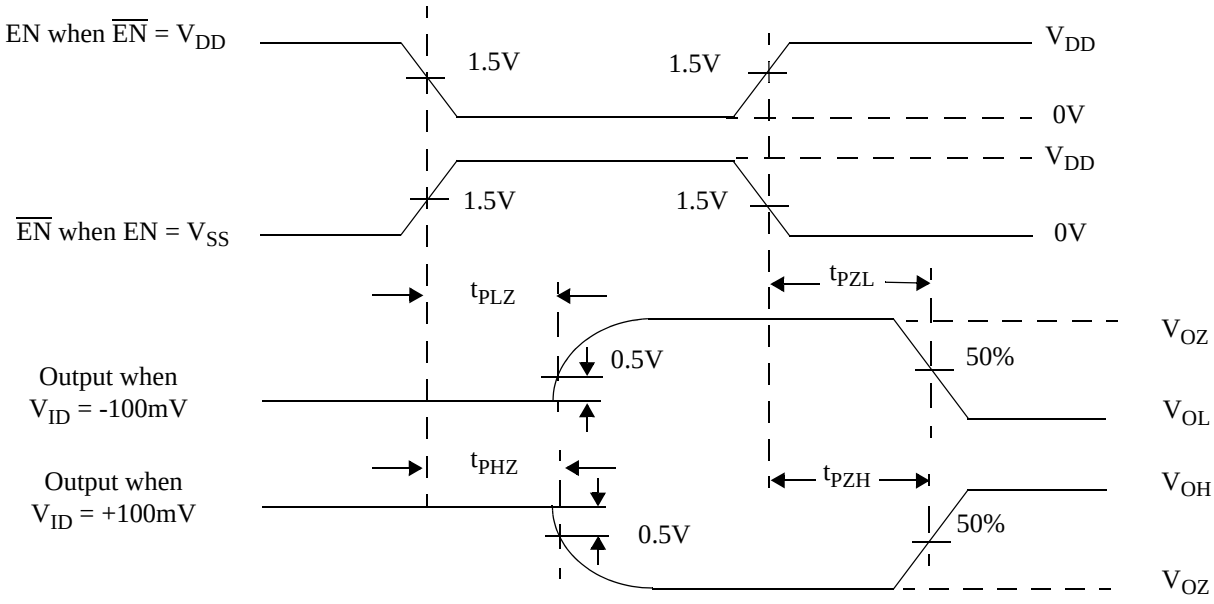
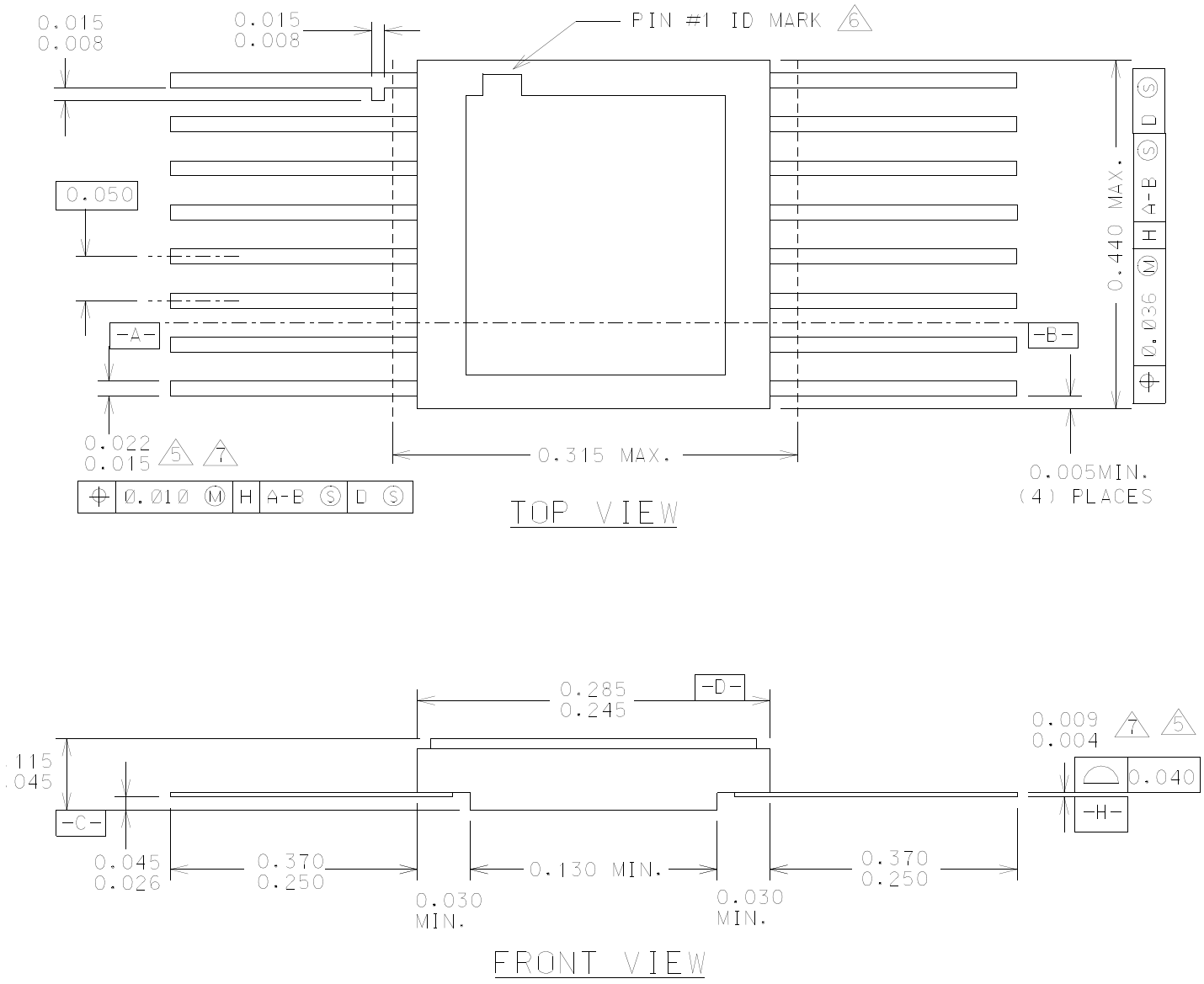


Figure 7. Receiver Three-State Delay Waveform

PACKAGING



Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Package dimensions and symbols are similar to MIL-STD-1835 variation F-5A.

5 Lead position and coplanarity are not measured.

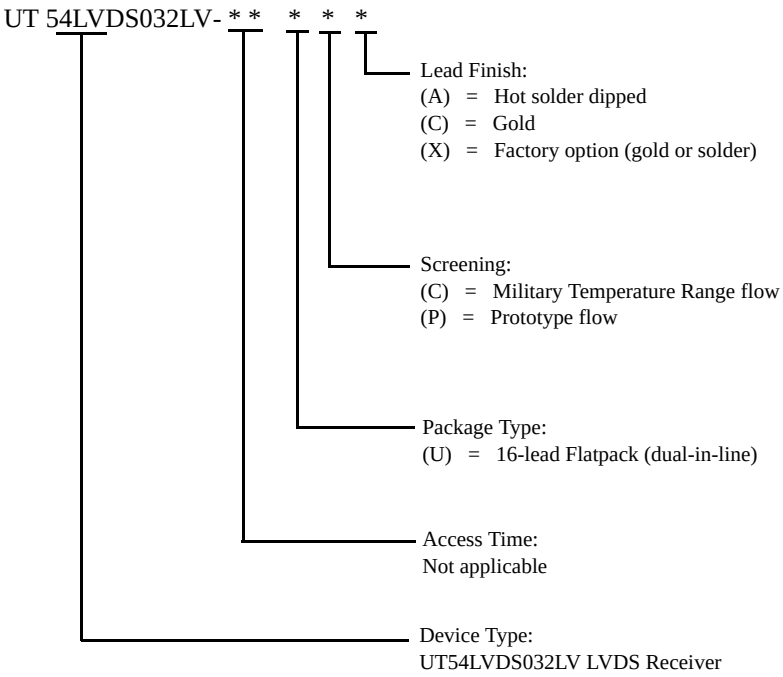
6 ID mark symbol is vendor option.

7 With solder, increase maximum by 0.003.

Figure 8. 16-pin Ceramic Flatpack

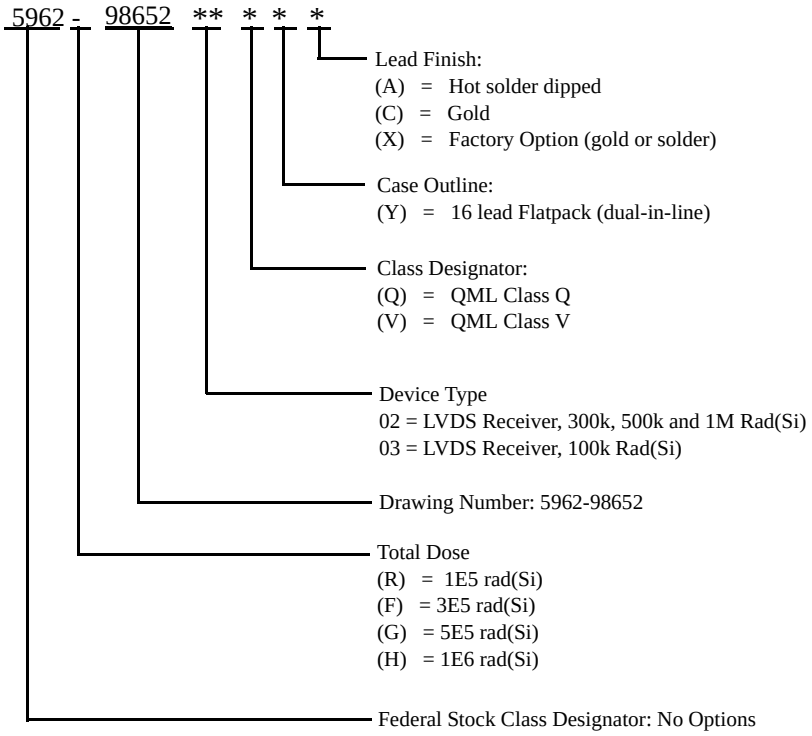
ORDERING INFORMATION

UT54LVDS032LV QUAD RECEIVER:



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

UT54LVDS032LV QUAD RECEIVER: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.