NEC

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD72870B

IEEE1394 1-CHIP OHCI HOST CONTROLLER

The μPD72870B is the LSI which integrated OHCI-Link and PHY function into a single chip.

The μPD72870B complies with the P1394a draft 2.0 specifications and the OpenHCI IEEE1394 1.0, and works up to 400 Mbps.

It makes design so compact for PC and PC card application.

FEATURES

- Compliant with Link Layer Services as defined in 1394 Open Host Controller Interface specification release 1.0
- Compliant with Physical Layer Services as defined in P1394a draft 2.0 (Data Rate 100/200/400 Mbps)
- Numbers of supported port (1, 2, 3 ports) are selectable
- Compliant with protocol enhancement as defined in P1394a draft 2.0
- Modular 32-bit host interface compliant to PCI Specification release 2.1
- Support PCI-Bus Power Management Interface Specification release 1.1
- Modular 32-bit host interface compliant to Card Bus Specification
- Cycle Master and Isochronous Resource Manager capable
- Built-in FIFOs for isochronous transmit (1024 bytes), asynchronous transmit (1024 bytes), and receive (2048 bytes)
- 32-bit CRC generation and checking for receive/transmit packets
- 4 isochronous transmit DMAs and 4 isochronous receive DMAs supported
- 32-bit DMA channels for physical memory read/write
- Clock generation by 24.576 MHz X'tal
- Internal control and operational registers direct-mapped to PCI configuration space
- 2-wire Serial EEPROM™ interface supported
- Separate power supply Link and PHY
- Programmable latency timer from serial EEPROM in Cardbus mode (CARD_ON = 1)

ORDERING INFORMATION

Part number	Package
μPD72870BGM-8ED	160-pin plastic LQFP (Fine pitch) (24 x 24)

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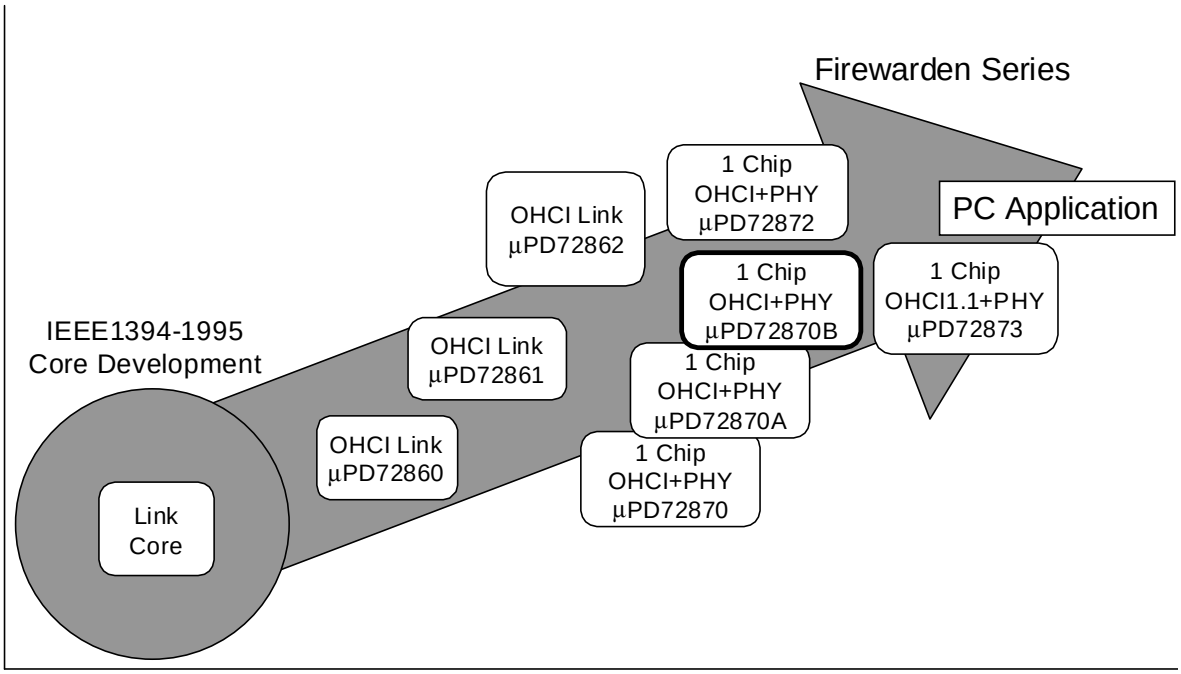
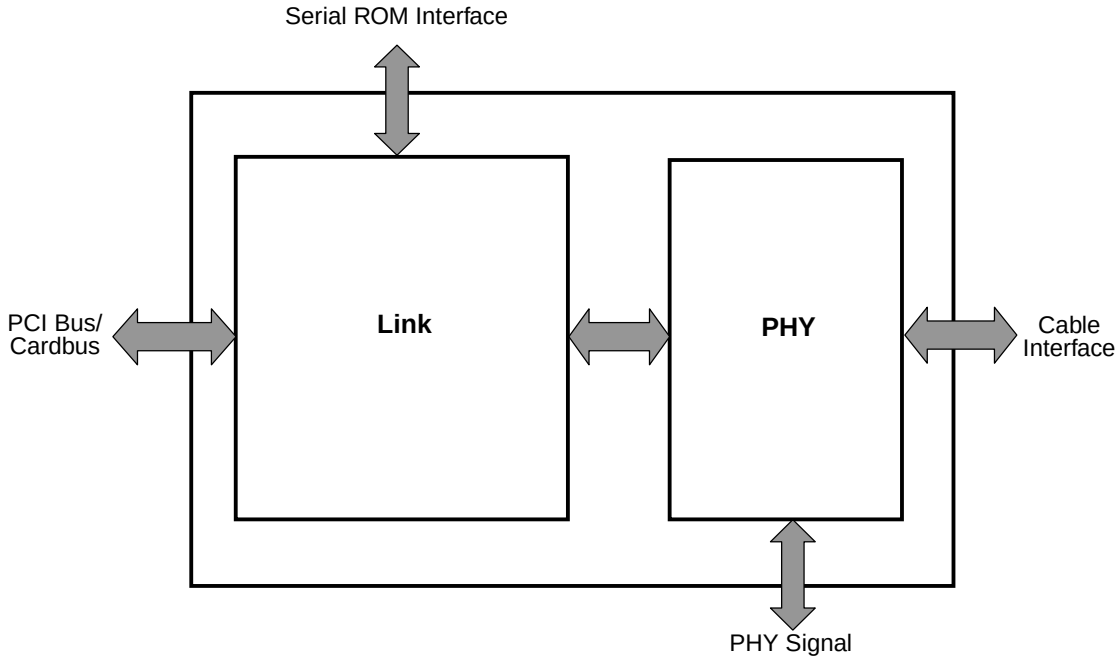
Firewarden™ PRODUCT EVOLUTION

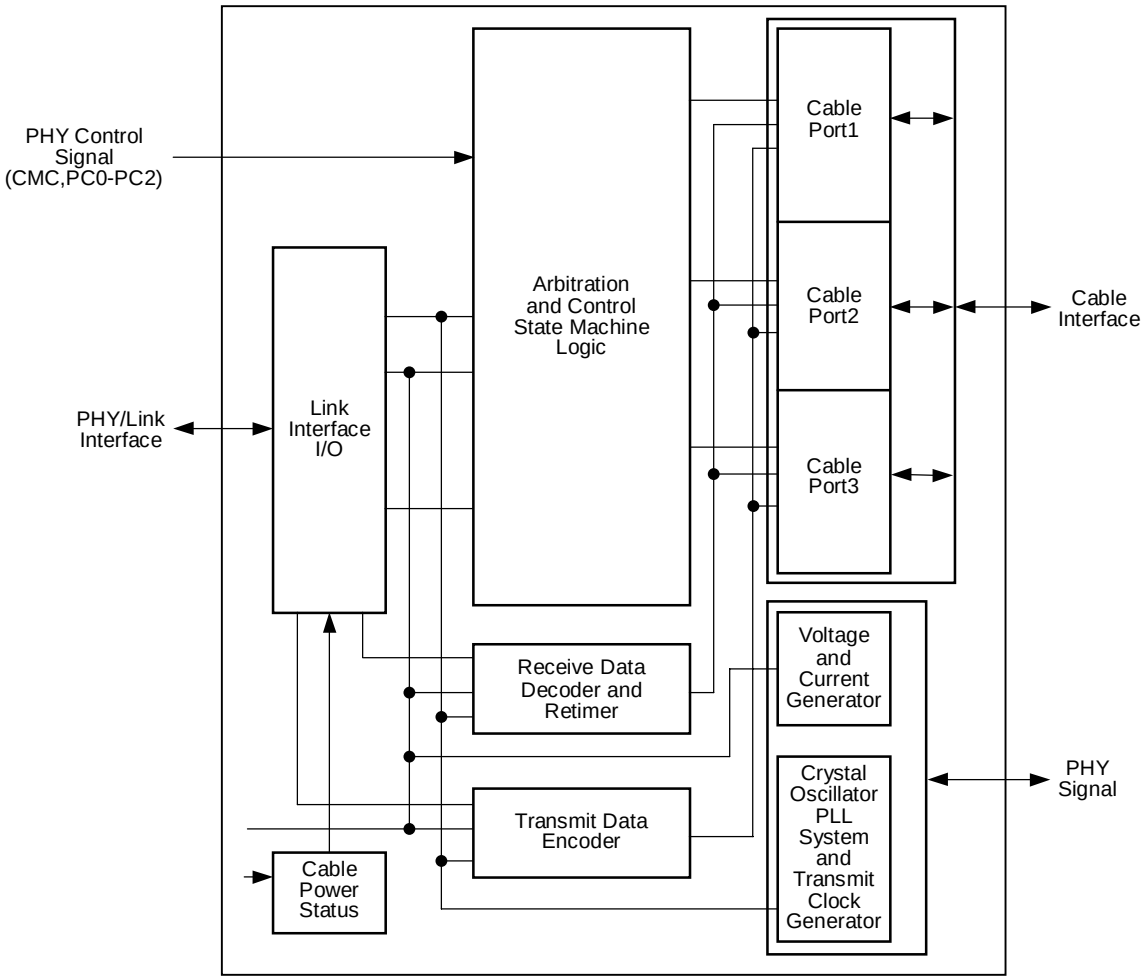


BLOCK DIAGRAMS

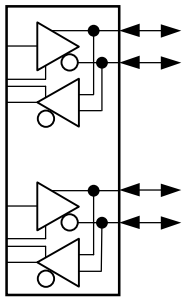
Top Block Diagram



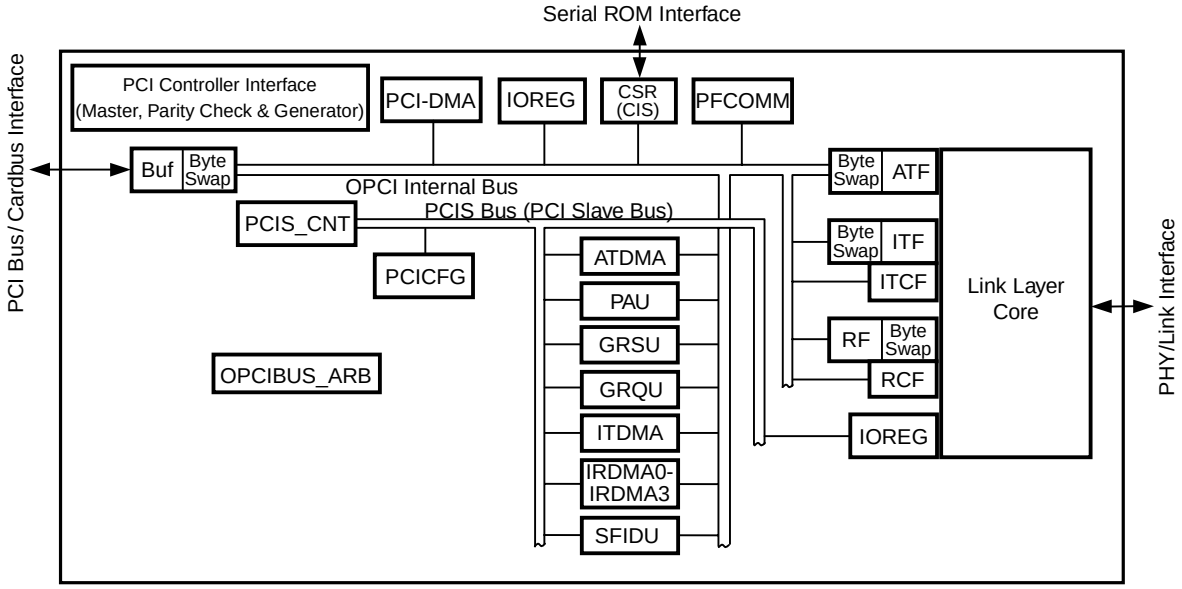
PHY Block Diagram



Remark Cable Port:



Link Block Diagram



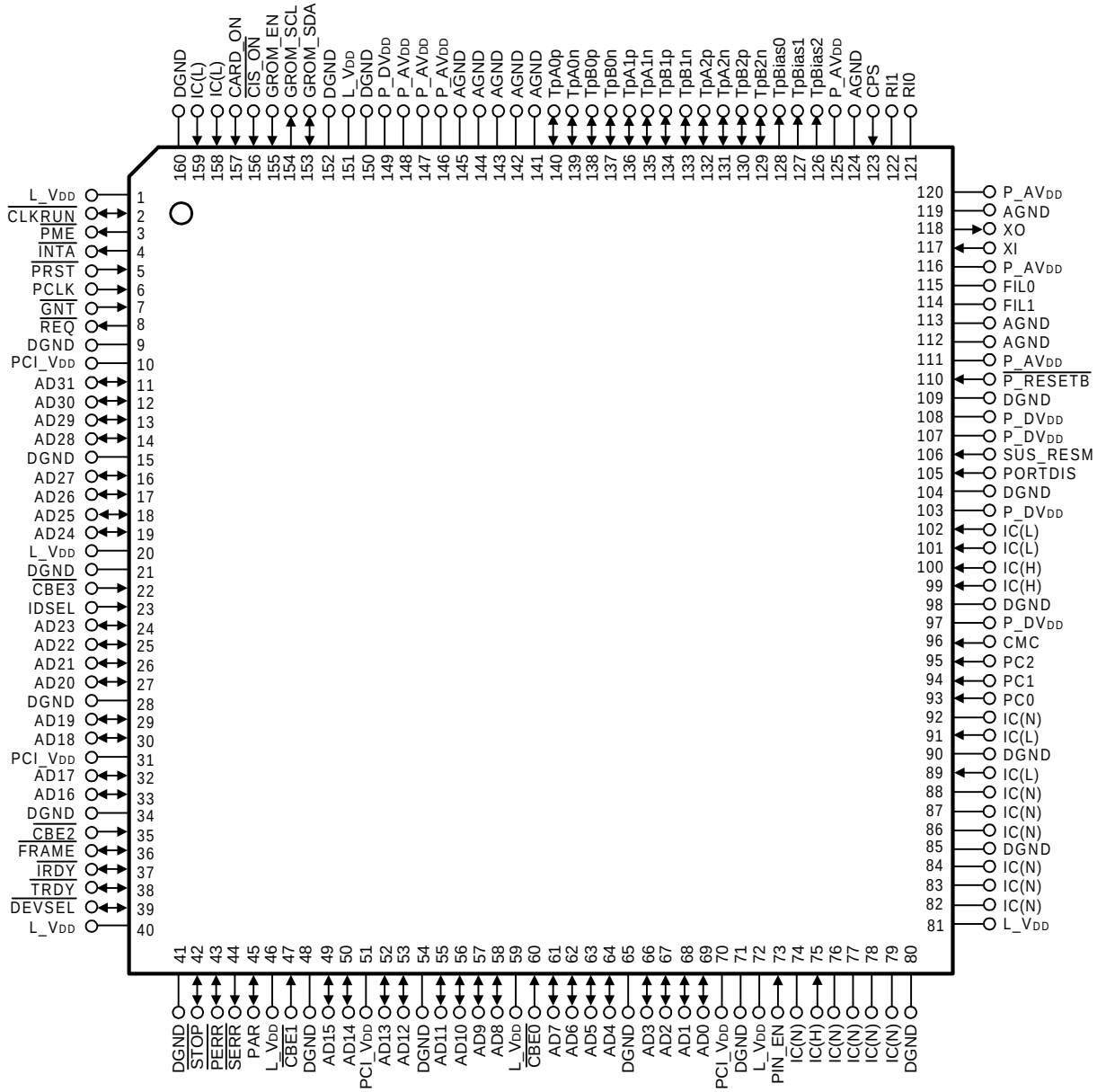
ATDMA	: Asynchronous Transmit DMA
ATF	: Asynchronous Transmit FIFO
CIS	: CIS Register
CSR	: Control and Status Registers
IOREG	: IO Registers
IRDMA	: Isochronous Receive DMA
ITCF	: Isochronous Transmit Control FIFO
ITDMA	: Isochronous Transmit DMA
ITF	: Isochronous Transmit FIFO
OPCIBUS_ARB	: OPCI Internal Bus Arbitration
PAU	: Physical Response and Request Unit
PCICFG	: PCI Configuration Registers
PCIS_CNT	: PHY Control Isochronous Control
PFCOMM	: Pre Fetch Command FIFO
RCF	: Receive Control FIFO
RF	: Receive FIFO
SFIDU	: Self-ID DMA

PIN CONFIGURATION

- **160-pin plastic LQFP (Fine pitch) (24 x 24)**

μPD72870BGM-8ED

Top View



PIN NAME

AD0-AD31 : PCI Multiplexed Address and Data
AGND : Analog GND
CARD_ON : PCI/Card Select
$\overline{CBE0}$-$\overline{CBE3}$: Command/Byte Enables
$\overline{CIS\_ON}$: CIS Register ON
$\overline{CLKRUN}$: PCICLK Running
CMC : Configuration Manager Capable
CPS : Cable Power Status Input
$\overline{DEVSEL}$: Device Select
DGND : Digital GND
FIL0 : APLL Filter GND
FIL1 : APLL Filter Terminal
$\overline{FRAME}$: Cycle Frame
$\overline{GNT}$: Bus_master Grant
GROM_EN : Serial EEPROM Enable
GROM_SCL : Serial EEPROM Clock Output
GROM_SDA : Serial EEPROM Data Input / Output
IC(H) : Internally Connected (High Clamped)
IC(L) : Internally Connected (Low Clamped)
IC(N) : Internally Connected (Open)
IDSEL : ID Select
$\overline{INTA}$: Interrupt
$\overline{IRDY}$: Initiator Ready
L_V_{DD} : V_{DD} for Link Digital Core and Link I/Os
PAR : Parity
PC0-PC2 : Power Class Input
PCI_V_{DD} : V_{DD} for PCI I/Os
PCLK : PCI Clock
$\overline{PERR}$: Parity Error
PIN_EN : Pin Enable Input
$\overline{PME}$: PME Output
PORTDIS : Port Disable
$\overline{PRST}$: Reset
P_AV_{DD} : PHY Analog V_{DD}
P_DV_{DD} : PHY Digital V_{DD}
$\overline{P\_RESETB}$: PHY Power on Reset Input
$\overline{REQ}$: Bus_master Request
RI0 : Resistor0 for Reference Current Setting
RI1 : Resistor1 for Reference Current Setting
$\overline{SERR}$: System Error
$\overline{STOP}$: PCI Stop
SUS_RESM : Suspend/Resume Function Select
TpA0n : Port-1 Twisted Pair A Negative Input/Output
TpA0p : Port-1 Twisted Pair A Positive Input/Output
TpA1n : Port-2 Twisted Pair A Negative Input/Output
TpA1p : Port-2 Twisted Pair A Positive Input/Output
TpA2n : Port-3 Twisted Pair A Negative Input/Output
TpA2p : Port-3 Twisted Pair A Positive Input/Output
TpB0n : Port-1 Twisted Pair B Negative Input/Output
TpB0p : Port-1 Twisted Pair B Positive Input/Output
TpB1n : Port-2 Twisted Pair B Negative Input/Output
TpB1p : Port-2 Twisted Pair B Positive Input/Output
TpB2n : Port-3 Twisted Pair B Negative Input/Output
TpB2p : Port-3 Twisted Pair B Positive Input/Output
TpBias0 : Port-1 Twisted Pair Bias Voltage Output
TpBias1 : Port-2 Twisted Pair Bias Voltage Output
TpBias2 : Port-3 Twisted Pair Bias Voltage Output
$\overline{TRDY}$: Target Ready
XI : X'tal XI
XO : X'tal XO

CONTENTS

1. PIN FUNCTIONS

1.1 PCI/Cardbus Interface Signals: (52 pins)

(1/2)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
PAR	I/O	45	PCI/Cardbus	5/3.3	**Parity** is even parity across AD0-AD31 and $\overline{CBE0}$-$\overline{CBE3}$. It is an input when AD0-AD31 is an input; it is an output when AD0-AD31 is an output.	Link[*1]
AD0-AD31	I/O	11-14,16-19, 24-27,29,30, 32,33,49,50, 52,53,55-58, 61-64,66-69	PCI/Cardbus	5/3.3	**PCI Multiplexed Address and Data**	Link
$\overline{CBE0}$-$\overline{CBE3}$	I	22,35,47,60	-	5/3.3	**Command/Byte Enables** are multiplexed Bus Commands & Byte enables.	Link
$\overline{FRAME}$	I/O	36	PCI/Cardbus	5/3.3	**Frame** is asserted by the initiator to indicate the cycle beginning and is kept asserted during the burst cycle. If Cardbus mode (CARD_ON = 1), this pin should be pulled up to V_{DD}.	Link
$\overline{TRDY}$	I/O	38	PCI/Cardbus	5/3.3	**Target Ready** indicates that the current data phase of the transaction is ready to be completed.	Link
$\overline{IRDY}$	I/O	37	PCI/Cardbus	5/3.3	**Initiator Ready** indicates that the current bus master is ready to complete the current data phase. During a write, its assertion indicates that the initiator is driving valid data onto the data bus. During a read, its assertion indicates that the initiator is ready to accept data from the currently-addressed target.	Link
$\overline{REQ}$	O	8	PCI/Cardbus	5/3.3	**Bus_master Request** indicates to the bus arbiter that this device wants to become a bus master.	Link
$\overline{GNT}$	I	7	-	5/3.3	**Bus_master Grant** indicates to this device that access to the bus has been granted.	Link
IDSEL	I	23	-	5/3.3	**Initialization Device Select** is used as chip select for configuration read/write transaction during the phase of device initialization. If Cardbus mode (CARD_ON = 1), this pin should be pulled up to V_{DD}.	Link

(2/2)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
$\overline{\text{DEVSEL}}$	I/O	39	PCI/Cardbus	5/3.3	**Device Select** when actively driven, indicates that the driving device has decoded its address as the target of the current access.	Link
$\overline{\text{STOP}}$	I/O	42	PCI/Cardbus	5/3.3	**PCI Stop** when actively driven, indicates that the target is requesting the current bus master to stop the transaction.	Link
$\overline{\text{PME}}$	O	3	PCI/Cardbus	5/3.3	**PME Output** for power management enable.	Link
$\overline{\text{CLKRUN}}$	I/O	2	PCI/Cardbus	5/3.3	**PCICLK Running** as input, to determine the status of PCLK; as output, to request starting or speeding up clock.	Link
$\overline{\text{INTA}}$	O	4	PCI/Cardbus	5/3.3	**Interrupt** the PCI interrupt request A.	Link
$\overline{\text{PERR}}$	I/O	43	PCI/Cardbus	5/3.3	**Parity Error** is used for reporting data parity errors during all PCI transactions, except a Special Cycle. It is an output when AD0-AD31 and PAR are both inputs. It is an input when AD0-AD31 and PAR are both outputs.	Link
$\overline{\text{SERR}}$	O	44	PCI/Cardbus	5/3.3	**System Error** is used for reporting address parity errors, data parity errors during the Special Cycle, or any other system error where the effect can be catastrophic. When reporting address parity errors, it is an output.	Link
$\overline{\text{PRST}}$	I	5	-	5/3.3	**Reset** PCI reset	Link
PCLK	I	6	-	5/3.3	**PCI Clock** 33 MHz system bus clock.	Link

1.2 Cable Interface Signals: (15 pins)

(1/2)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
TpA0p	I/O	140	-	-	**Port-1 Twisted Pair A Positive Input/Output** Note	PHY Analog *2
TpA0n	I/O	139	-	-	**Port-1 Twisted Pair A Negative Input/Output** Note	PHY Analog
TpB0p	I/O	138	-	-	**Port-1 Twisted Pair B Positive Input/Output** Note	PHY Analog
TpB0n	I/O	137	-	-	**Port-1 Twisted Pair B Negative Input/Output** Note	PHY Analog
TpA1p	I/O	136	-	-	**Port-2 Twisted Pair A Positive Input/Output** Note	PHY Analog
TpA1n	I/O	135	-	-	**Port-2 Twisted Pair A Negative Input/Output** Note	PHY Analog
TpB1p	I/O	134	-	-	**Port-2 Twisted Pair B Positive Input/Output** Note	PHY Analog
TpB1n	I/O	133	-	-	**Port-2 Twisted Pair B Negative Input/Output** Note	PHY Analog
TpA2p	I/O	132	-	-	**Port-3 Twisted Pair A Positive Input/Output** Note	PHY Analog
TpA2n	I/O	131	-	-	**Port-3 Twisted Pair A Negative Input/Output** Note	PHY Analog
TpB2p	I/O	130	-	-	**Port-3 Twisted Pair B Positive Input/Output** Note	PHY Analog
TpB2n	I/O	129	-	-	**Port-3 Twisted Pair B Negative Input/Output** Note	PHY Analog

Note If unused port, please refer to **4.1.4 Unused Ports**.

(2/2)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
PORTDIS	I	105			**Port Disable** SUS_RESM = 1 This selected state will be loaded to Disabled bit which allocated PHY register Port Status Page. 1:Disable At this time, all ports will be disabled. SUS_RESM = 0 PORTDIS has no effect.	PHY Digital *3
SUS_RESM	I	106			**Suspend/Resume Function Select** 1 : Suspend/Resume On (P1394a draft 2.0 compliant) 0 : Suspend/Resume Off (P1394a draft 1.3 compliant)	PHY Digital
CPS	I	123	-	-	**Cable Power Status Input** Note	PHY Digital

Note Please refer to **4.1.3 CPS**.

1.3 PHY Signals: (9 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
TpBias0	O	128	-	-	**Port-1 Twisted Pair Bias Voltage Output** Note 1	PHY Analog
TpBias1	O	127	-	-	**Port-2 Twisted Pair Bias Voltage Output** Note 1	PHY Analog
TpBias2	O	126	-	-	**Port-3 Twisted Pair Bias Voltage Output** Note 1	PHY Analog
RI0	-	121	-	-	**Resistor0 for Reference Current Setting** Note 2	PHY Analog
RI1	-	122	-	-	**Resistor1 for Reference Current Setting** Note 2	PHY Analog
FIL1	-	114	-	-	**APLL Filter Terminal** (No need to assemble)	PHY Analog
FIL0	-	115	-	-	**APLL Filter GND** (No need to assemble)	PHY Analog
XI	I	117	-	-	**X'tal XI**	PHY Analog
XO	O	118	-	-	**X'tal XO**	PHY Analog

Notes 1. If unused port, please refer to **4.1.4 Unused Ports**.

2. Please refer to **4.6 RI0, RI1**.

1.4 PHY Control Signals: (5 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
PC0-PC2	I	93-95	-	3.3	**Power Class Input** Note 1	PHY Digital
CMC	I	96	-	3.3	**Configuration Manager Capable** Note 1	PHY Digital
$\overline{\text{P\_RESETB}}$	I	110			**PHY Power on Reset Input** Note 2	PHY Digital

Notes 1. Please refer to **4.4 PC0-PC2, CMC**.

2. Please refer to **4.5 P_RESETB**.

1.5 PCI/Cardbus Select Signals: (2 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
CARD_ON	I	157	-	3.3	**PCI/Card Select** (1:Cardbus, 0:PCI bus)	Link
$\overline{\text{CIS\_ON}}$	I	156	-	3.3	**CIS Register ON** CARD_ON / $\overline{\text{CIS\_ON}}$ / CIS / $\overline{\text{PME}}$ 0 / 1 / Off / $\overline{\text{PME}}$ 0 / 0 / On / CSTSCHG 1 / X / On / CSTSCHG	Link

1.6 Serial ROM Interface Signals: (3 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
GROM_SDA	I/O	153	6 mA	3.3	**Serial EEPROM Data Input / Output**	Link
GROM_SCL	O	154	6 mA	3.3	**Serial EEPROM Clock Output**	Link
GROM_EN	I	155	-	3.3	**Serial EEPROM Enable** (1: GUID Load enabled, 0: GUID Load disabled)	Link

1.7 Miscellaneous Signal: (1 pin)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
PIN_EN	I	73	-	5/3.3	**Pin Enable Input** (High clamped)	Link

1.8 IC: (21 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
IC(H)	I	75	-	-	**Internally Connected** (High clamped)	Link
	I	99,100	-	-	**Internally Connected** (High clamped)	PHY Digital
IC(L)	I	89,158,159	-	-	**Internally Connected** (Low clamped)	Link
	I	91,101,102	-	-	**Internally Connected** (Low clamped)	PHY Digital
IC(N)	-	74,76-79,82-84,86-88,92	-	-	**Internally Connected** (Open)	-

1.9 V_{DD}

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function	
PCI_V_{DD}	-	10,31,51,70	-	5/3.3	**V_{DD} for PCI I/Os**	Link
L_V_{DD}	-	1,20,40,46,59,72,81,151	-	3.3	**V_{DD} for Link digital Core and Link I/Os**	Link
P_DV_{DD}	-	97,103,107,108,149	-	3.3	**PHY digital V_{DD}**	PHY Digital
P_AV_{DD}	-	111	-	3.3	**PHY PLL V_{DD}**	PHY Analog
	-	116	-	3.3	**PHY PLL, OSC V_{DD}**	PHY Analog
	-	120,125	-	3.3	**PHY Bias V_{DD}**	PHY Analog
	-	146-148	-	3.3	**PHY Port V_{DD}**	PHY Analog

1.10 GND

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
DGND	-	9,15,21,28,34,41,48,54, 65,71,80,85,90,98,104, 109,150,152,160	-	-	**Digital GND**
AGND	-	112	-	-	**PHY PLL GND**
	-	113	-	-	**PHY PLL, OSC GND**
	-	119,124	-	-	**PHY Bias GND**
	-	141	-	-	**PHY Common GND**
	-	142	-	-	**PHY Speed Signal GND**
	-	143,144,145	-	-	**PHY Port GND**

[Caution]

*1: If the Link pin is pulled up, it should be connected to L_V_{DD}.

*2: If the PHY Digital pin is pulled up, it should be connected to P_DV_{DD}.

*3: If the PHY Analog pin is pulled up, it should be connected to P_AV_{DD}.

2. PHY REGISTERS

2.1 Complete Structure for PHY Registers

Figure 2-1. Complete Structure of PHY Registers

	0	1	2	3	4	5	6	7
0000	Physical_ID						R	PS
0001	RHB	IBR	Gap_count					
0010	Extended (7)			Reserved	Total_ports			
0011	Max_speed			Reserved	Delay			
0100	Link_active	Contender	Jitter			Pwr_class		
0101	Resume_int	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
0110	Reserved							
0111	Page_select			Reserved	Port_select			
1000	Register0 (page_select)							
1001	Register1 (page_select)							
1010	Register2 (page_select)							
1011	Register3 (page_select)							
1100	Register4 (page_select)							
1101	Register5 (page_select)							
1110	Register6 (page_select)							
1111	Register7 (page_select)							

Table 2-1. Bit Field Description (1/3)

Field	Size	R/W	Reset value	Description
Physical_ID	6	R	000000	Physical_ID value selected from Self_ID period.
R	1	R	0	If this bit is 1, the node is root. 1: Root 0: Not root
PS	1	R		Cable power status. 1: Cable power on 0: Cable power off
RHB	1	R/W	0	Root Hold -off bit. If 1, becomes root at the bus reset.
IBR	1	R/W	0	Initiate bus reset. Setting to 1 begins a long bus reset. Long bus reset signal duration: 166 μs. Returns to 0 at the beginning of bus reset.
Gap_count	6	R/W	111111	Gap count value. It is updated by the changes of transmitting and receiving the PHY configuration packet Tx/Rx. The value is maintained after first bus reset. After the second bus reset it returns to reset value.

Table 2-1. Bit Field Description (2/3)

Field	Size	R/W	Reset value	Description
Extended	3	R	111	Shows the extended register map.
Total_ports	4	R	0011	Supported port number. 0011: 3 ports
Max_speed	3	R	010	Indicate the maximum speed that this node supports. 010: 98.304, 196.608 and 393.216 Mbps
Delay	4	R	0010	Indicate worst case repeating delay time. 144 + (2 x 20) = 184 ns
Link_active	1	R/W	1	Link active. 1: Enable 0: Disable The logical AND status of this bit and LPS. State will be referred to “L bit” of Self-ID Packet#0. The LPS is a PHY/Link interface signal and is defined in P1394a draft 2.0. It is an internal signal in the μPD72870B.
Contender	1	R/W	See Description	Contender. “1” indicate this node support bus manager function. This bit will be referred to “C bit” of Self-ID Packet#0. The reset data is depending on CMC pin setting. CMC pin condition 1: Pull up (Contender) 0: Pull down (Non Contender)
Jitter	3	R	010	The difference of repeating time (Max.-Min.). (2+1) x 20 = 60 ns
Pwr_class	3	R/W	See Description	Power class. Please refer to IEEE1394 -1995 [4.3.4.1]. This bit will be referred to Pwr field of Self-ID Packet#0. The reset data will be determined by PC0-PC2 Pin status.
Resume_int	1	R/W	0	Resume interrupt enable. When set to 1, if any one port does resume, the Port_event bit becomes 1.
ISBR	1	R/W	0	Initiate short (arbitrated) bus reset. Setting to 1 acquires the bus and begins short bus reset. Short bus reset signal output : 1.3 μs Returns to 0 at the beginning of the bus reset.
Loop	1	R/W	0	Loop detection output. 1: Detection Writing 1 to this bit clears it to 0. Writing 0 has no effect.
Pwr_fail	1	R/W	0	Power cable disconnect detect. It becomes 1 when there is a change from 1 to 0 in the CPS bit. Writing 1 to this bit clears it to 0. Writing 0 has no effect.
Timeout	1	R/W	0	Arbitration state machine time-out. Writing 1 to this bit clears it to 0. Writing 0 has no effect.

Table 2-1. Bit Field Description (3/3)

Field	Size	R/W	Reset value	Description
Port_event	1	R/W	0	Set to 1 when the Int_Enable bit in the register map of each port is 1 and there is a change in the ports connected, Bias, Disabled and Fault bits. Set to 1 when the Resume_int bit is 1 and any one port does resume. Writing 1 to this bit clears it to 0. Writing 0 has no effect.
Enab_accel	1	R/W	0	Enables arbitration acceleration. Ack-acceleration and Fly-by arbitration are enabled. 1: Enabled 0: Disabled If this bit changes while the bus request is pending, the operation is not guaranteed.
Enab_multi	1	R/W	0	Enable multi-speed packet concatenation. Setting this bit to 1 follows multi-speed transmission. When this bit is set to 0,the packet will be transmitted with the same speed as the first packet.
Page_select	3	R/W	000	Select page address between 1000 to 1111. 000: Port Status Page 001: Vendor Definition Page Others: Unused
Port_select	4	R/W	0000	Port Selection. Selecting 000 (Port Status Page) with the page selection selects the port. 0000: Port 0 0001: Port 1 0010: Port 2 Others: Unused
Reserved	-	R	000…	Reserved. Read as 0.

2.2 Port Status Page (Page 000)

Figure 2-2. Port Status Page

	0	1	2	3	4	5	6	7
1000	AStat		BStat		Child	Connected	Bias	Disabled
1001	Negotiated_speed			Int_enable	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

Table 2-2. Bit Field Description

Field	Size	R/W	Reset value	Description
AStat	2	R	XX	A port status value. 00:---, 10: “0” 01: “1”, 11: “Z”
BStat	2	R	XX	B port status value. 00:---, 10: “0” 01: “1”, 11: “Z”
Child	1	R		Child node status value. 1: Connected to child node 0 : Connected to parent node
Connected	1	R	0	Connection status value. 1: Connected 0: Disconnected
Bias	1	R		Bias voltage status value. 1: Bias voltage 0: No bias voltage
Disabled	1	R/W	See Description	The reset value is set by the PORTDIS pin. 1: Disable
Negotiated_ Speed	3	R		Shows the maximum data transfer rate of the node connected to this port. 000: 100 Mbps 001: 200 Mbps 010: 400 Mbps
Int_enable	1	R/W	0	The Port_event is set to 1 by a change to 1 of the Connected, Bias, Disable, and Fault bits.
Fault	1	R/W	0	Set to 1 if an error occurs during Suspend/Resume. Writing 1 to this bit clears it to 0. Writing 0 has no effect.
Reserved	-	R	000…	Reserved. Read as 0.

2.3 Vendor ID Page (Page 001)

Figure 2-3. Vendor ID Page

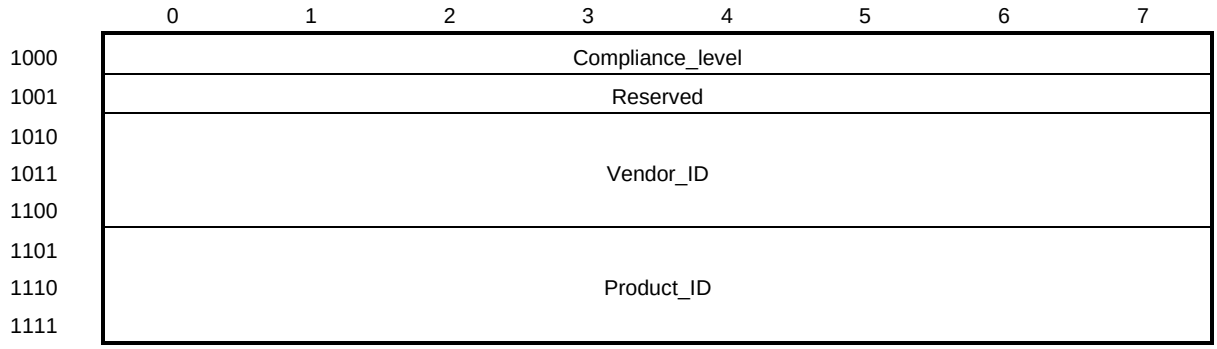


Table 2-3. Bit Field Description

Field	Size	R/W	Reset value	Description
Compliance_level	8	R	00000001	According to IEEE P1394a.
Vendor_ID	24	R	00004CH	Company ID Code value, NEC IEEE OUI.
Product_ID	24	R		Product code.
Reserved	-	R	000…	Reserved. Read as 0.

3. CONFIGURATION REGISTERS

3.1 PCI Bus Mode Configuration Register (CARD_ON = Low)

31 24	23 16	15 08	07 00	
Device ID		Vendor ID		00H
Status		Command		04H
Class Code			Revision ID	08H
BIST	Header Type	Latency Timer	Cache Line Size	0CH
Base Address 0				10H
Base Address 1				14H
Base Address 2				18H
Base Address 3				1CH
Base Address 4				20H
Base Address 5				24H
CardBus CIS Pointer				28H
Subsystem ID		Subsystem Vendor ID		2CH
Expansion Rom Base Address Register				30H
000000H			Cap_Ptr	34H
00000000H				38H
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3CH
PCI_OHCI_Control				40H
00000000H				44H
00000000H				48H
00000000H				4CH
Diagnostic register0				50H
Diagnostic register1				54H
Diagnostic register2				58H
Diagnostic register3				5CH
Power Management Capabilities		Next_Item_Ptr	Cap_ID	60H
Data	PMCSR_BSE	Power Management Control/Status		64H
00000000H				68H
00000000H				6CH
00000000H				70H
User Area (GENERAL_RegisterB)				74H
User Area (GENERAL_RegisterC)				78H
User Area (GENERAL_RegisterD)				7CH
00000000H				80H FCH

3.1.1 Offset_00 Vendor ID Register

This register identifies the manufacturer of the μPD72870B. The ID is assigned by the PCI_SIG committee.

Bits	R/W	Description
15-0	R	Constant value of 1033H.

3.1.2 Offset_02 Device ID Register

This register identifies the type of the device for the μPD72870B. The ID is assigned by NEC Corporation.

Bits	R/W	Description
15-0	R	Constant value of 00CDH.

3.1.3 Offset_04 Command Register

The register provides control over the device's ability to generate and respond to PCI cycles.

Bits	R/W	Description
0	R	**I/O enable** Constant value of 0. The μPD72870B does not respond to PCI I/O accesses.
1	R/W	**Memory enable** Default value of 1. It defines if the μPD72870B responds to PCI memory accesses. This bit should be set to one upon power-up reset. 0: The μPD72870B does not respond to PCI memory cycles 1: The μPD72870B responds to PCI memory cycles
2	R/W	**Master enable** Default value of 1. It enables the μPD72870B as bus-master on the PCI-bus. 0: The μPD72870B cannot generate PCI accesses by being a bus-master 1: The μPD72870B is capable of acting as a bus-master
3	R	**Special cycle monitor enable** Constant value of 0. The special cycle monitor is always disabled.
4	R/W	**Memory write and invalidate enable** Default value of 0. It enables Memory Write and Invalid Command generation. 0: Memory write must be used 1: The μPD72870B, when acts as PCI master, can generate the command
5	R	**VGA color palette invalidate enable** Constant value of 0. VGA color palette invalidate is always disabled.
6	R/W	**Parity error response** Default value of 0. It defines if the μPD72870B responds to $\overline{\text{PERR}}$. 0: Ignore parity error 1: Respond to parity error
7	R	**Stepping enable** Constant value of 0. Stepping is always disabled.
8	R/W	**System error enable** Default value of 0. It defines if the μPD72870B responds to $\overline{\text{SERR}}$. 0: Disable system error checking 1: Enable system error checking
9	R	**Fast back-to-back enable** Constant value of 0. Fast back-to-back transactions are only allowed to the same agent.
15-10	R	**Reserved** Constant value of 000000.

3.1.4 Offset_06 Status Register

This register tracks the status information of PCI-bus related events which are relevant to the μPD72870B. "Read" and "Write" are handled somewhat differently.

Bits	R/W	Description
3-0	R	**Reserved** Constant value of 0000.
4	R	**New capabilities** Constant value of 1. It indicates the existence of the Capabilities List.
6,5	R	**Reserved** Constant value of 00.
7	R	**Fast back-to-back capable** Constant value of 1. It indicates that the μPD72870B, as a target, cannot accept fast back-to-back transactions when the transactions are not to the same agent.
8	R/W	**Signaled parity error** Default value of 0. It indicates the occurrence of any "Data Parity". 0: No parity detected (default) 1: Parity detected
10,9	R	**DEVSEL timing** Constant value of 01. These bits define the decode timing for $\overline{\text{DEVSEL}}$. 0: Fast (1 cycle) 1: Medium (2 cycles) 2: Slow (3 cycles) 3: undefined
11	R/W	**Signaled target abort** Default value of 0. This bit is set by a target device whenever it terminates a transaction with "Target Abort". 0: The μPD72870B did not terminate a transaction with Target Abort 1: The μPD72870B has terminated a transaction with Target Abort
12	R/W	**Received target abort** Default value of 0. This bit is set by a master device whenever its transaction is terminated with a "Target Abort". 0: The μPD72870B has not received a Target Abort 1: The μPD72870B has received a Target Abort from a bus-master
13	R/W	**Received master abort** Default value of 0. This bit is set by a master device whenever its transaction is terminated with "Master Abort". The μPD72870B asserts "Master Abort" when a transaction response exceeds the time allocated in the latency timer field. 0: Transaction was not terminated with a Master Abort 1: Transaction has been terminated with a Master Abort
14	R/W	**Signaled system error** Default value of 0. It indicates that the assertion of $\overline{\text{SERR}}$ by the μPD72870B. 0: System error was not signaled 1: System error was signaled
15	R/W	**Received parity error** Default value of 0. It indicates the occurrence of any $\overline{\text{PERR}}$. 0: No parity error was detected 1: Parity error was detected

3.1.5 Offset_08 Revision ID Register

This register specifies a revision number assigned by NEC Corporation for the μPD72870B.

Bits	R/W	Description
7-0	R	Default value of 03H. It specifies the silicon revision. It will be incremented for subsequent silicon revisions.

3.1.6 Offset_09 Class Code Register

This register identifies the class code, sub-class code, and programming interface of the μPD72870B.

Bits	R/W	Description
7-0	R	Constant value of 10H. It specifies an IEEE1394 OpenHCI-compliant Host Controller.
15-8	R	Constant value of 00H. It specifies an “IEEE1394” type.
23-16	R	Constant value of 0CH. It specifies a “Serial Bus Controller”.

3.1.7 Offset_0C Cache Line Size Register

This register specifies the system cache line size, which is PC-host system dependent, in units of 32-bit words. The following cache line sizes are supported: 2, 4, 8, 16, 32, 64, and 128. All other values will be recognized as 0, i.e. cache disabled.

Bits	R/W	Description
7-0	R/W	Default value of 00H.

3.1.8 Offset_0D Latency Timer Register

This register defines the maximum amount of time that the μPD72870B is permitted to retain ownership of the bus after it has acquired bus ownership and initiated a subsequent transaction.

Bits	R/W	Description
7-0	R/W	Default value of 00H. It specifies the number of PCI-bus clocks that the μPD72870B may hold the PCI bus as a bus-master.

3.1.9 Offset_0E Header Type Register

Bits	R/W	Description
7-0	R	Constant value of 00H. It specifies a single function device.

3.1.10 Offset_0F BIST Register

Bits	R/W	Description
7-0	R	Constant value of 00H. It specifies whether the device is capable of Built-in Self Test.

3.1.11 Offset_10 Base Address 0 Register

This register specifies the base memory address for accessing all the "Operation registers" (i.e. control, configuration, and status registers) of the μPD72870B, while the BIOS is expected to set this value during power-up reset.

Bits	R/W	Description
11-0	R	Constant value of 000H. These bits are "read-only".
31-12	R/W	-

3.1.12 Offset_20 Subsystem Vendor ID Register

This register identifies the subsystem that contains the NEC's μPD72870B function. While the ID is assigned by the PCI_SIG committee, the value should be loaded into the register from the external serial ROM after power-up reset. Access to this register through PCI-bus is prohibited.

Bits	R/W	Description
15-0	R	Default value of 1033H.

3.1.13 Offset_22 Subsystem ID Register

This register identifies the type of the subsystem that contains the NEC's μPD72870B function. While the ID is assigned by the manufacturer, the value should be loaded into the register from the external serial EEPROM after power-up reset. Access to this register through PCI-bus is prohibited.

Bits	R/W	Description
15-0	R	Default value of 0063H.

3.1.14 Offset_30 Expansion Rom Base Address Register

This register is not supported by the current implementation of the μPD72870B.

Bits	R/W	Description
31-0	R	**Reserved** Constant value of 0.

3.1.15 Offset_34 Cap_Ptr Register

This register points to a linked list of additional capabilities specific to the μPD72870B, the NEC's implementation of the 1394 OpenHCI specification.

Bits	R/W	Description
7-0	R	Constant value of 60H. The value represents an offset into the μPD72870B's PCI Configuration Space for the location of the first item in the New Capabilities Linked List.

3.1.16 Offset_3C Interrupt Line Register

This register provides the interrupt line routing information specific to the μPD72870B, the NEC's implementation of the 1394 OpenHCI specification.

Bits	R/W	Description
7-0	R/W	Default value of 00H. It specifies which input of the host system interrupt controller the interrupt pin of the μPD72870B is connected to.

3.1.17 Offset_3D Interrupt Pin Register

This register provides the interrupt line routing information specific to the μPD72870B, the NEC's implementation of the 1394 OpenHCI specification.

Bits	R/W	Description
7-0	R	Constant value of 01H. It specifies PCI $\overline{\text{INTA}}$ is used for interrupting the host system.

3.1.18 Offset_3E Min_Gnt Register

This register specifies how long of a burst period the μPD72870B needs, assuming a clock rate of 33 MHz. Resolution is in units of ¼ μs. The value should be loaded into the register from the external serial EEPROM upon power-up reset, and access to this register through PCI-bus is prohibited.

Bits	R/W	Description
7-0	R	Default value of 00H. Its value contributes to the desired setting for Latency Timer value.

3.1.19 Offset_3F Max_Lat Register

This register specifies how often the μPD72870B needs to gain access to the PCI-bus, assuming a clock rate of 33 MHz. Resolution is in units of ¼ μs. The value should be loaded into the register from the external serial EEPROM after hardware reset, and access to this register through PCI-bus is prohibited.

Bits	R/W	Description
7-0	R	Default value of 00H. Its value contributes to the desired setting for Latency Timer value.

3.1.20 Offset_40 PCI_OHCI_Control Register

This register specifies the control bits that are IEEE1394 OpenHCI specific. Vendor options are not allowed in this register. It is reserved for OpenHCI use only.

Bits	R/W	Description
0	R/W	**PCI global SWAP** Default value of 0. When this bit is 1, all quadrates read from and written to the PCI Interface are byte swapped, thus a "PCI Global Swap". PCI addresses for expansion ROM and PCI Configuration registers, are, however, unaffected by this bit. This bit is not required for motherboard implementations.
31-1	R	**Reserved** Constant value of all 0.

3.1.21 Offset_60 Cap_ID & Next_Item_Ptr Register

The Cap_ID signals that this item in the Linked List is the registers defined for PCI Power Management, while the Next_Item_Ptr describes the location of the next item in the μPD72870B's Capability List.

Bits	R/W	Description
7-0	R	**Cap_ID** Constant value of 01H. The default value identified the Link List item as being the PCI Power Management registers, while the ID value is assigned by the PCI SIG.
15-8	R	**Next_Item_Ptr** Constant value of 00H. It indicated that there are no more items in the Link List.

3.1.22 Offset_62 Power Management Capabilities Register

This is a 16-bit read-only register that provides information on the power management capabilities of the μPD72870B.

Bits	R/W	Description
2-0	R	**version** Constant value of 010. The power management registers are implemented as defined in revision 1.1 of PCI Bus Power Management Interface Specification.
3	R	**PME clock** Constant value of 0.
4	R	**Reserved** Constant value of 0.
5	R	**DIS** Constant value of 0.
8-6	R	**Auxiliary power source** Constant value of 000. The alternative power source is not supported.
9	R	**D1_support** Constant value of 0. The μPD72870B does not support the D1 Power Management state.
10	R	**D2_support** Constant value of 1. The μPD72870B supports the D2 Power Management state.
15-11	R	**PME_support** Constant value of 01100.

3.1.23 Offset_64 Power Management Control/Status Register

This is a 16-bit read-only register that provides control status information of the μPD72870B.

Bits	R/W	Description
1,0	R/W	**PowerState** Default value is undefined. This field is used both to determine the current power state of the μPD72870B and to set the μPD72870B into a new power state. As D1 is not supported in the current implementation of the μPD72870B, writing of '01' will be ignored. 00: D0 (DMA contexts: ON, Link Layer: ON) 01: Reserved (D1 state not supported) 10: D2 (DMA contexts: OFF, Link Layer: OFF, LPS: OFF, $\overline{\text{PME}}$ will be asserted upon LinkON being active) 11: D3 (DMA contexts: OFF, Link Layer: OFF, LPS: OFF, $\overline{\text{PME}}$ will be asserted upon LinkON being active, Power can be removed) The LPS is a PHY/Link interface signal and is defined in P1394a draft 2.0. It is an internal signal in the μPD72870B.
7-2	R	**Reserved** Constant value of 000000.
8	R/W	**PME_En** Default value of 0. This field is used to enable the specific power management features of the μPD72870B.
12-9	R	**Data_Select** Constant value of 0000.
14,13	R	**Data_Scale** Constant value of 00.
15	R/W	**PME_Status** Default value is undefined. A write of '1' clears this bit, while a write of '0' is ignored.

3.2 CardBus Mode Configuration Register (CARD_ON = High)

31 — 24	23 — 16	15 — 08	07 — 00	
Device ID		Vendor ID		00H
Status		Command		04H
Class Code			Revision ID	08H
BIST	Header Type	Latency Timer	Cache Line Size	0CH
Base Address 0				10H
Base Address 1 (CardBus Status Reg) Note				14H
Base Address 2 (CardBus Status Reg) Note				18H
Base Address 3				1CH
Base Address 4				20H
Base Address 5				24H
CardBus CIS Pointer Note				28H
Subsystem ID		Subsystem Vendor ID		2CH
Expansion Rom Base Address Register				30H
000000H			Cap_Ptr	34H
00000000H				38H
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3CH
PCI_OHCI_Control				40H
00000000H				44H
00000000H				48H
00000000H				4CH
Diagnostic register0				50H
Diagnostic register1				54H
Diagnostic register2				58H
Diagnostic register3				5CH
Power Management Capabilities		Next_Item_Ptr	Cap_ID	60H
Data	PMCSR_BSE	Power Management Control/Status		64H
00000000H				68H
00000000H				6CH
00000000H				70H
User Area (GENERAL_RegisterB)				74H
User Area (GENERAL_RegisterC)				78H
User Area (GENERAL_RegisterD)				7CH
CIS Area Note				80H FCH

Note Different from PCI Bus Mode Configuration Register.

3.2.1 Offset_14/18 Base_Address_1/2 Register (Cardbus Status Registers)

Bits	R/W	Description
7-0	R	Constant value of 00.
31-8	R/W	-

(1) Function Event Register (FER) (Base Address 1 (2)+ 0H)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup
14-5	R	Reserved. Read only as '0'
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

(2) Function Event Mask Register (FEMR) (Base Address 1 (2)+ 4H)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup Mask
5	R	BAM. Read only as '0'
6	R	PWM. Read only as '0'
13-7	R	Reserved. Read only as '0'
14	R/W	Wakeup Mask
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

(3) Function Reset Status Register (FRSR) (Base Address 1 (2)+ 8H)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup Mask
14-5	R	Reserved. Read only as '0'
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

(4) Function Force Event Register (FFER) (Base Address 1 (2)+ CH)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup Mask
14-5	-	No Use
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

3.2.2 Offset_28 Cardbus CIS Pointer

This register specifies start memory address of the Cardbus CIS Area.

Bits	R/W	Description
31-0	R	Starting Pointer of CIS Area. Constant value of 00000080H.

3.2.3 Offset_80 CIS Area

The μPD72870B supports external Serial ROM (AT24C02 compatible) interface.

CIS Area Register can be loaded from external Serial ROM in the CIS area when CARD_ON is 1.

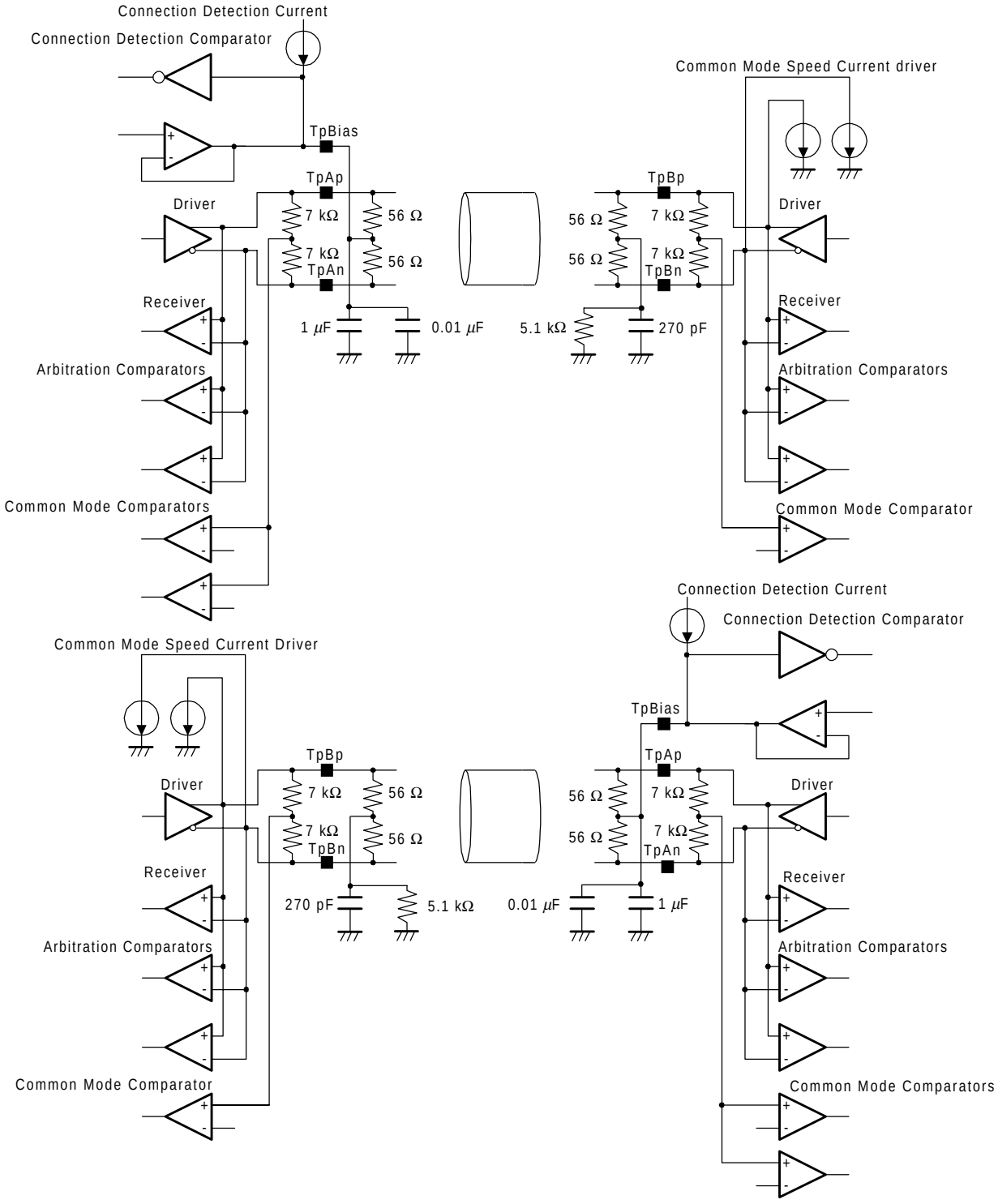
CARD_ON	$\overline{\text{CIS\_ON}}$	Bus	CIS	Function
0	1	PCI	Off	$\overline{\text{PME}}$
0	0	PCI	On	CSTSCHG
1	X	Cardbus	On	CSTSCHG

4. PHY FUNCTION

4.1 Cable Interface

4.1.1 Connections

Figure 4-1. Cable Interface



4.1.2 Cable Interface Circuit

Each port is configured with two twisted-pairs of TpA and TpB.

TpA and TpB are used to monitor the state of the Transmit/Receive line, control signals, data and cables.

During transmission to the IEEE1394 bus, the Data/Strobe signal received from the Link layer controller is encoded, converted from parallel to serial and transmitted.

While receiving from the IEEE1394 bus, the Data/Strobe signal from TpA, TpB is converted from serial to parallel after synchronization by SCLK [Note], then transmitted to the Link layer controller in 2/4/8 bits according to the data rate of 100/200/400 Mbps.

The bus arbitration for TpA and TpB and the state of the line are monitored by the built-in comparator. The state of the 1394 bus is transmitted to the state machine in the LSI.

Note The SCLK is a PHY/Link interface signal and is defined in P1394a draft 2.0. It is an internal signal in the μPD72870B.

4.1.3 CPS

An external resistance of 390 kΩ is connected in series to the power cable to monitor the power of the power cable. If the cable power falls under 7.5 V there is an indication to the Link layer that the power has failed.

4.1.4 Unused Ports

TpAp, TpAn : Not connected
TpBp, TpBn : AGND
TpBias : Connected to AGND using a 1.0 μF load capacitor
No need to assemble the capacitor if using as Suspend/Resume On mode (SUS_RESM = 1).

4.2 Suspend/Resume

4.2.1 Suspend/Resume On Mode (SUS_RESM = 1)

There are two ways of transition from the active status to the suspended status.

One is when the receipt of a remote command packet that sets the initiate suspend command. After that, the PHY transmits a remote confirmation packet with the ok bit set, subsequently signals TX_SUSPEND to the connected peer PHY with the port which specified by the port field in the remote command packet, and then the PHY port transitions to the suspended state.

The other is when the receipt of a RX_SUSPEND or RX_DISABLE_NOTIFY signal. When the port observes RX_SUSPEND, it transmits TX_SUSPEND to the active ports.

The TX_SUSPEND transmitted propagates until it reaches a leaf node. The PHY port transitions to the suspended state. The propagation of the suspended domain may be blocked by a PHY compliant with IEEE Std 1394-1995, a disabled or a suspended port.

Any one of a number of reasons may cause a suspended port to attempt to resume normal operations:

- Bias is detected and there is no fault condition;
- A resume packet is received or transmitted by the PHY;
- A remote command packet that sets the resume port command is received; or
- Either port of a node without active ports detects bias.

4.2.2 Suspend/Resume Off Mode (SUS_RESM = 0)

- Remote command packet is ignored.
- Resume packet is ignored.
- Disabled, Int_enable and resume_int bits in PHY register are ignored.
- Responses to Remote access packet.
- Detects the connection of the port in TpBias.

4.3 PLL and Crystal Oscillation Circuit

4.3.1 Crystal Oscillation Circuit

To supply the clock of 24.576 MHz ± 100 ppm, use an external capacitor of 10 pF and a crystal of 50 ppm.

4.3.2 PLL

The crystal oscillator multiplies the 24.576 MHz frequency by 16 (393.216 MHz).

4.4 PC0-PC2, CMC

CMC shows the bus manager function which corresponds to the c bit of the Self_ID packet and the Contender bit in the PHY register when the input is High.

The value of CMC can be changed with software through the Link layer; this pin sets the initial value during Power-on Reset. Use a pull-up or pull-down resistor of 10 kΩ, based on the device's specification.

The PC0-PC2 pin corresponds to the power field of the Self_ID packet and Pwr_class in the PHY register. Refer to Section 4.3.4.1 of the IEEE1394-1995 specification for information regarding the Pwr_class. The value of Pwr can be changed with software through the Link layer; this pin sets the initial value during Power-on Reset. Use a pull-up or pull-down resistor of 10 kΩ based on the application.

4.5 $\overline{\text{P\_RESETB}}$

Connect an external capacitor of 0.1 μF between the pins $\overline{\text{P\_RESETB}}$ and GND. If the voltage drops below 0 V, a reset pulse is generated. All of the circuits are initialized, including the contents of the PHY register.

4.6 RI0, RI1

Connect an external resistor of 9.1 kΩ ± 0.5 % to limit the LSI's current.

5. SERIAL ROM INTERFACE

The μPD72870B provides a serial ROM interface to initialize the 1394 Global Unique ID Register and the PCI/Cardbus Mode Configuration registers from a serial EEPROM.

The table 5-1 shows the serial EEPROM memory map required for initializing their registers.

5.1 Serial EEPROM Register

Register Address	Register Name	R/W
Base address + 0x930	SUBID register	R/W
Base address + 0x934	LATVAL register	R/W
Base address + 0x938	W_GUIDHi register	R/W
Base address + 0x93C	W_GUIDLo register	R/W
Base address + 0x940	Parameters Write register	R/W
Base address + 0x950	W_LAT register	R/W
Base address + 0x954	W_GENERAL register	R/W
Base address + 0x960	W_PHYS register	R/W
Base address + 0x980	W_CIS register	R/W

Remark Base address : Base Address 0 in Configuration register

5.2 Serial EEPROM Register Description

(1) SUBID register (Base address + 0x930)

31 — 16	15 — 0
W_SUBSYSID	W_SUBVNDID

Field	Bits	R/W	Default value	Description
W_SUBSYSID	31-16	R/W	0063H	Subsystem ID value. The value is loaded into Subsystem ID register in Configuration register (Offset+2CH bit 31-16).
W_SUBVNDID	15-0	R/W	1033H	Subsystem Vendor ID value. The value is loaded into Subsystem Vendor ID register in Configuration register (Offset+2CH bit 15-0).

(2) LATVAL register (Base address + 0x934)

31 — 24	23 — 16	15 — 12	11	10 — 4	3 — 0
W_MAXLAT	W_MINGNT	- 0 -	1	- 0 -	W_MAX_REC

Field	Bits	R/W	Default value	Description
W_MAXLAT	31-24	R/W	00H	Max Latency value. The value is loaded into Max Latency register in Configuration register (Offset+3CH bit 31-24).
W_MINGNT	23-16	R/W	00H	Min Grant value. The value is loaded into Min Grant register in Configuration register (Offset+3CH bit 23-16).
-	15-12	-	-	Reserved. Write 0 to these bits.
	11	-	-	Reserved. Write 1 to this bit.
	10-4	-	-	Reserved. Write 0 to these bits.
W_MAX_REC	3-0	R/W	9H	MAX_REC value. The value is loaded into the max_rec field of OHCI BusOption register in OHCI register (Offset+020H bit 15-12).

(3) W_GUIDHi register (Base address + 0x938)

31	0
W_GUIDHi	

Field	Bits	R/W	Default value	Description
W_GUIDHi	31-0	R/W	Undefined	GlobalUniqueIDHi value. The value is loaded into OHCI GlobalUniqueIDHi register in OHCI register (Offset+024H bit 31-0). Please refer to the 1394 Open Host Controller Interface Specification/Release 1.0 [5.5.5].

(4) W_GUIDLo register (Base address + 0x93C)

31	0
W_GUIDLo	

Field	Bits	R/W	Default value	Description
W_GUIDLo	31-0	R/W	Undefined	GlobalUniqueIDLo value. The value is loaded into GlobalUniqueIDLo register in OHCI register (Offset+028H bit 31-0). Please refer to the 1394 Open Host Controller Interface Specification/Release 1.0 [5.5.5].

(5) Parameters Write register (Base address + 0x940)

31	7	6	4	3	1	0
- 0 -		PAGE_S		- 0 -		PAR_W

Field	Bits	R/W	Default value	Description
-	31-7	-	-	Reserved. Write 0 to these bits.
PAGE_S	6-4	R/W	000	Write register select page. The bit field returns zero when read. 000: Select SUBID register and LATVAL register. 001: Select W_GUIDHi register and W_GUIDLo register. 010: Select W_LAT register and W_GENERAL register (W_GENERAL_0). 011: Select W_GENERAL register (W_GENERAL_1 and W_GENERAL_2). 100: Select W_PHYS register (W_ programPhyEnable, W_aPhyEnhanceEnable). 101: Select W_CIS register (W_CIS_EVEN - W_CIS_ODD).
-	3-1	-	-	Reserved. Write 0 to these bits.
PAR_W	0	R/W	0	Write control signal. The bit field returns zeros when read. 1: Write the value of select page defined PAGE_S. One write transaction is the units of 8 byte. 0: Ignored.

(6) W_LAT register (Base address + 0x950)

31 - 8	7 - 3	2 - 0
- 0 -	W_LAT	- 0 -

Field	Bits	R/W	Default value	Description
-	31-8	-	-	Reserved. Write 0 to these bits.
W_LAT	7-3	R/W	00000	Latency timer value. The value is loaded into Latency Timer in Configuration register (Offset+0CH bit 15-8) when using as Cardbus mode (CARD_ON = 1). It is not loaded when using as PCI bus mode (CARD_ON = 0).
-	2-0	-	-	Reserved. Write 0 to these bits.

(7) W_GENERAL register (Base address + 0x954 - 0x95C)

31 - 0
W_GENERAL_0 (Base address + 0x954) - W_GENERAL_2 (Base address + 0x95C)

Field	Bits	R/W	Default value	Description
W_GENERAL_0 - W_GENERAL_2	31-0	R/W	Undefined	User define value. The value is loaded into GENERAL_registerB - D in Configuration register (Offset+70H - 7BH).

(8) W_PHYS register (Base address + 0x960)

31 - 10	9	8	7 - 3	2 - 0
- 0 -			- 0 -	- 1 -

W_aPhyEnhanceEnable

W_programPhyEnable

Field	Bits	R/W	Default value	Description
-	31-10	-	-	Reserved. Write 0 to these bits.
W_programPhyEnable	9	R/W	1	programPhyEnable bit. The bit is loaded into HCControl registers in OHCI register ((Offset+50H bit 23) and (54H bit 23)). Please refer to the 1394 Open Host Controller Interface Specification/Release 1.0 [5.7]. 1: P1394a enhancement is supported. 0. P1394a enhancement is not supported.
W_aPhyEnhanceEnable	8	R/W	0	aPhyEnhanceEnable bit. The bit is loaded into HCControl registers in OHCI register ((Offset+50H bit 23) and (54H bit 23)).
-	7-3	-	-	Reserved. Write 0 to these bits.
	2-0	-	-	Reserved. Write 1 to these bits.

(9) W_CIS register (Base address + 0x980 - 0x984)

31	0
W_CIS_EVEN (Base address + 0x980) - W_CIS_ODD (Base address + 0x984)	

Field	Bits	R/W	Default value	Description
W_CIS_EVEN - W_CIS_ODD	31-0	R/W	Undefined	CIS Area value. The value is loaded into CIS Area in Configuration register (Offset+80H - FCH).

Table 5-1. Serial EEPROM Memory Map

Byte address	Bit 7	6	5	4	3	2	1	0
0	W_SUBSYSID(31 : 24)							
1	W_SUBSYSID(23 : 16)							
2	W_SUBVNDID(15 : 8)							
3	W_SUBVNDID(7 : 0)							
4	W_MAXLAT(31 : 24)							
5	W_MINGNT(23 : 16)							
6	0	0	0	0	1	0	0	0
7	0	0	0	0	W_MAX_REC(3 : 0)			
8	W_GUIDHi(31 : 24)							
9	W_GUIDHi(23 : 16)							
A	W_GUIDHi(15 : 8)							
B	W_GUIDHi(7 : 0)							
C	W_GUIDLo(31 : 24)							
D	W_GUIDLo(23 : 16)							
E	W_GUIDLo(15 : 8)							
F	W_GUIDLo(7 : 0)							
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
13	W_LAT(7 : 3)					0	0	0
14	W_GENERAL_0(31 : 24)							
15	W_GENERAL_0(23 : 16)							
16	W_GENERAL_0(15 : 8)							
17	W_GENERAL_0(7 : 0)							
:	:							
:	:							
1C	W_GENERAL_2(31 : 24)							
1D	W_GENERAL_2(23 : 16)							
1E	W_GENERAL_2(15 : 8)							
1F	W_GENERAL_2(7 : 0)							
20	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	WPE	WPEE
23	0	0	0	0	0	1	1	1
:	:							
:	:							
28	W_CIS_0(31 : 24)							
29	W_CIS_0(23 : 16)							
2A	W_CIS_0(15 : 8)							
2B	W_CIS_0(7 : 0)							
:	:							
:	:							
A4	W_CIS_31(31 : 24)							
A5	W_CIS_31(23 : 16)							
A6	W_CIS_31(15 : 8)							
A7	W_CIS_31(7 : 0)							

WPE: W_programPhyEnable, WPEE: W_aPhyEnhanceEnable

5.3 Load Control

GROM_EN	CARD_ON	$\overline{\text{CIS\_ON}}$	Description
0	X	X	No loading.
1	0	1	W_SUBSYSID, W_SUBVNDID, W_MAXLAT, W_MINGNT, W_MAX_REC, W_GUIDHi/Lo, W_LAT, W_GENERAL_0 - W_GENERAL_2, W_programPhyEnable, W_aPhyEnhanceEnable are loaded.
1	0	0	All parameters (W_SUBSYSID, W_SUBVNDID, W_MAXLAT, W_MINGNT, W_MAX_REC, W_GUIDHi/Lo, W_LAT, W_GENERAL_0 - W_GENERAL_2, W_programPhyEnable, W_aPhyEnhanceEnable, W_CIS_EVEN - W_CIS_ODD) are loaded.
1	1	X	

5.4 Programming Sequence Example

The example of programming sequence to the serial EEPROM is shown below.

(1) Write SUBID register. **Note1**
(2) Write LATVAL register. **Note1**
(3) Write PAGE_S = 000 and PAR_W = 1 on Parameters Write register. **Note1**
(4) Wait over 13 ms for serial EEPROM access time. **Note1**
(5) Write W_GUIDHi register. **Note2**
(6) Write W_GUIDLo register. **Note2**
(7) Write PAGE_S = 001 and PAR_W = 1 on Parameters Write register. **Note2**
(8) Wait over 13 ms for serial EEPROM access time. **Note2**
(9) Write W_LAT register. **Note3**
(10) Write W_GENERAL register (W_GENERAL_0). **Note3**
(11) Write PAGE_S = 010 and PAR_W = 1 on Parameters Write register. **Note3**
(12) Wait over 13 ms for serial EEPROM access time. **Note3**
(13) Write W_GENERAL register (W_GENERAL_1, W_GENERAL_2). **Note4**
(14) Write PAGE_S = 011 and PAR_W = 1 on Parameters Write register. **Note4**
(15) Wait over 13 ms for serial EEPROM access time. **Note4**
(16) Write W_CIS register. **Note5**
(17) Write PAGE_S = 100 and PAR_W = 1 on Parameters Write register. **Note5**
(18) Wait over 30 ms for serial EEPROM access time. **Note5**
(19) Complete to write parameters into Serial EEPROM.
(20) Parameters are loaded from serial EEPROM after PCI reset.

Notes 1. If none of W_SUBSYSED, W_SUBVNDID, W_MAXLAT, W_MINGNT, W_HOLD_TIMER, W_MAX_REC in serial EEPROM are changed, (1)-(4) transactions don't need.

2. If none of W_GUIDHi, W_GUIDLo in serial EEPROM are changed, (5)-(8) transactions don't need.

3. If none of W_LAT, W_GENERAL_0 in serial EEPROM are changed, (9)-(12) transactions don't need.

4. If none of W_GENERAL_1, W_GENERAL_2 in serial EEPROM are changed, (13)-(15) transactions don't need.

5. If none of W_CIS_0 - W_CIS_31 in serial EEPROM are changed, (16)-(18) transactions don't need. One write transaction (Parameters Write register : PAGE_S = 100 and PAR_W = 1) is the units of 8 byte . If more than 8 byte write, you need to repeat (16)-(18). *****

***:** • Write W_CIS_0, W_CIS_1 register.
• Write PAGE_S = 100 and PAR_W = 1 on Parameters Write register.
• Wait over 30 ms for serial EEPROM access time.
:
• Write W_CIS_30, W_CIS_31 register.
• Write PAGE_S = 100 and PAR_W = 1 on Parameters Write register.
• Wait over 30 ms for serial EEPROM access time.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I	LVTTL @ (V_I < 0.5 V + V_{DD})	–0.5 to +4.6	V
		PCI @ (V_I < 3.0 V + V_{DD})	–0.5 to +6.6	V
Output voltage	V_O	LVTTL @ (V_O < 0.5 V + V_{DD})	–0.5 to +4.6	V
		PCI @ (V_O < 3.0 V + V_{DD})	–0.5 to +6.6	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Ranges

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Used to clamp reflection on PCI bus.	4.5 to 5.5	V
			3.0 to 3.6	V
Operating ambient temperature	T_A		0 to +70	°C

DC Characteristics (V_{DD} = 3.3 V ± 10 %, V_{SS} = 0 V, T_A = 0 to +70°C)

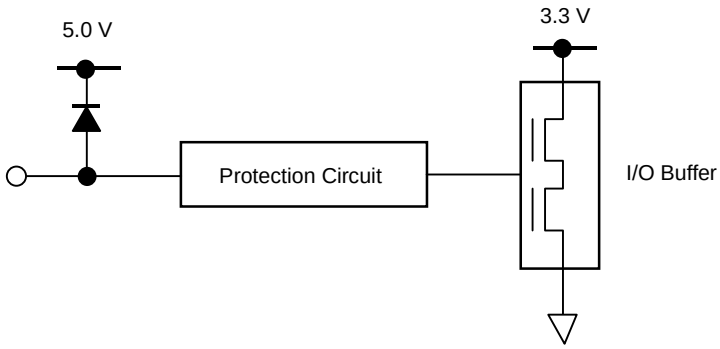
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}			2.0		V_{DD}+0.5	V
Low-level input voltage	V_{IL}			–0.5		+0.8	V
High-level output current	I_{OH}	V_{OH}	Pin No.153,154	–6			mA
		=2.4 V	Pin No.74,76-79,83,84,92	–9			mA
Low-level output current	I_{OL}	V_{OL}	Pin No.153,154	6			mA
		=0.4 V	Pin No.74,76-79,83,84,92	9			mA
Input leakage current	I_L	V_{IN} = V_{DD} or GND				±10.0	μA
Supply current	I_{DD}	3 ports, S400, V_{DD} = 3.3 V				280	mA
PCI interface							
High-level input voltage	V_{IH}			2.0		5.5	V
Low-level input voltage	V_{IL}			–0.5		+0.8	V
High-level output current	I_{OH}	V_{OH} = 2.4 V		–2			mA
Low-level output current	I_{OL}	V_{OL} = 0.4 V		9			mA
Input leakage current	I_L	V_{IN} = V_{DD} or GND				±10.0	μA
Cable interface							
Differential input voltage	V_{ID}	Cable input, 100 Mbps operation		142		260	mV
		Cable input, 200 Mbps operation		132		260	mV
		Cable input, 400 Mbps operation		118		260	mV
TpB common mode input voltage	V_{ICM}	100 Mbps speed signaling off		1.165		2.515	V
		200 Mbps speed signaling		0.935		2.515	V
		400 Mbps speed signaling		0.523		2.515	V
Differential output voltage	V_{OD}	Cable output (Test load 55Ω)		172.0		265.0	mV
TpA common mode output voltage	V_{OCM}	100 Mbps speed signaling off		1.665		2.015	V
		200 Mbps speed signaling		1.438		2.015	V
		400 Mbps speed signaling		1.030		2.015	V
TpA common mode output current	I_{CM}	100 Mbps speed signaling off		–0.81		+0.44	mA
		200 Mbps speed signaling		–4.84		–2.53	mA
		400 Mbps speed signaling		–12.40		–8.10	mA
Power status threshold voltage	V_{TH}	CPS				7.5	V
TpBias output voltage	V_{TPBIAS}			1.665		2.015	V

Remarks 1. Digital core runs at 3.3 V.

2. PCI Interface can run at 5 or 3.3 V, depending on the choice of 5 V-PCI or 3.3 V-PCI.

3. All other I/Os are 3.3 V driving, and 5 V tolerant.

4. 5 V are used only for 5 V-PCI clamping diode.



AC Characteristics

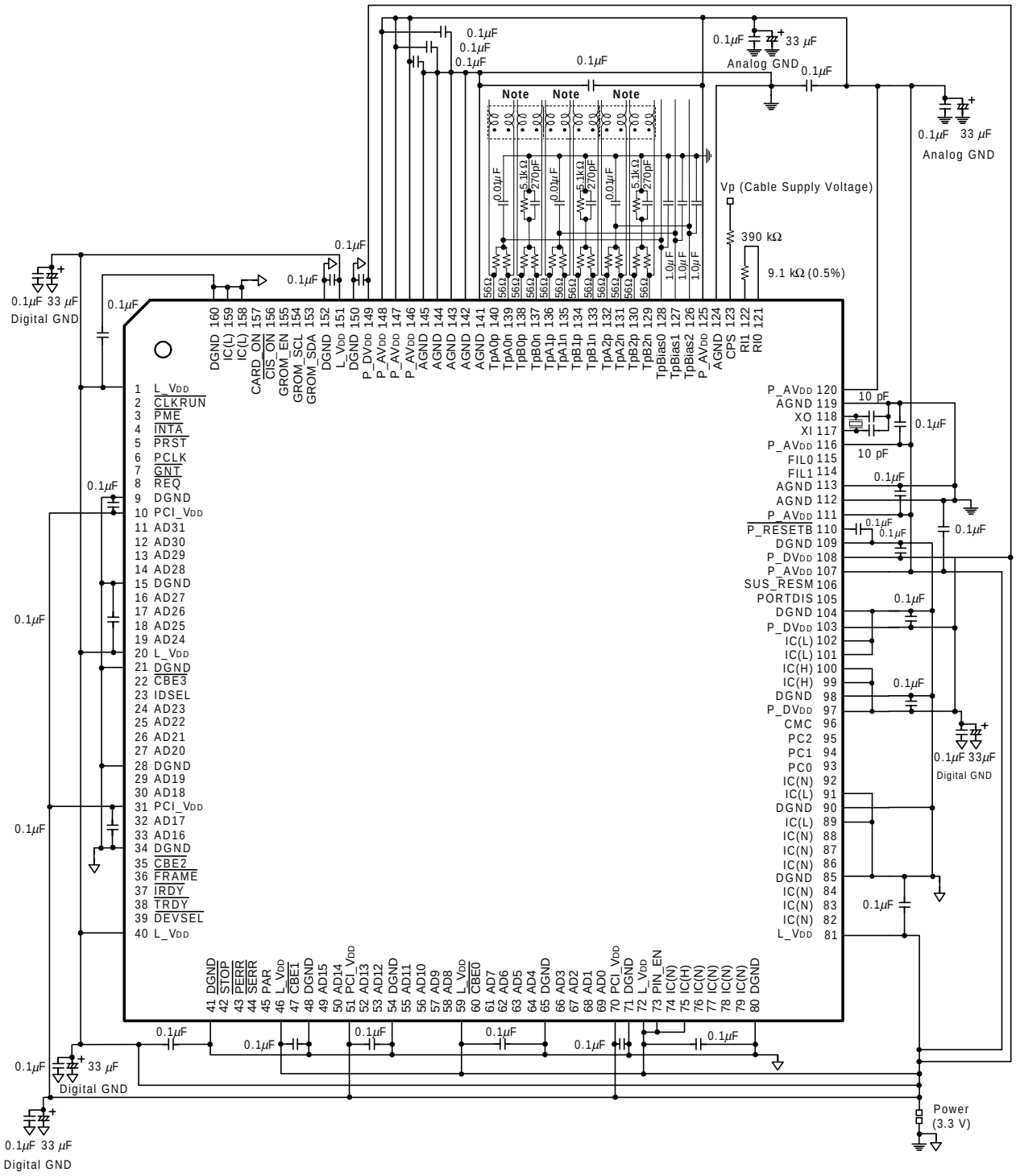
PCI Interface

See PCI local bus specification Revision 2.1.

Serial ROM Interface

See AT24C01A/02/04/08/16 Spec. Sheet.

7. APPLICATION CIRCUIT EXAMPLE



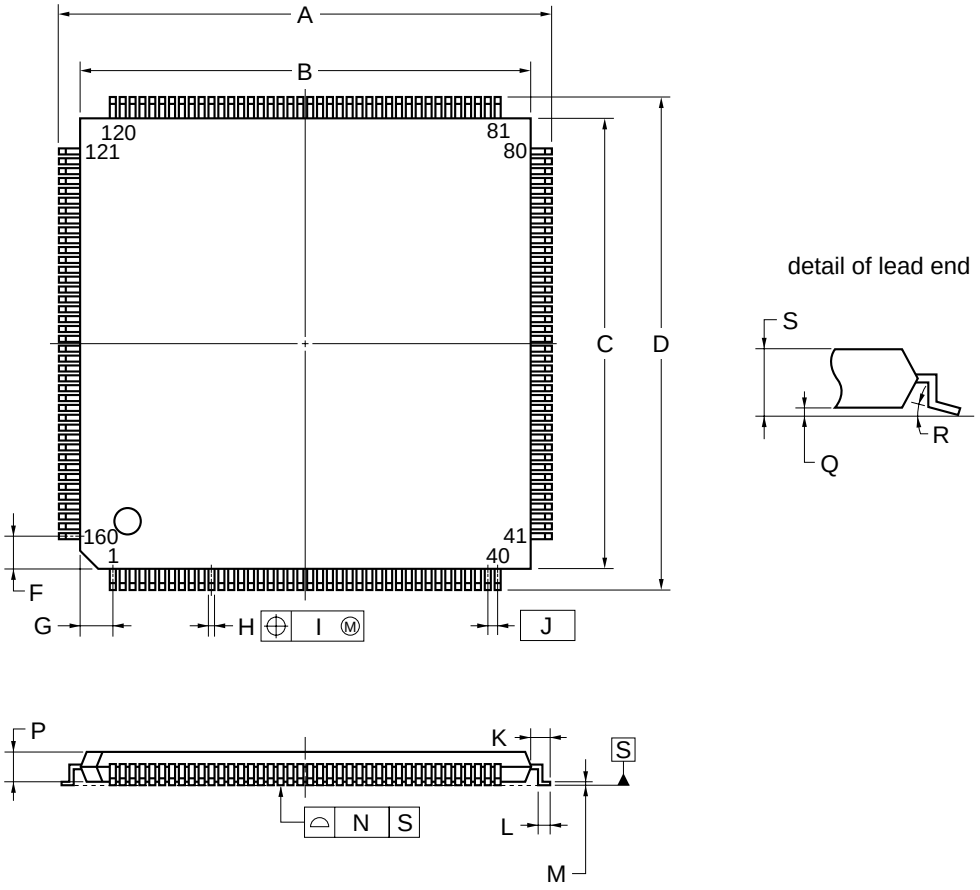
Note Common mode choke.

Recommendation : TOKO Part No. 857CM-0009 (TYPE B5W)

: MURATA Part No. PLW3216S161SQ2

8. PACKAGE DRAWINGS

160-PIN PLASTIC LQFP (FINE PITCH) (24x24)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	26.0±0.2
B	24.0±0.2
C	24.0±0.2
D	26.0±0.2
F	2.25
G	2.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.4±0.1
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.

S160GM-50-8ED-3

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 00.4