

# ACPL-M21L, ACPL-021L and ACPL-024L

## Low Power, 5 MBd Digital CMOS Optocoupler



### Data Sheet

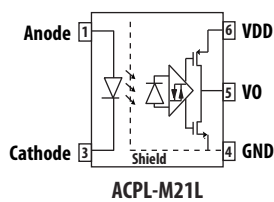


#### Description

ACPL-M21L (single channel SO-5 package), ACPL-021L (single channel SO-8 package) and ACPL-024L (dual channel SO-8 package) are optically-coupled logic gates. The detector IC has CMOS output stage and optical receiver input stage with built-in Schmitt trigger to provide logic-compatible waveforms, eliminating the need for additional waveshaping.

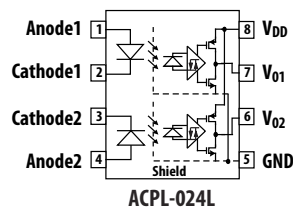
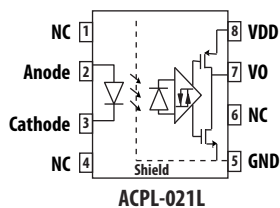
An internal shield on the ACPL-M21L/021L/024L guarantees common mode transient immunity of 25 kV/μs at a common mode voltage of 1000 V. The ACPL-x2xL optocouplers' series operates from a 2.7 V to 5.5 V supply with guaranteed AC and DC performance from an extended temperature range of -40 °C to 105 °C. Glitches free output upon power-up and power-down of optocoupler.

#### Functional Diagram



**TRUTH TABLE  
(POSITIVE LOGIC)**

LED	VO
ON	HIGH
OFF	LOW



A 0.1 μF bypass capacitor must be connected between pins Vdd and GND

#### Features

- CMOS output
- Wide supply voltage: 2.7 V – 5.5 V
- Low power supply current I<sub>DD</sub>: 1.1 mA/channel max.
- Low forward current I<sub>F</sub>: 1.6 mA min
- Speed: 5 MBd typ
- Pulse width distortion (PWD): 200 ns max
- Propagation delay skew (tpsk): 220 ns max
- Propagation delay (tp): 250 ns max
- Common mode rejection: 25 kV/μs min at V<sub>CM</sub> = 1000 V
- Hysteresis: 0.2 mA typ
- Temperature range: -40 °C to 105 °C
- Safety and regulatory approvals
  - UL 1577 recognized – 3750 Vrms for 1 minute for ACPL-M21L/021L/024L
  - CSA Approval
  - IEC/EN 60747-5-5, Approval for Reinforced Insulation

#### Applications

- Low isolation of high speed logic systems
- Computer peripheral interface
- Microprocessor system interface
- Ground loop elimination
- Pulse transformer replacement
- High speed line receiver
- Power control systems

## Ordering Information

ACPL-M21L, ACPL-024L and ACPL-021L are UL Recognized with 3750 V<sub>rms</sub> for 1 minute per UL1577.

Part number	Option	Package	Surface Mount	Tape & Reel	UL1577	IEC/EN 60747-5-5	Quantity
	RoHS Compliant				5000 V <sub>rms</sub> / 1 Minute Rating		
ACPL-M21L	-000E	SO-5	X				100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1500 per reel
	-560E		X	X		X	1500 per reel
ACPL-024L	-000E	SO-8	X				100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1500 per reel
	-560E		X	X		X	1500 per reel
ACPL-021L	-000E	SO-8	X				100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1500 per reel
	-560E		X	X		X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

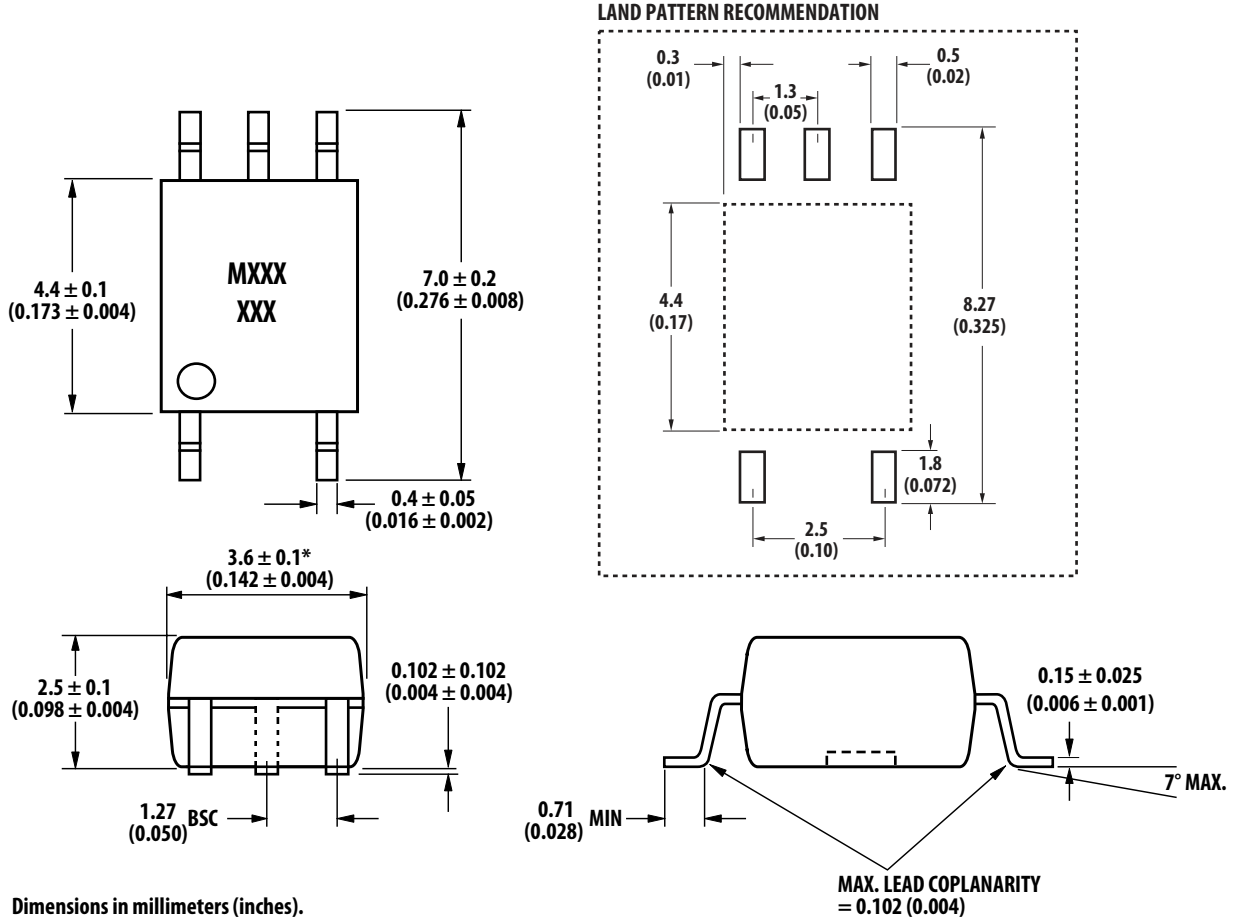
### Example 1:

ACPL-M21L-500E to order product of SO-5 package in Tape and Reel packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

# Package Outline Drawings

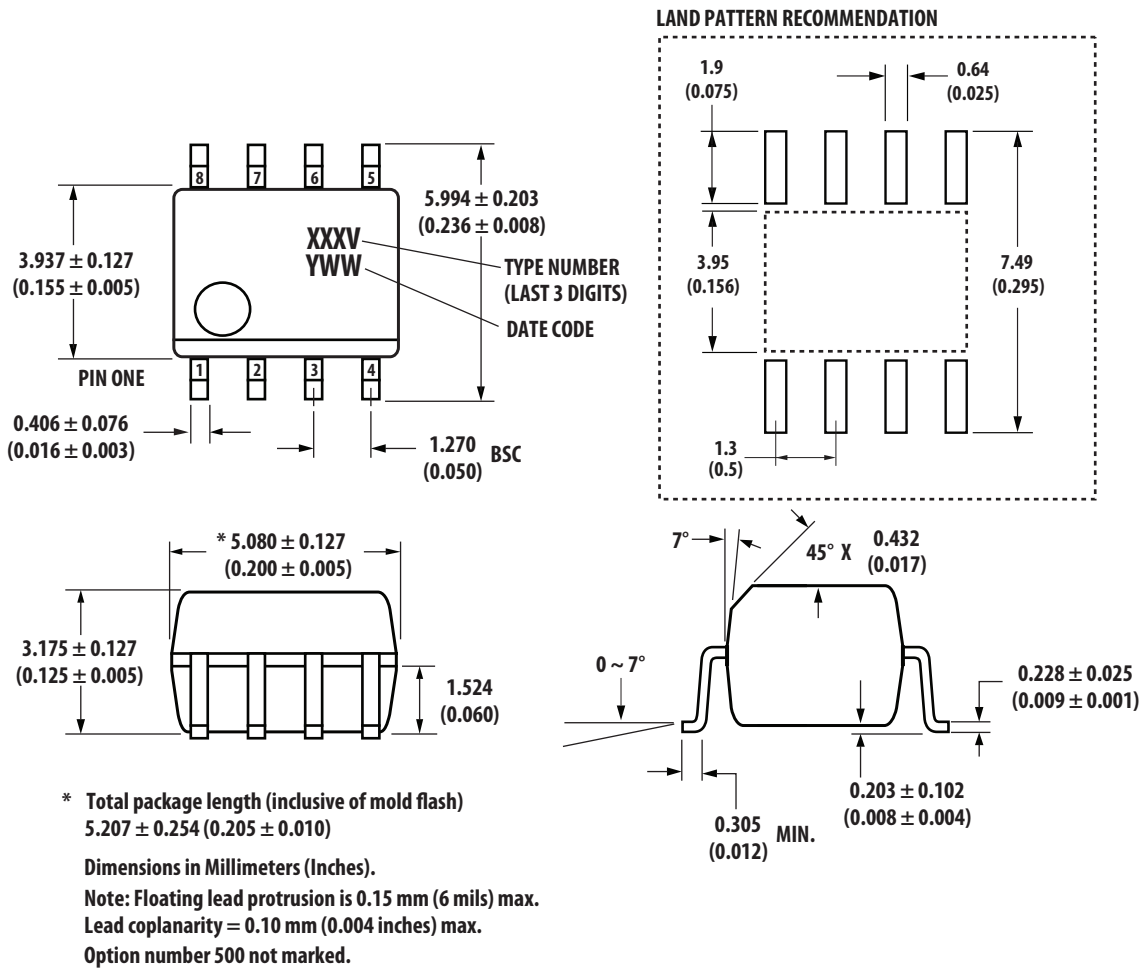
## ACPL-M21L S0-5 Package



Dimensions in millimeters (inches).  
 Note: Floating Lead Protrusion is 0.15 mm (6 mils) max.

\* Maximum Mold flash on each side is 0.15 mm (0.006).

## ACPL-024L/021L SO-8 Package



## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Regulatory Information

The ACPL-M21L/024L/021L is approved by the following organizations:

### UL

Approval under UL 1577, component recognition program up to  $V_{ISO} = 3750 V_{RMS}$  for ACPL-M21L/024L/021L

### CSA

Approval under CSA Component Acceptance Notice #5.

### IEC/EN 60747-5-5 (Option 060 only)

## Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-024L		Units	Conditions
		ACPL-M21L	ACPL-021L		
Minimum External Air Gap (Clearance)	L(101)	5	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	5	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

## IEC/EN 60747-5-5 Insulation Characteristics\* (Option 060)

Description	Symbol	Characteristic	
		ACPL-M21L/ 024L/021L	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 150 V_{rms}$ for rated mains voltage $\leq 300 V_{rms}$ for rated mains voltage $\leq 600 V_{rms}$ for rated mains voltage $\leq 1000 V_{rms}$		I – IV I – III I – II	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	567	$V_{peak}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1063	$V_{peak}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial discharge $< 5$ pC	$V_{PR}$	896	$V_{peak}$
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ sec)	$V_{IOTM}$	6000	$V_{peak}$
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	$T_S$	150	$^{\circ}C$
Input Current**	$I_{S, INPUT}$	150	mA
Output Power**	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

\* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

\*\* Refer to the following figure for dependence of  $P_S$  and  $I_S$  on ambient temperature.

## Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Condition
Storage Temperature	$T_S$	-55	125	°C	
Operating Temperature	$T_A$	-40	105	°C	
Reverse Input Voltage	$V_R$		5	V	
Supply Voltage	$V_{DD}$		6.5	V	
Average Forward Input Current	$I_F$		8	mA	
Peak Forward Input Current	$I_{F(TRAN)}$		1	A	$\leq 1 \mu s$ Pulse Width, < 300 pulses per second
Output Current	$I_O$		10	mA	At max $V_{DD}$
Output Voltage	$V_O$	-0.5	$V_{DD} + 0.5$	V	
Lead Solder Temperature	$T_{LS}$		260 °C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile		See Package Outline Drawings section			

## Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Operating Temperature	$T_A$	-40	105	°C
Input Current, Low Level	$I_{FL}$	0	250	$\mu A$
Input Current, High Level	$I_{FH}$	1.6*	6	mA
Power Supply Voltage	$V_{DD}$	2.7	5.5	V
Forward Input Voltage	$V_{F(OFF)}$		0.8	V

\* The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% LED degradation guardband.

## Electrical Specifications (DC)

Over recommended temperature ( $T_A = -40 \text{ °C}$  to  $105 \text{ °C}$ ) and supply voltage ( $2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ). All typical specifications are at  $V_{DD} = 2.7 \text{ V}$ ,  $T_A = 25 \text{ °C}$ , unless otherwise specified.

Parameter	Symbol	Channel	Min	Typ	Max	Units	Test Conditions
Input Forward Voltage	$V_F$			1.5	2.0	V	$I_F = 2.2 \text{ mA}$ (Figure 1 & 2)
Input Reverse Breakdown Voltage	$BV_R$		8	11		V	$I_R = 10 \mu A$
Logic High Output Voltage	$V_{OH}$		$V_{DD} - 0.1$			V	$I_F = 2.2 \text{ mA}$ , $I_O = -20 \mu A$
			$V_{DD} - 1.0$			V	$I_F = 2.2 \text{ mA}$ , $I_O = -3.2 \text{ mA}$ (Figure 3)
Logic Low Output Voltage	$V_{OL}$			0.001	0.1	V	$I_F = 0 \text{ mA}$ , $I_O = 20 \mu A$
				0.15	0.4	V	$I_F = 0 \text{ mA}$ , $I_O = 3.2 \text{ mA}$ (Figure 4)
Input Threshold Current	$I_{TH}$			0.5	1.4	mA	Figure 5
Logic Low Output Supply Current	$I_{DDL}$	Single		0.6	1.1	mA	$V_F = 0 \text{ V}$ , $V_{DD} = 5.5 \text{ V}$ , $I_O = \text{Open}$ (Figure 6)
		Dual		1.2	2.2		
Logic High Output Supply Current	$I_{DDH}$	Single		0.5	1.1	mA	$I_F = 2.2 \text{ mA}$ , $V_{DD} = 5.5 \text{ V}$ , $I_O = \text{Open}$ (Figure 7)
		Dual		1.0	2.2		
Input Capacitance	$C_{IN}$			77		pF	$f = 1 \text{ MHz}$ , $V_F = 0 \text{ V}$
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$			-1.9		mV/°C	$I_F = 2.2 \text{ mA}$

## Switching Specifications (AC)

Over recommended temperature ( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ), supply voltage ( $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ). All typical specifications are at  $V_{DD} = 2.7\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Propagation Delay Time to Logic Low Output <sup>[1]</sup>	$t_{PHL}$		130	250	ns	$I_F = 2.2\text{ mA}$ , $C_L = 15\text{ pF}$ (Figure 8, 12) CMOS Signal Levels
Propagation Delay Time to Logic High Output <sup>[1]</sup>	$t_{PLH}$		115	250	ns	$I_F = 2.2\text{ mA}$ , $C_L = 15\text{ pF}$ (Figure 9, 12) CMOS Signal Levels
Pulse Width Distortion <sup>[2]</sup>	PWD			200	ns	CMOS Signal Levels
Propagation Delay Skew <sup>[3]</sup>	$t_{PSK}$			220	ns	
Output Rise Time (10% – 90%)	$t_R$		11		ns	$I_F = 2.2\text{ mA}$ , $C_L = 15\text{ pF}$ , CMOS Signal Levels.
Output Fall Time (90% – 10%)	$t_F$		11		ns	$I_F = 2.2\text{ mA}$ , $C_L = 15\text{ pF}$ , CMOS Signal Levels.
Static Common Mode Transient Immunity at Logic High Output <sup>[4]</sup>	$ CM_H $	25	40		kV/ $\mu\text{s}$	$V_{CM} = 1000\text{ V}$ , $T_A = 25^\circ\text{C}$ , $I_F = 2.2\text{ mA}$ , $C_L = 15\text{ pF}$ , $V_I = 5\text{ V}$ ( $R_T = 1.6\text{ k}\Omega$ ) or $V_I = 3.3\text{ V}$ ( $R_T = 840\ \Omega$ ) CMOS Signal Levels Figure 13
Static Common Mode Transient Immunity at Logic Low Output <sup>[5]</sup>	$ CM_L $	25	40		kV/ $\mu\text{s}$	$V_{CM} = 1000\text{ V}$ , $T_A = 25^\circ\text{C}$ , $I_F = 0\text{ mA}$ , $C_L = 15\text{ pF}$ , $V_I = 0\text{ V}$ ( $R_T = 1.6\text{ k}\Omega$ ) or ( $R_T = 840\ \Omega$ ) CMOS Signal Levels Figure 13

Notes:

- $t_{PHL}$  propagation delay is measured from the 50% ( $V_{in}$  or  $I_F$ ) on the falling edge of the input pulse to the 50%  $V_{DD}$  of the falling edge of the  $V_O$  signal.  $t_{PLH}$  propagation delay is measured from the 50% ( $V_{in}$  or  $I_F$ ) on the rising edge of the input pulse to the 50% level of the rising edge of the  $V_O$  signal
- PWD is defined as  $|t_{PHL} - t_{PLH}|$
- $t_{PSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between units at any given temperature within the recommended operating conditions.
- $CM_H$  is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
- $CM_L$  is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a low logic state.
- Use of a  $0.1\ \mu\text{F}$  bypass capacitor connected between  $V_{DD}$  and ground is recommended.

## Package Characteristics

All typical at  $T_A = 25^\circ\text{C}$

Parameter	Symbol	Part Number	Min	Typ	Max	Units	Test Conditions
Input-Output Insulation	$V_{ISO}$	ACPL-M21L/ 024L/021L	3750			$V_{rms}$	$RH < 50\%$ for 1 min. $T_A = 25^\circ\text{C}$
Input-Output Resistance	$R_{I-O}$			$10^{12}$		$\Omega$	$V_{I-O} = 500\text{ V}$
Input-Output Capacitance	$C_{I-O}$			0.6		pF	$f = 1\text{ MHz}$ , $T_A = 25^\circ\text{C}$

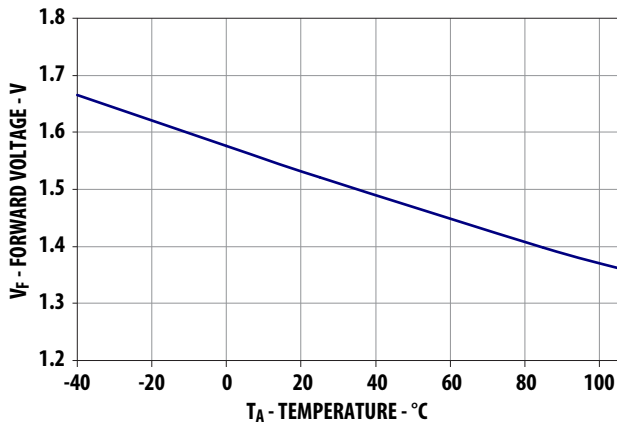


Figure 1. Forward Voltage vs. Temperature

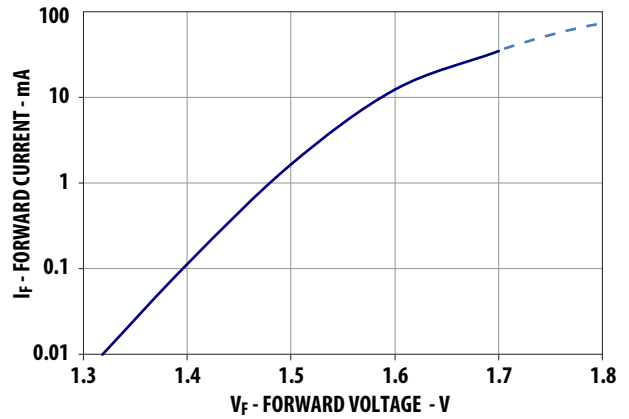


Figure 2. Forward Current vs Forward Voltage

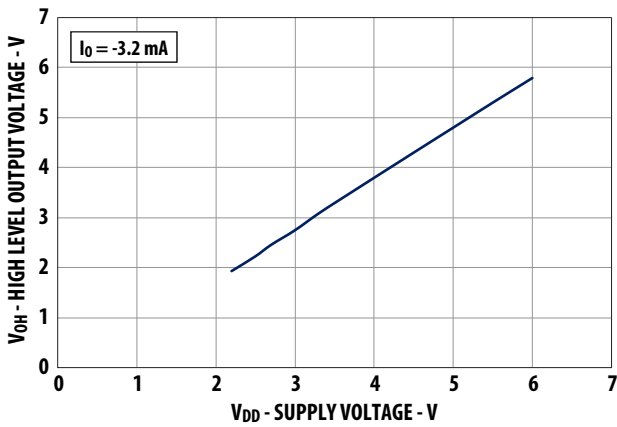


Figure 3. Logic High Output voltage vs Supply Voltage

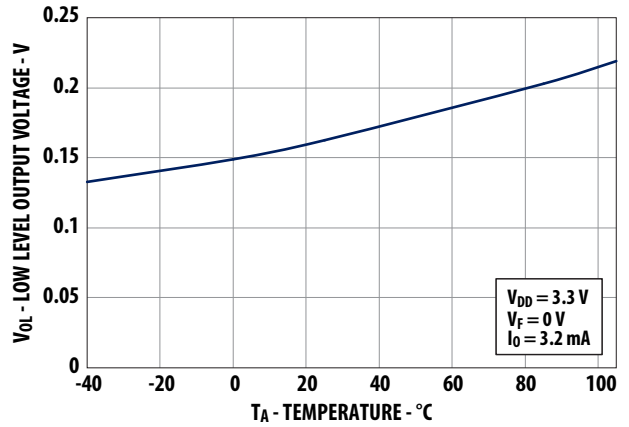


Figure 4. Logic Low Output Voltage vs. Temperature

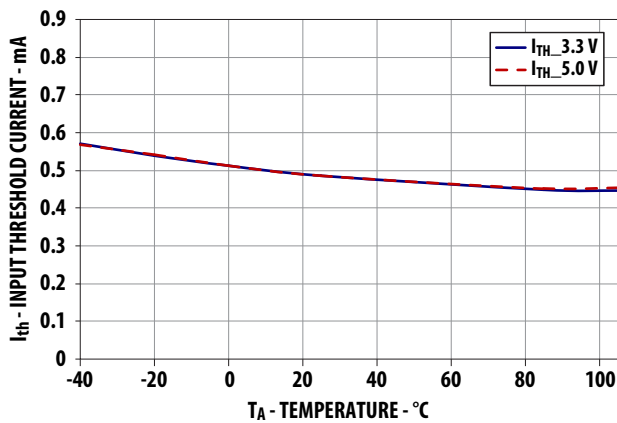


Figure 5. Input Threshold Current vs. Temperature

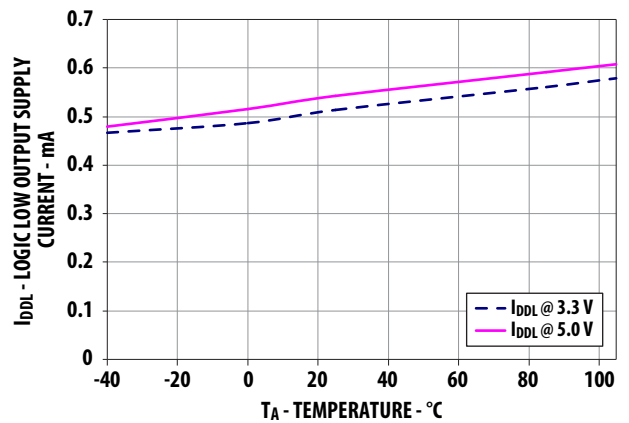


Figure 6. Logic Low Output Supply Current vs. Temperature



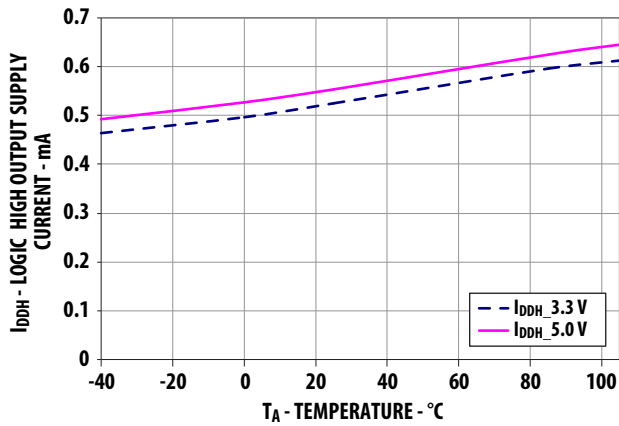


Figure 7. Logic High Output Supply Current vs. Temperature

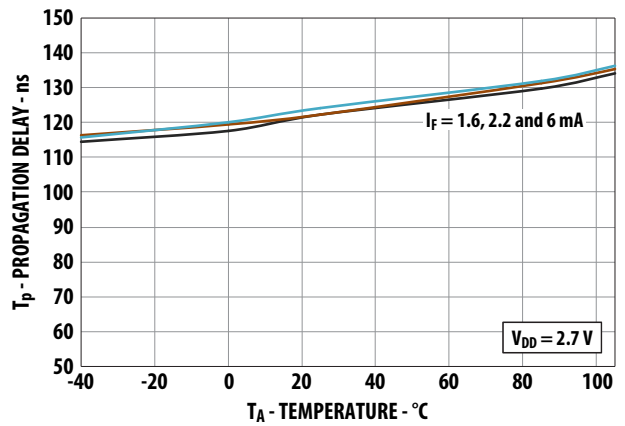


Figure 8. Propagation Delay,  $t_{PHL}$  vs. Temperature

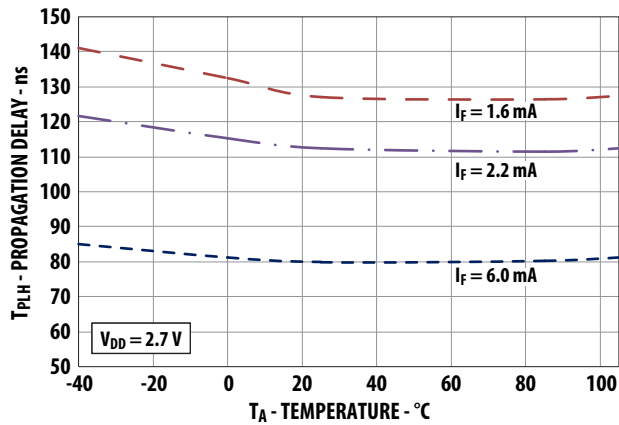


Figure 9. Propagation Delay,  $t_{PLH}$  vs. Temperature

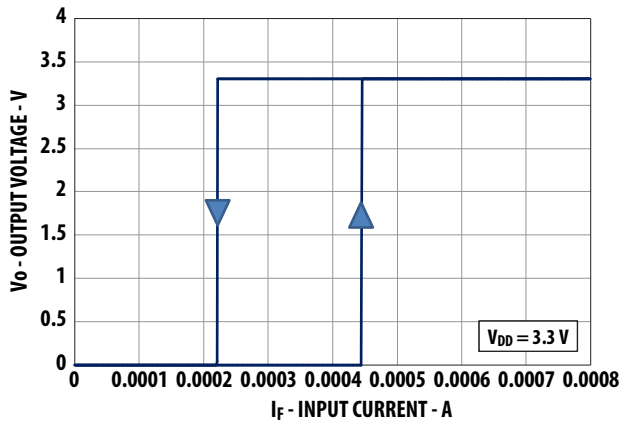


Figure 10. Output Voltage vs Input Current @  $V_{DD} = 3.3 V$

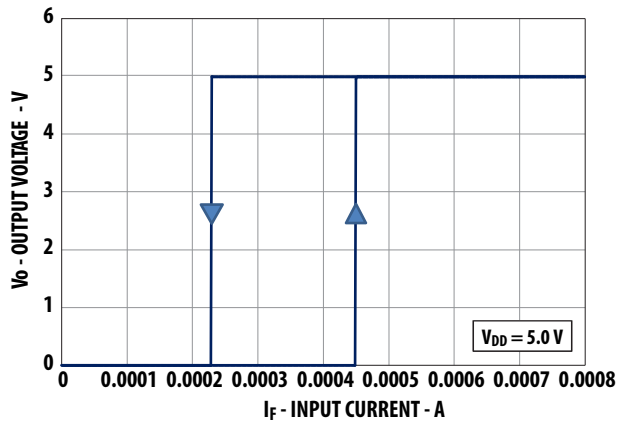
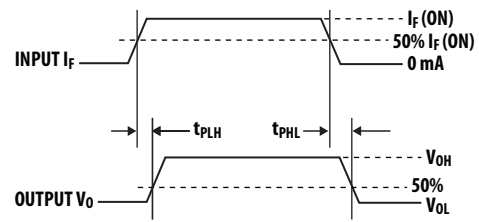
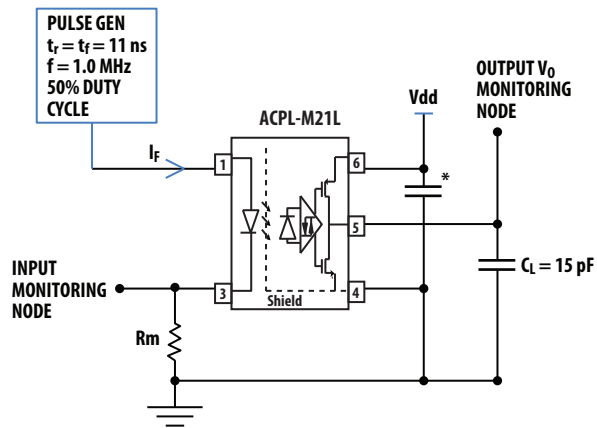


Figure 11. Output Voltage vs Input Current @  $V_{DD} = 5 V$



\* 0.1  $\mu\text{F}$  BYPASS — SEE NOTE 6 ABOVE.<sup>[6]</sup>

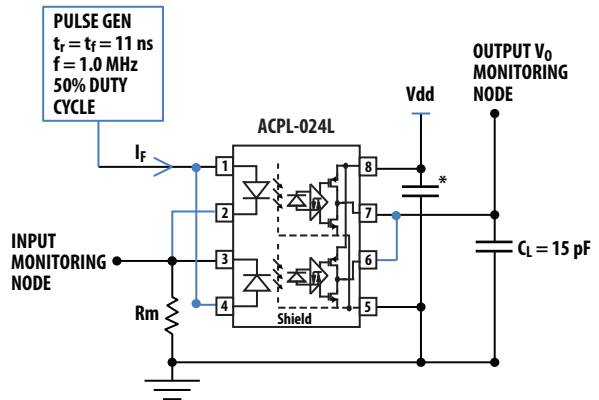
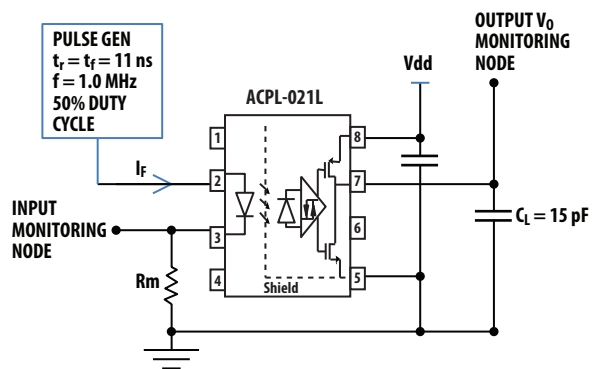


Figure 12. Circuit for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ ,  $t_f$

ACPL-M21L, ACPL-021L, ACPL-024L:

$V_1 = 3.3\text{ V}$ :  $R_1 = 510\ \Omega \pm 1\%$ ,  $R_2 = 330\ \Omega \pm 1\%$

$V_1 = 5.0\text{ V}$ :  $R_1 = 1\text{ k}\Omega \pm 1\%$ ,  $R_2 = 600\ \Omega \pm 1\%$

$R_T = R_1 + R_2$   $R_1/R_2 \approx 1.5$

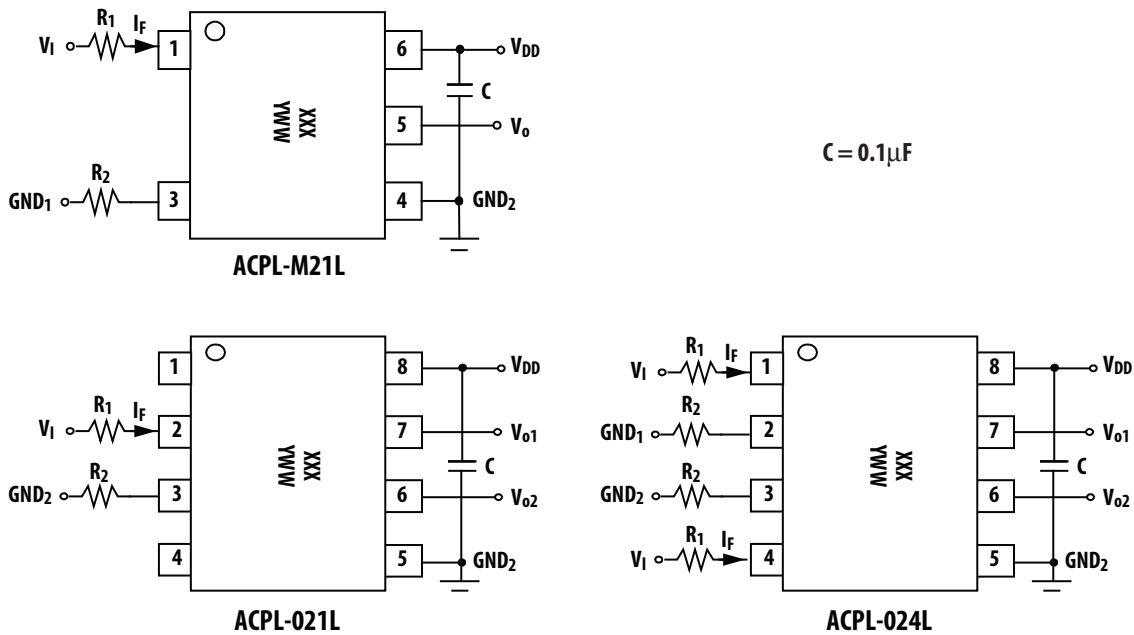


Figure 13. Recommended printed circuit board layout and input current limiting resistor selection

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

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