Before beginning any new design with this device, please contact Cirrus Logic Inc. for the latest errata information. See the back cover of this document for sales office locations and phone numbers. Note that the timing values in Section 7 apply to revision 'K' or later.

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Operating ambient temperature (T_A) ..... 0°C to 70°C
Storage temperature ..... –65°C to 150°C
All voltages with respect to ground ..... –0.5 V to V_{CC} + 0.5 V (volts)
Supply voltage (V_{CC}) ..... +7.0 V
Power dissipation ..... 0.25 W (watt)

NOTE: Stresses above those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

7.2 DC Electrical Characteristics

(@ V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	MIN	MAX	Units	Test Conditions
V_{IL}	Input low voltage	–0.5	0.8	V	
V_{IH}	Input high voltage (all pins except CLK, RESET*, and BGIN*)	2.0		V_{CC}	V
V_{OL}	Output low voltage	0.4		V	I_{OL} = 2.4 mA
V_{OH}	Output high voltage	2.4		V	I_{OH} = –400 µA
I_{IL}	Input leakage current	–10	10	µA	0 < V_{IN} < V_{CC}
I_{LL}	Data bus tristate leakage current	–10	10	µA	0 < V_{OUT} < V_{CC}
I_{OC}	Open-drain output leakage	–10	10	µA	0 < V_{OUT} < V_{CC}
I_{CC}	Power supply current		50	mA	CLK = 20 MHz
C_{IN}	Input capacitance		10	pF	
C_{OUT}	Output capacitance		10	pF	
V_{IH}	Input high voltage for CLK, RESET*, and BGIN*	2.7	V_{CC}	V	

7.3 AC Electrical Characteristics

Symbol	Parameter	MIN	MAX
t_1	CLK high to BUSCLK high		20
t_2	CLK high to BUSCLK low		20
Bus Arbitration			
t_{11}	CLK high to BGACK* tristate		25
t_{12}	BGIN* low to address valid[a]		40
t_{13}	Address hold after CLK high	0	
t_{14}	CLK high to address tristate		25
t_{15}	CLK high to ADLD* low		25
t_{16}	CLK high to ADLD* high		20
t_{17}	Address setup to ADLD* high	15	
t_{18}	CLK high to AEN*/DATEN*/DATDIR* high		25
t_{19}	CLK high to AEN*/DATEN*/DATDIR* tristate		25
t_{20}	CLK high to AEN*/DATEN*/DATDIR* low		25
DMA Read			
t_{21}	Data setup to CLK high	10	
t_{22}	Data hold after CLK high	15	
t_{23}	CLK high to address valid		30
t_{24}	CLK low to AS* low		25
t_{25}	CLK high to AS* high		20
t_{26}	CLK low to DS* low		25
t_{27}	CLK high to DS* high		20
t_{28}	DTACK* low setup to CLK high	10	
t_{29}	DTACK* high setup to CLK high (to avoid false termination)	50	
DMA Write			
t_{31}	CLK high to data valid		40
t_{32}	Data hold after CLK high	5	
t_{33}	CLK low to DS* low		25
t_{34}	CLK high to DS* high		20
t_{35}	DTACK* low setup to CLK high	10	
t_{36}	DTACK* high setup to CLK high (to avoid false termination)	50	

Symbol	Parameter	MIN	MAX
Host Read/Write			
t_{41}	DS* and CS* low setup to CLK high	7	
t_{42}	Reserved		
t_{43}	Reserved		
t_{44}	R/W* setup to CLK high	5	
t_{45}	CLK high to data valid		25
t_{46}	Data setup time to CLK high	5	
t_{47}	Data hold time after CLK high	15	
t_{48}	Address setup time to CLK high	5	
t_{49}	Address hold time after CLK high	15	
t_{50}	CLK high to DTACK* low (read cycle)		25
t_{51}	CLK high to DTACK* low (write cycle)		25
t_{52}	(CS* and DS*) low to DATEN*/DATDIR* low		25
t_{53}	DS* high to DATEN*/DATDIR* tristate		25
t_{54}	DS* high to data bus tristate		25
t_{55}	DS* high to DTACK* high-impedance		25
Interrupt Acknowledge			
t_{61}	CLK high to IACKIN*, DS* setup	20	
t_{63}	CLK high to data valid		20
t_{64}	Address setup to IACKIN* low	0	
t_{65}	Address hold after IACKIN* high	0	
t_{66}	CLK high to DTACK* low		25
t_{67}	(IACKIN* and DS*) low and BUSCLK high to DATEN* and DATDIR* low		40

[a] This timing assumes the following conditions BGACK* high, DTACK* high, DS* high, and BUSCLK high.

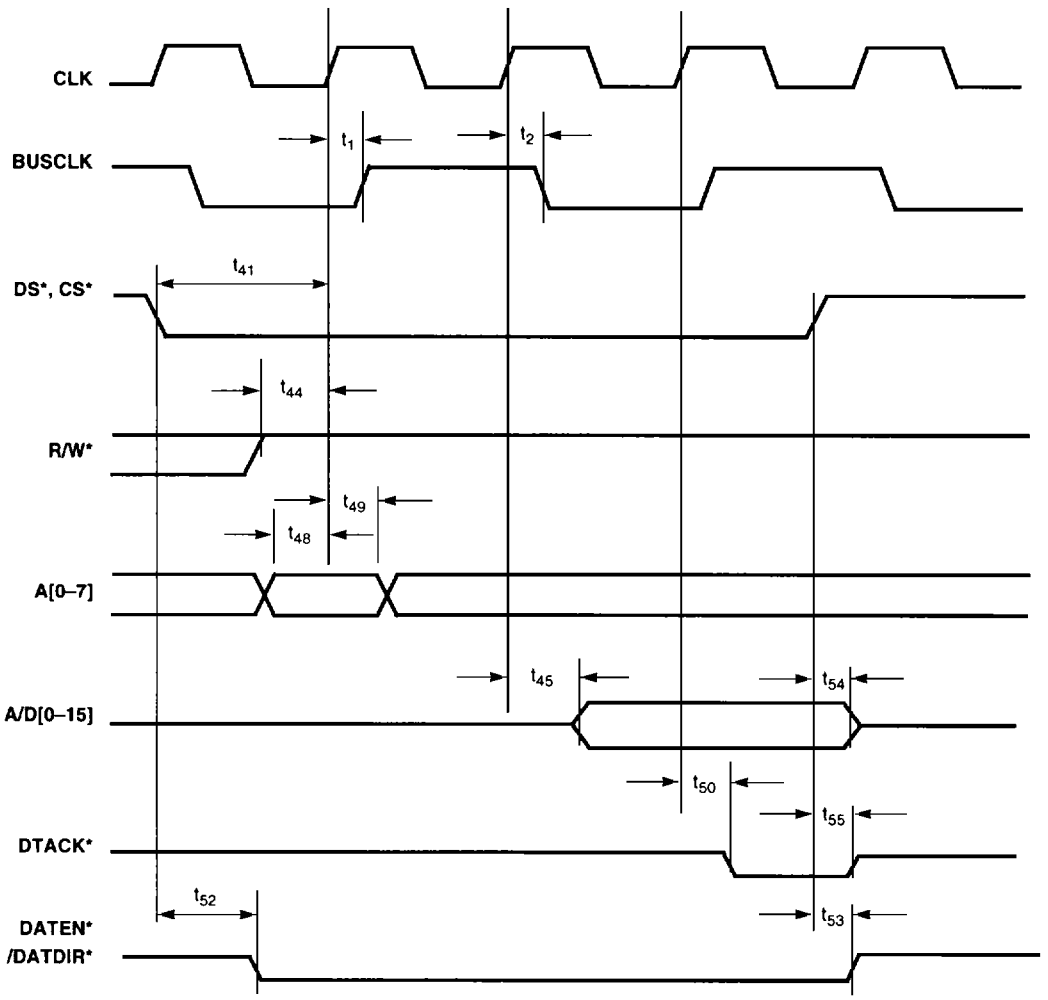


Figure 7-1. Slave Read Cycle Timing

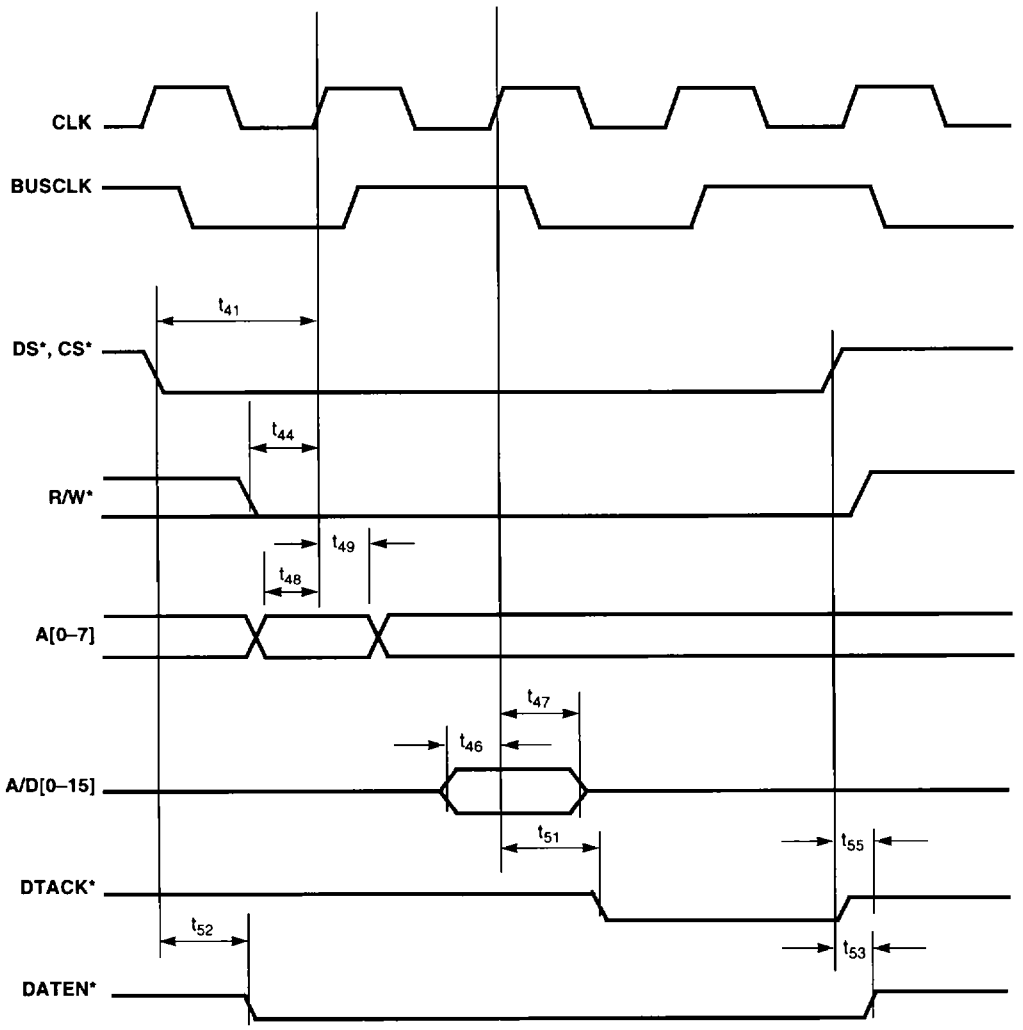


Figure 7-2. Slave Write Cycle Timing

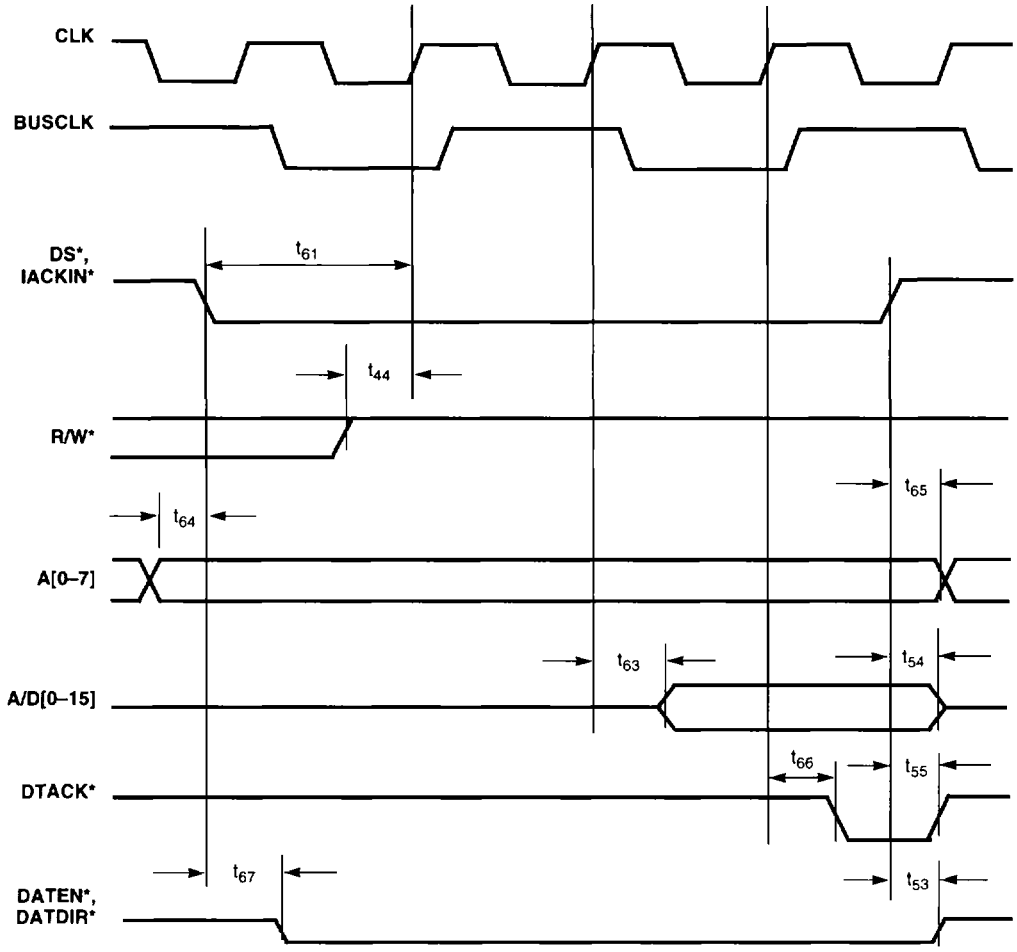
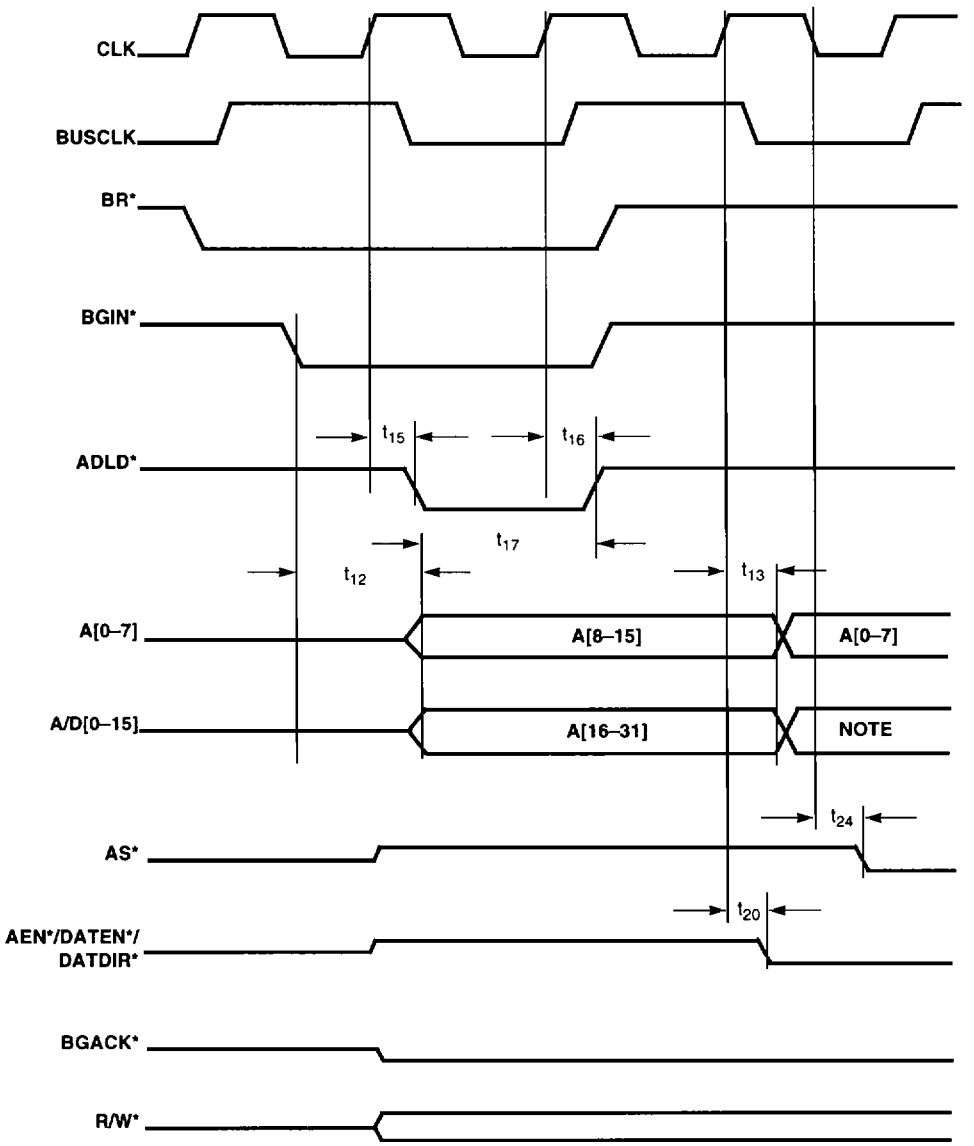


Figure 7-3. Interrupt Acknowledge Cycle Timing



NOTE: In DMA Read Cycle, these pins will be tristated.
In DMA Write Cycle, these pins will be D[0–15].

Figure 7-4. Bus Arbitration Cycle Timing

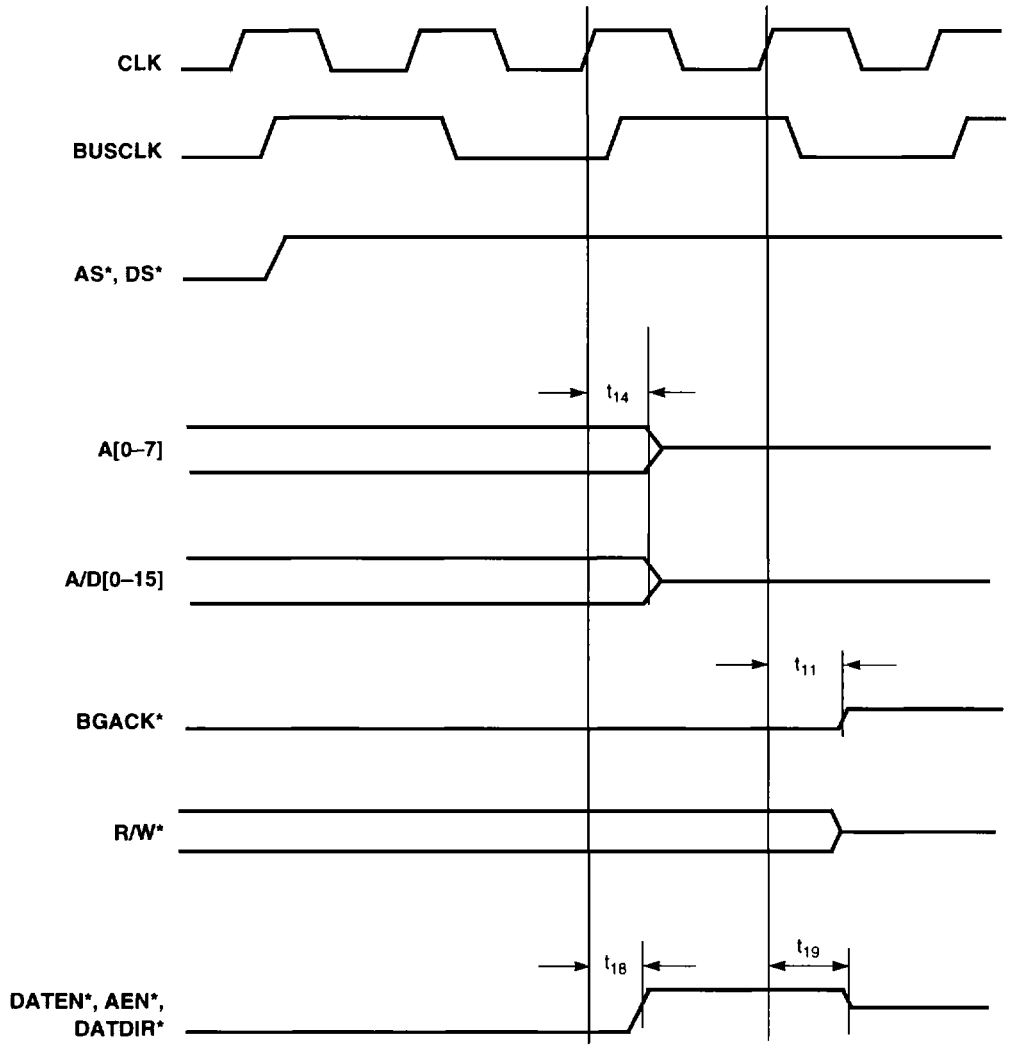


Figure 7-5. Bus Release Timing

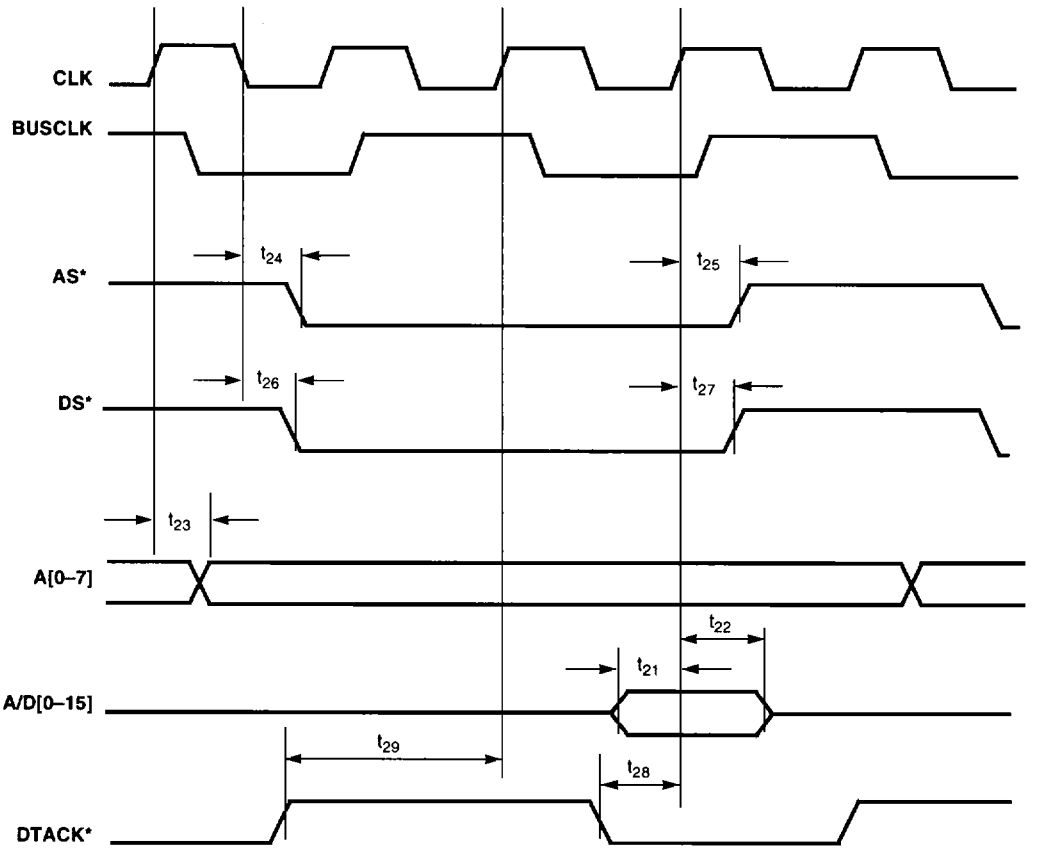


Figure 7-6. DMA Read Cycle Timing

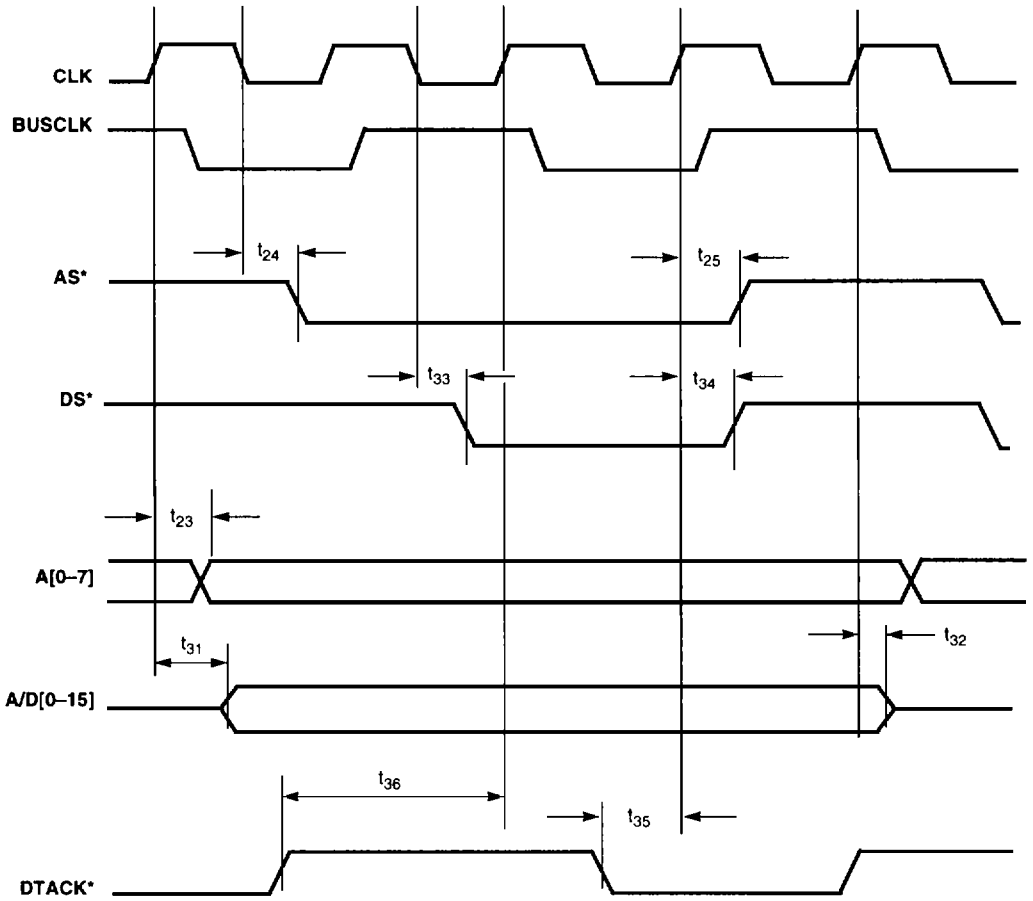


Figure 7-7. DMA Write Cycle Timing