Ordering number : ENA0677

SANYO Semiconductors
DATA SHEET

LB11993W

Monolithic Digital IC
For Digital Video Camera
Three-phase Brushless 3-in-1 Motor Driver

Overview

The LB11993W is a 3-phase brushless motor driver for digital video camera. It integrates, on a single chip, three motor driver functions (for capstan, drum, and loading motors) for driving a tape. This IC also includes 4-channel operation amplifiers (2 channels for reel and 2 channels for general purpose), which significantly reduces the number of peripheral components required.

Functions

- Capstan unit
  Voltage linear drive
  Built-in torque ripple compensation circuit
  FG amplifier
- Drum unit
  Current drive
  Sensorless drive
  FG amplifier
  PG amplifier
- Loading unit
  2-channel reel amplifiers
- Common unit
  Thermal shutdown circuit
  2-channel OP amplifiers

SANYO Semiconductor Co.,Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$ max		7	V
Supply voltage 2	$V_{CC}2$ max		9.0	V
Supply voltage 3	VS_C max	Capstan motor driver	7.0	V
Supply voltage 4	VS_D max	Drum motor driver	7.0	V
Supply voltage 5	VS_L max	Loading motor driver	7.0	V
Output voltage	V_O max		9.0	V
Input voltage	V_I1 max	Control system	-0.3 to V_{CC}1+0.3	V
	V_I2 max	U, V, W, COM	9.0	V
Capstan output current	IOC max		1.0	A
Drum output current	IOD max		1.0	A
Loading output current	IOL max		0.6	A
Internal power dissipation	Pd max	Independent IC	0.6	W
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

Recommended Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$	$V_{CC}1 \leq V_{CC}2$	2.7 to 6.0	V
Supply voltage 2	$V_{CC}2$		3.5 to 8.5	V
Supply voltage 3	VS_C	VS_C≤$V_{CC}2$	up to 6.5	V
Supply voltage 4	VS_D	VS_D≤$V_{CC}2$	up to 6.5	V
Supply voltage 5	VS_L	VS_L≤$V_{CC}2$	2.2 to 6.5	V
Hall input amplitude	VHALL	Capstan motor	±20 to ±80	mVp-p

Electrical Characteristics / Capstan motor driver block at Ta = 25°C, $V_{CC}1$=3V, $V_{CC}2$=4.75V, VS=1.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Supply currents]						
$V_{CC}1$ supply current	$I_{CC}1$	I_{OUT}=100mA VSTBY_C=3V		5.6	10	mA
$V_{CC}2$ supply current	$I_{CC}2$	I_{OUT}=100mA VSTBY_C=3V		6	12	mA
$V_{CC}1$ quiescent current	$I_{CC}1Q$	VSTBY_C=0V		3.3	5	mA
$V_{CC}2$ quiescent current	$I_{CC}2Q$	VSTBY_C=0V			100	μA
VS quiescent current	ISQ	VSTBY_C=0V		75	100	μA
[VX1]						
Upper-side residual voltage	VXH1	I_{OUT}=0.2A		0.22	0.28	V
Lower-side residual voltage	VXL1	I_{OUT}=0.2A		0.22	0.28	V
[VX2]						
Upper-side residual voltage	VXH2	I_{OUT}=0.5A		0.3	0.4	V
Lower-side residual voltage	VXL2	I_{OUT}=0.5A		0.3	0.4	V
Output saturation voltage	$V_O$sat	I_{OUT}=0.8A, Sink+Source			1.3	V
Amount of overlap	O.L	R_L=39Ω*3, Rangle=20kΩ, Note 2	70	80	90	%
[Hall amplifier]						
Input offset voltage	VHOFF	Design target value*	-5		+5	mV
Common-mode input range	VHCM	Rangle=20kΩ	0.95		2.1	V
Input/output voltage gain	VGVH	Rangle=20kΩ	25	27.5	30.5	dB
[Standby pin]						
High-level voltage	VSTH		2.5		$V_{CC}1$	V
Low-level voltage	VSTL		-0.2		0.7	V
Input current	ISTIN	VSTBY_C=3V			50	μA
Leakage current	ISTLK	VSTBY_C=0V	-30			μA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FRC pin]						
High-level voltage	VFRCH		2.5		$V_{CC}1$	V
Low-level voltage	VFRCL		-0.2		0.4	V
Input current	IFRCIN	VFRC_C=3V		20	40	μA
Leakage current	IFRCLK	VFRC_C=0V			-30	μA
[VH]						
Hall supply voltage	VHALL	I_H=5mA, VH(+)-VH(-)	0.83	0.93	1.03	V
Minus (-) pin voltage	VH(-)	I_H=5mA	0.90	0.97	1.04	V
[FG comparator]						
Input offset voltage	VFGOFF		-3		+3	mV
Input bias current	IbFG	VFGIN+=VFGIN-=1.5V			500	nA
Input bias current offset	ΔIbFG	VFGIN+=VFGIN-=1.5V	-100		100	nA
Common-mode input range	VFGCM		1.2		2.5	V
High-level output voltage	VFGOH	When internally pulled up	2.8			V
Low-level output voltage	VFGOL	When internally pulled up			0.2	V
Voltage gain	VGFG	Design target value, Note 1		100		dB
Output current (sink)	IFGOs	Output pin set to low			5	mA

Note 1: Design target value parameters are not tested.
Note 2: The standard for the overlap amount parameter is to report the measured value without change.

Cylinder Motor Driver Block at Ta=25°C, $V_{CC}1$=3V, $V_{CC}2$=4.75V, VS=3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 4	$I_{CC}2$	I_O=76mA, VSTBY_D=3V VSTBY_C=0V		0.75	2.5	mA
Output quiescent current 4	$I_{CC}2Q$	VSTBY_D=VSTBY_C=0V			100	μA
Output quiescent current 5	IS(D)Q	VSTBY_D=VSTBY_C=0V		100	300	μA
Output saturation voltage upper side 1	VOU1	I_O=0.1A, RF=0.25Ω		0.2	0.4	V
Output saturation voltage lower side 1	VOD1	I_O=0.1A, RF=0.25Ω		0.2	0.4	V
Output saturation voltage upper side 2	VOU2	I_O=0.4A, VS=3V, RF=0.25Ω		0.3	0.6	V
Output saturation voltage lower side 2	VOD2	I_O=0.4A, VS=3V, RF=0.25Ω		0.3	0.6	V
COM pin common-mode input voltage range	VIC		0.3		$V_{CC}2$-0.9	V
Standby pin high-level voltage	VSTBYH		2		$V_{CC}1$	V
Standby pin low-level voltage	VSTBYL		-0.2		0.7	V
Standby pin input current	ISTBYH	VSTBY_D=3V			50	μA
Standby pin leakage current	ISTBYL	VSTBY_D=0V	-10			μA
FRC pin high-level voltage	VFRCH		2		$V_{CC}1$	V
FRC pin low-level voltage	VFRCL		-0.2		0.7	V
FRC pin input current	IFRCI	VFRC_D=3V			50	μA
FRC pin leakage current	IFRCL	VFRC_D=0V	-10			μA
Slope pin source current ratio	RSOURCE	ICSLP1SOURCE/ICSLP2SOURCE	-20		20	%
Slope pin sink current ratio	RSINK	ICSLP1SINK/ICSLP2SINK	-20		20	%
CSLP1 source-to-sink current ratio	RCSLP1	ICSLP1SOURCE/ICSLP1SINK	-35		15	%
CSLP2 source-to-sink current ratio	RCSLP2	ICSLP2SOURCE/ICSLP2SINK	-35		15	%
Startup frequency	Freq	Cosc=0.1μF, OSC frequency Design target value, Note 1		11.5		Hz
Phase delay width	Dwidth	Design target value, Note 1		30		deg

Note 1: Design target value parameters are not tested.

FG and PG Amplifier Blocks at Ta=25°C, $V_{CC}1$=3V, $V_{CC}2$=4.75V, VS=3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FG amplifier]						
Input offset voltage	VIO			±1	±5	mV
Input bias current	IBIN-				250	nA
Common-mode input voltage range	VICOM		1		2	V
Open loop gain	GVFG	f=1kHz		55		dB
Output ON voltage	V_{OL}	When I_O=10μA			0.4	V
Output OFF voltage	V_{OH}	When I_O=10μA	$V_{CC}1$-0.5			V
Schmitt amplifier hysteresis width	VSHIS			50		mV
Reference voltage	VREF		1.30	1.40	1.50	V
[PG amplifier]						
Input offset voltage	VIO			±1	±5	mV
Input bias current	IBIN-				250	nA
Common-mode input voltage range	VICOM		1		2	V
Open loop gain	GVPG	f=1kHz		55		dB
Output ON voltage	V_{OL}	When I_O=10μA			0.4	V
Output OFF voltage	V_{OH}	When I_O=10μA	$V_{CC}1$-0.5			V
Schmitt amplifier hysteresis width	VSHIS			50		mV

Loading Motor Driver Block at Ta=25°C, $V_{CC}1$=3V, $V_{CC}2$=4.75V, VS=3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
$V_{CC}1$ supply current 1	$I_{CC}11$	Standby mode VSTBY_C=VSTBY_D=0V		3.3	5	mA
$V_{CC}1$ supply current 2	$I_{CC}12$	Forward/reverse mode VSTBYC=VSTBY_D=0V		14	21	mA
$V_{CC}1$ supply current 3	$I_{CC}13$	Brake mode VSTBYC=VSTBY_D=0V		12	18	mA
$V_{CC}2$ supply current 1	$I_{CC}21$	Standby mode($V_{CC}1$=OPEN) VSTBY_C, D=0V			100	μA
$V_{CC}2$ supply current 2	$I_{CC}22$	Standby mode($V_{CC}1$=3.0V) VSTBY_C, D=0V			100	μA
$V_{CC}2$ supply current 3	$I_{CC}23$	Forward/reverse mode VSTBY_C, D=0V		23	35	mA
VS_L supply current	IVS_L	Standby mode VSTBY_C, D=0V			20	μA
[Logic inputs] (DEC1 and DEC2 pins)						
High-level input voltage	VINH	$V_{CC}1$=2.7 to 4.0V	2.0		$V_{CC}1$	V
High-level influx current	IINH	V_{IN}=3.0V		45	100	μA
Low-level input voltage	VINL	$V_{CC}1$=2.7 to 4.0V	-0.2		0.6	V
Low-level influx current	IINL	V_{IN}=0.6V		5	10	μA
[Loading motor driver]						
Output saturation voltage 1	VOH	I_O=200mA (upper and lower composition)		0.2	0.3	V
Output saturation voltage 2	VSHIS	I_O=400mA (upper and lower composition)		0.4	0.6	V
[OP-AMP1, OP-AMP2]						
Input offset voltage	VIO			±1	±5	mV
Input bias current	IB				1	μA
Common-mode input voltage range	VICM		1		2	V
Open loop gain	GV1		50	55		dB

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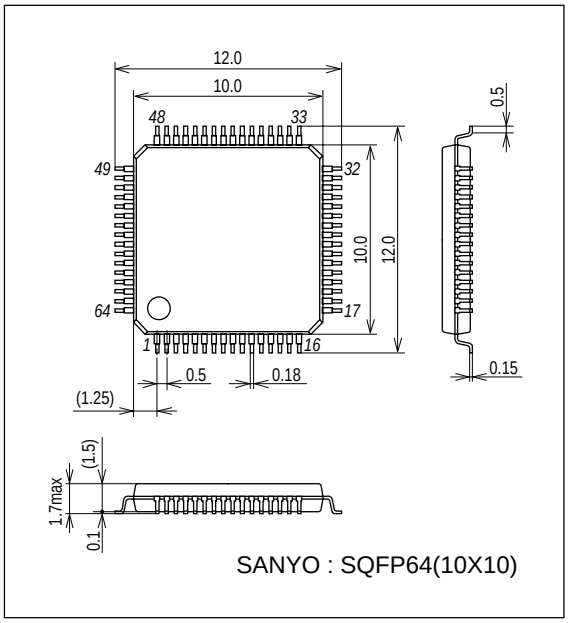
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[OP-AMP3, 4]						
Input offset voltage	VIO			±1	±5	mV
Input bias current	IB				1	μA
Common-mode input voltage range	VICM		1		2	V
Open loop gain	GV1		50	55		dB
[Thermal shutdown circuit]						
TSD operating temperature	T-TSD	Design target value, Note 1	150	180	210	°C
TSD temperature hysteresis width	ΔTSD	Design target value, Note 1		15		°C

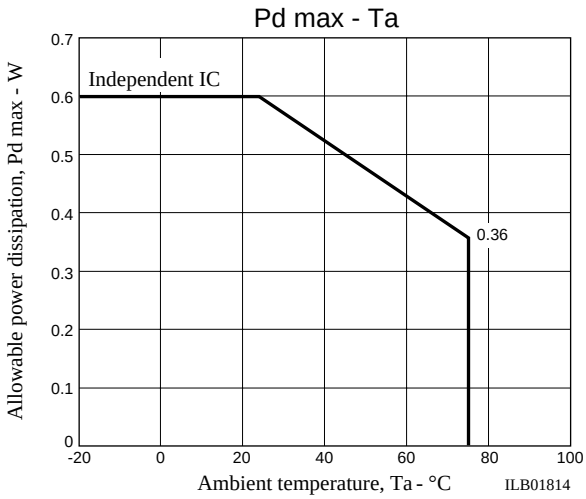
Note 1: Design target value parameters are not tested.

Package Dimensions

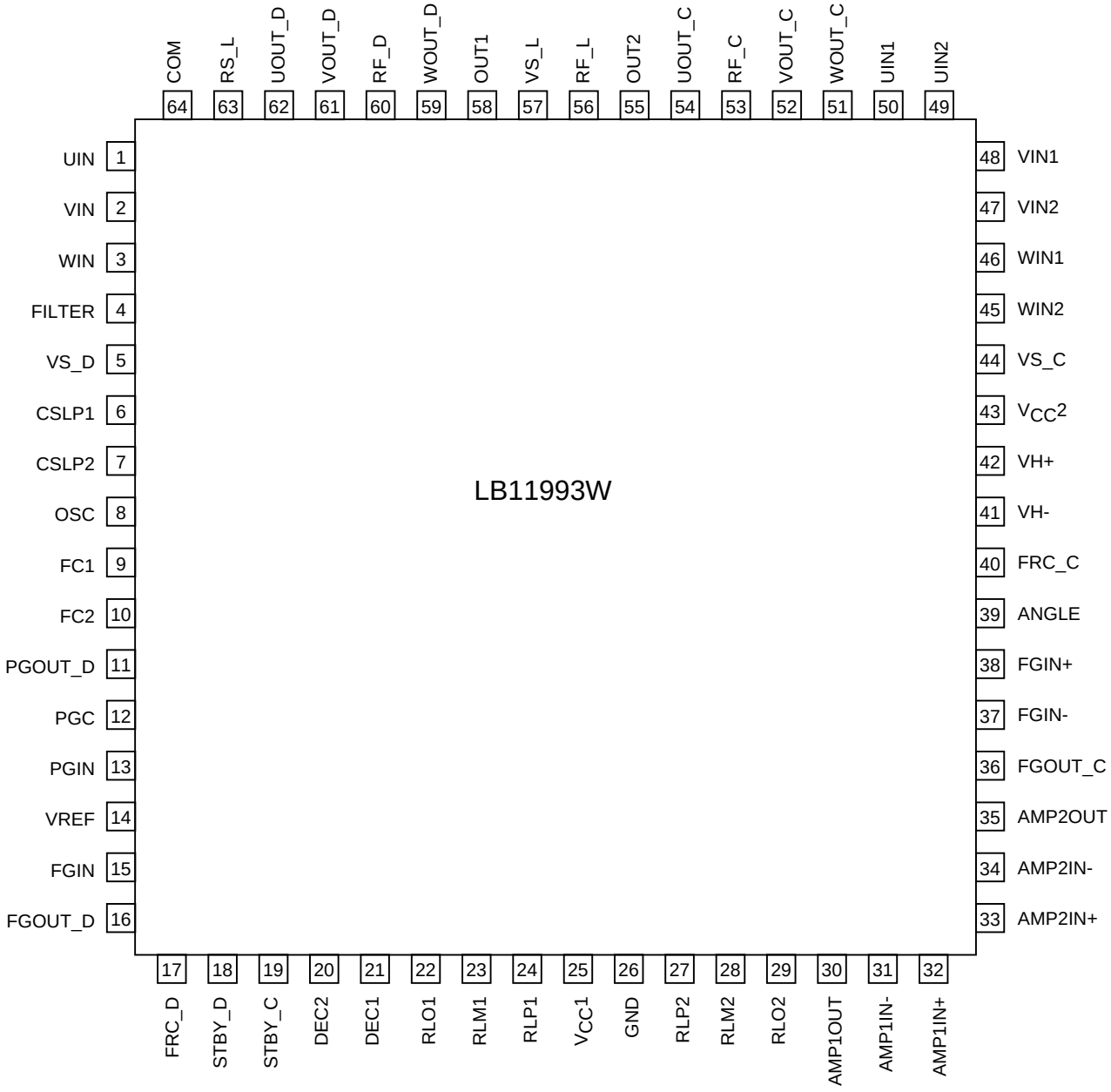
unit : mm (typ)

3190A





Pin Assignment



Top view

Truth Table

Capstan Motor Driver Truth Table

	Source → Sink	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

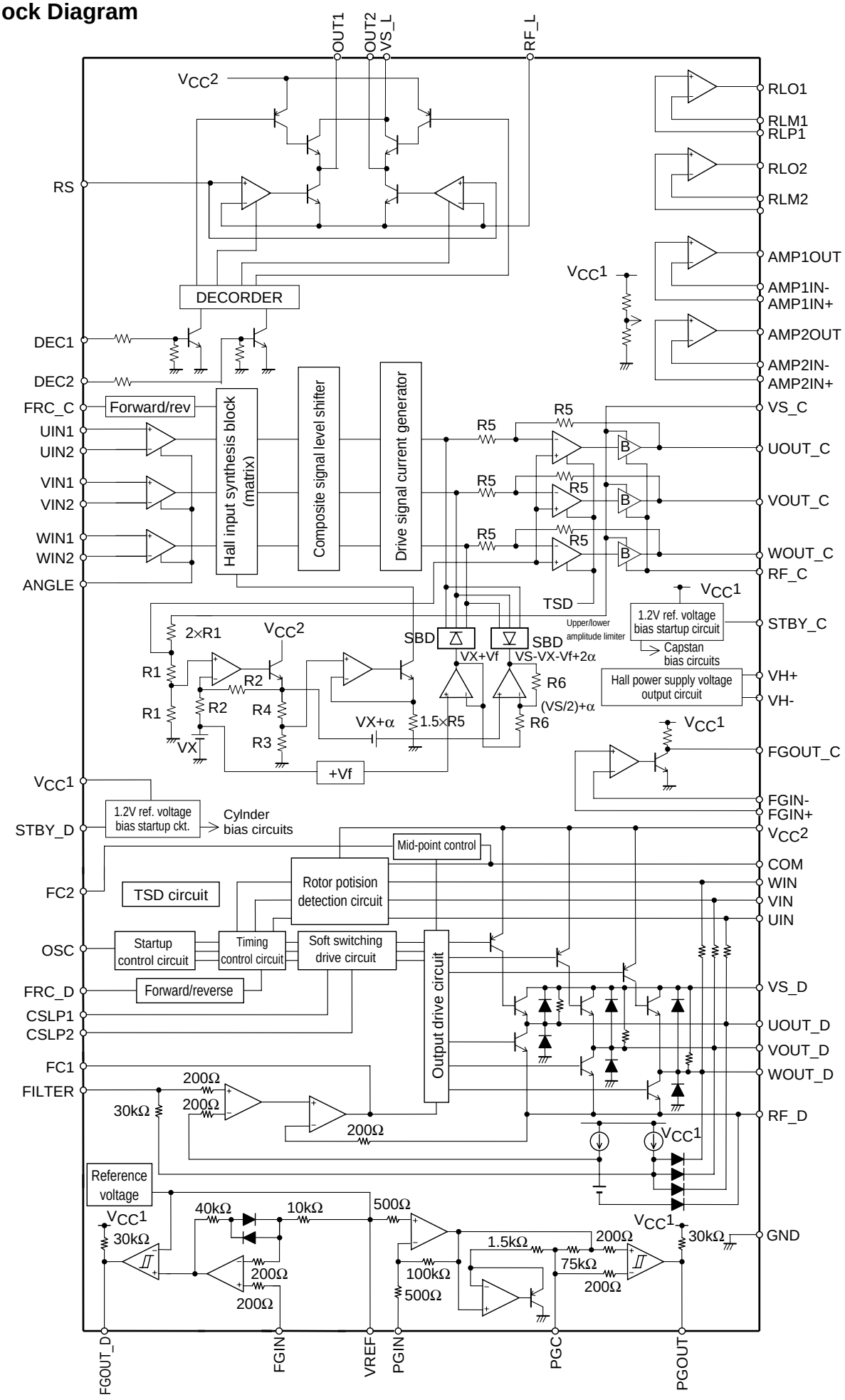
Note 1: H in the FR column means the voltage of 2.50V or more while L means the voltage of 0.4V or less. (at $V_{CC}1$=3V)

Note 2: For the Hall input, the input H means the condition in which (+) relative to each phase input (-) is higher by 0.02V or more.
The input L means the condition in which (+) relative to (-) is lower by 0.02V or more.

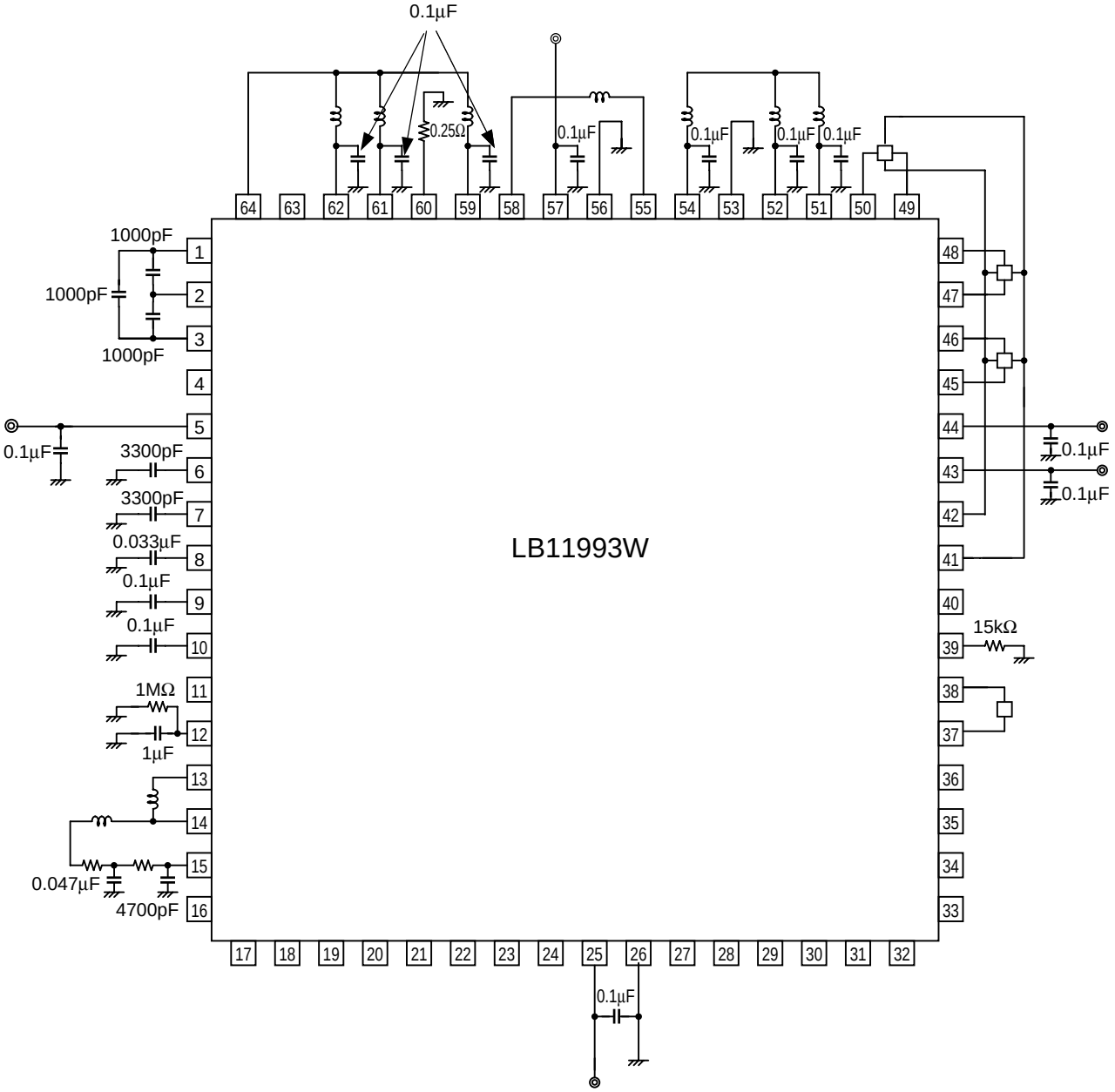
Loading Motor Driver Truth Table

Input		Output		Mode
DEC1	DEC2	OUT1	OUT2	
L	L	Off	Off	Standby
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake

Block Diagram

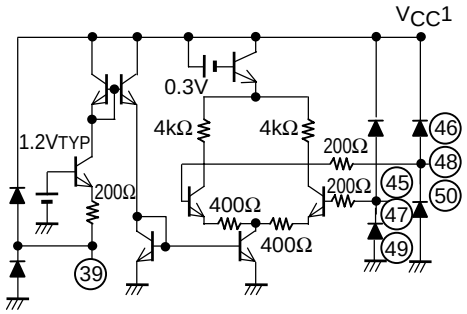
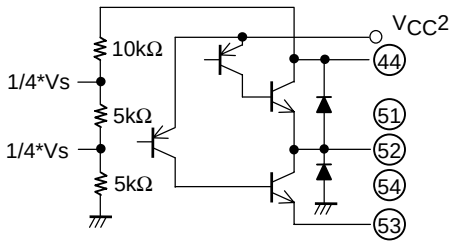
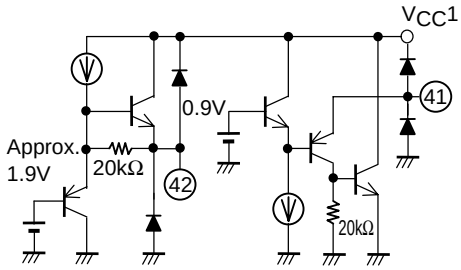
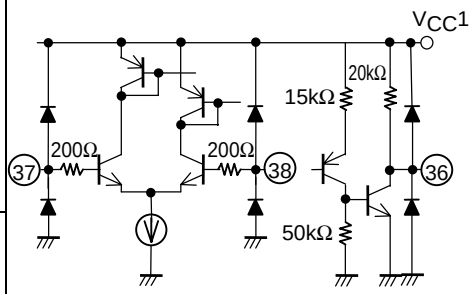
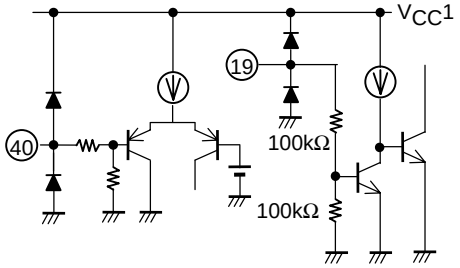


Sample Application Circuit



Note: The external constant is reference and may vary depending on the motor to be connected.

Pin Description

Pin No.	Symbol	Voltage	Equivalent Circuit Diagram	Description
50 49 48 47 46 45	UIN1 UIN2 VIN1 VIN2 WIN1 WIN2	0 to $V_{CC}1$		Capstan motor driver U, V, and W phase Hall element input/output. IN1 > IN2 state for logic H
39	ANGLE			Hall input/output gain control. Insertion of a resistor between this pin and ground controls the gain.
44	VS_C	0 to $V_{CC}2$		Power pin that determines the amplitude of the outputs to the capstan motor. The voltage applied to this pin must be lower than $V_{CC}2$.
54 52 51 53	UOUT_C VOUT_C WOUT_C Rf_C			Capstan motor driver U, V, and W phase output.
42	VH+			Hall element bias voltage supply. A voltage that is typically 0.85V is generated between the VH+ and VH- pins (when IH= 5mA).
41	VH-			
37	FGIN-	0 to $V_{CC}1$		FG comparator inverting input. There is no internally applied bias.
38	FGIN+			FG comparator noninverting input. There is no internally applied bias.
36	FGOUT_C			FG comparator output. There is an internal 20kΩ resistor load.
40	FRC_C	0 to $V_{CC}1$		Capstan forward/reverse select pin. The voltage on this pin selects forward or reverse rotation. (with hysteresis)
19	STBY_C			Pin to select bias supply to capstan circuits other than FG comparator. Setting this pin to low cuts-off the bias supply. Capstan motor standby pin.

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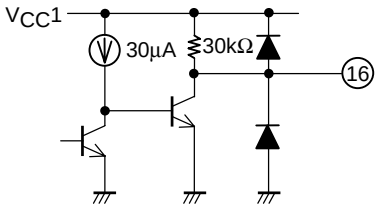
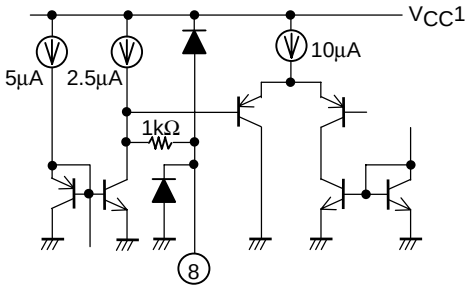
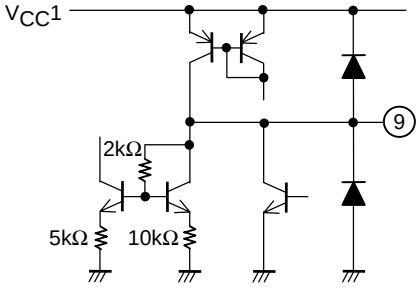
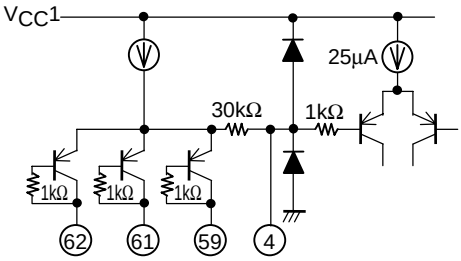
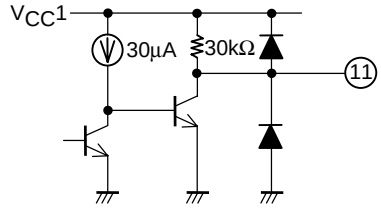
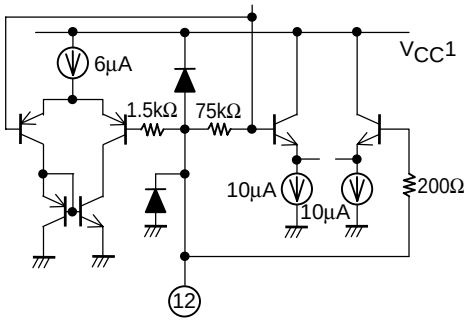
Pin No.	Symbol	Voltage	Equivalent Circuit Diagram	Description
16	FGOUT_D			FG amplifier output.
8	OSC			Pin for connecting triangular wave oscillator capacitor. Serves for forced startup waveform generation.
9	FC1			Frequency characteristics. Connecting a capacitor between this pin and ground serves to prevent closed-loop oscillation in the current control circuitry.
4	FILTER			Connecting a capacitor between this pin and ground activates the coil output saturation prevention function. In this condition, the VS pin is controlled for motor voltage control. By adjusting the external capacitor, torque ripple compensation can be varied.
11	PGOUT_D			PG amplifier output.
12	PGC			PG amplifier peak hold capacitor connection.

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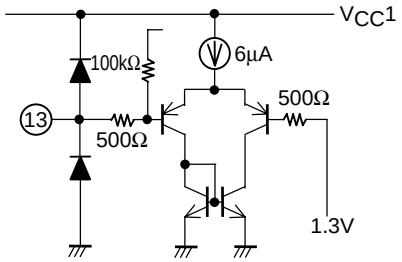
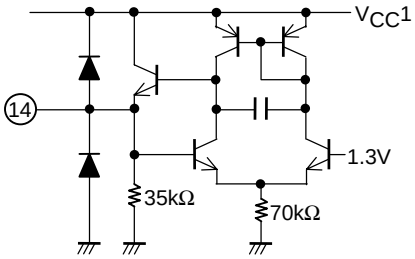
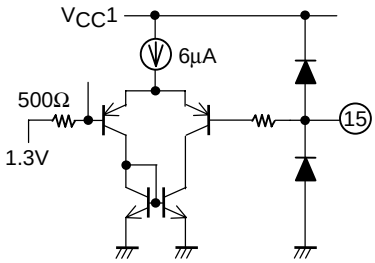
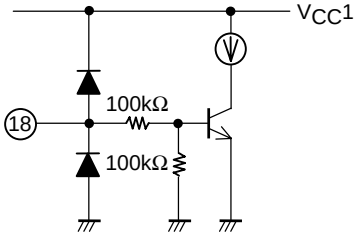
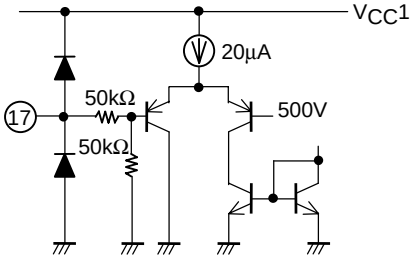
Pin No.	Symbol	Voltage	Equivalent Circuit Diagram	Description
13	PGIN	max2.0V min1.0V (when V_{CC}=3V)		PG amplifier input. Connect PG coil between this pin and VREF.
14	VREF			Internal 1.3V reference voltage. Used as reference voltage for FG and PG amplifiers.
15	FGIN_D	max2.0V min1.0V (when V_{CC}1=3V)		FG amplifier input. Connect FG coil between this pin and VREF.
18	STBY_D	0 to V_{CC}1		When this pin is at 0.7V or lower or when it is open, only the FG/PG amplifier operates. In the motor drive state, the pin should be at 2V or higher. Drum motor standby pin.
17	FRC_D	0 to V_{CC}1		Drum motor forward/reverse rotation select pin. Low: forward (-0.2V to 0.7V or open) High: reverse (2V to V_{CC}1)
5	VS_D	0V to V_{CC}2		Power supply for determining output amplitude by supplying drum motor voltage. Must be lower than V_{CC}2 voltage.

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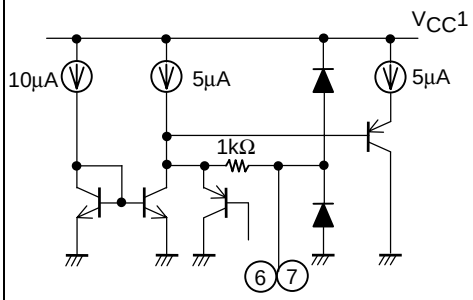
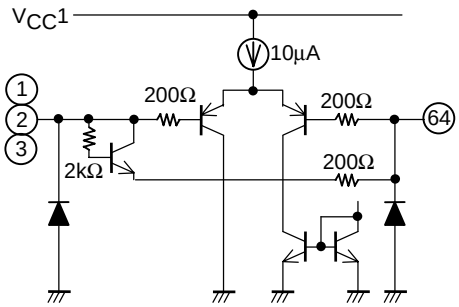
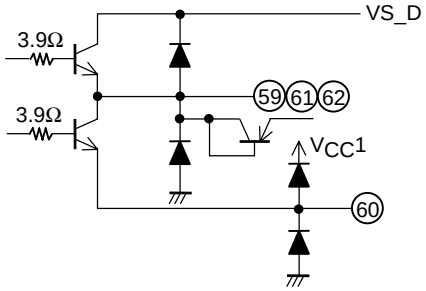
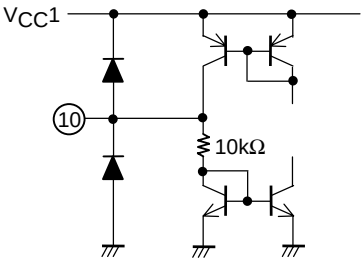
Pin No.	Symbol	Voltage	Equivalent Circuit Diagram	Description
43	$V_{CC}2$	3.5V to 6V		Power supply for supplying source side predriver voltage and coil waveform detect comparator voltage. Common for loading, capstan, and drum motors.
25	$V_{CC}1$	2.7V to 6V		Power supply for circuits except motor voltage, source side predriver voltage, and coil waveform detect comparator voltage. Common for loading, capstan, and drum motors.
6 7	CSLP1 CSLP2			Connection for the triangular wave generator. The coil output waveform is made to operate in a soft switching manner by this triangular wave.
26	GND			Ground for all circuits except output.
3 2 1	WIN UIN VIN			Coil waveform detect comparator input.
64	COM			Motor coil midpoint input. Using this voltage as a reference, the coil voltage waveform is detected.
59 62 61	WOUT_D UOUT_D VOUT_D			U, V, and W phase coil output.
60	RF_D			Drum motor driver output. transistor ground. Constant current drive is performed by detecting the voltage at this pin.
10	FC2			Output midpoint control. Connection for oscillation prevention capacitor.

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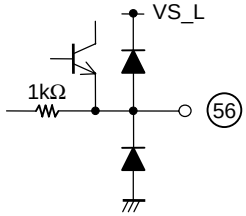
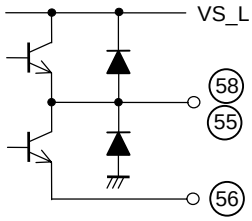
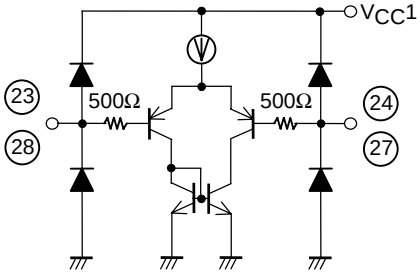
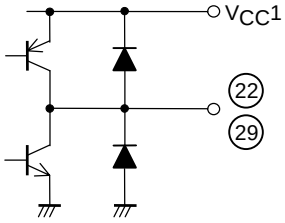
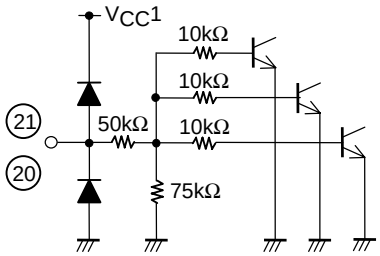
Pin No.	Symbol	Voltage	Equivalent Circuit Diagram	Description
57	VS_L	2.2 to $V_{CC}2$		Loading motor power supply. Stabilize against noise in the same way as for $V_{CC}2$.
56	RF_L			Output transistor P ground. Output current can be detected for motor current control by inserting a resistor between Rf pin and ground.
58 55	OUT1 OUT2			Loading motor driver output. Connect to loading motor.
23 24 28 27	RLM1 RLP1 RLM2 RLP2	0.2V to $V_{CC}1$-1V		L–FG amplifier input. RLM1 and RLM2 are negative input. RLP1 and RLP2 are positive input.
22 29	RLO1 RLO2			R-FG amplifier output.
21 20	DEC1 DEC2	0 to $V_{CC}1$		Loading motor input. When $V_{CC}1$ = 3.0V 2.0V or higher: High 0.6V or lower: Low

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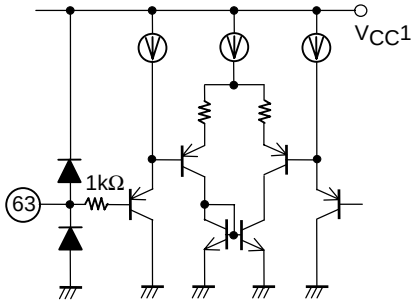
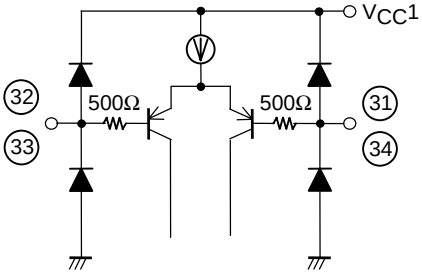
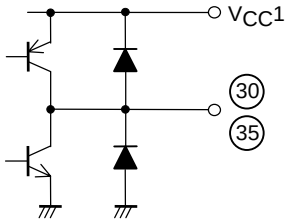
Pin No.	Symbol	Voltage	Equivalent Circuit Diagram	Description
63	RS_L	0 to $V_{CC}1$ -1.5V		Current limiter setting. Set voltage between RF pin and ground, for limiting current.
31 32 34 33	AMP1IN- AMP1IN+ AMP2IN- AMP2IN+	0.2V to ($V_{CC}1$-1)V		OP amplifier input. AMP1IN+ and AMP2IN+ are non-inverting input. AMP1IN- and AMP2IN- are inverting input.
30 35	AMP1OUT AMP2OUT			OP amplifier output.