System Reset
Monolithic IC PST574

Outline

This IC functions in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted. This ultra-low current consumption low reset type system reset IC has a built-in fixed delay time generating circuit. It is ideal for use in multi-CPU systems because a fast-rising output waveform can be obtained.

Features

1. Ultra-low current consumption	I_{CCH}=7.5μA typ. I_{CCL}=400μA typ.
2. Low operating limit voltage	0.65V typ.
3. Output current high for ON	30mA typ.
4. Hysteresis voltage provided in detection voltage	50mV typ.
5. Built-in delay circuit with excellent delay time temperature characteristics	50mV typ.
6. 10 ranks of detection voltage	PST574 C : 4.5V typ. H : 3.1V typ. D : 4.2V typ. I : 2.9V typ. E : 3.9V typ. J : 2.7V typ. F : 3.6V typ. K : 2.5V typ. G : 3.3V typ. L : 2.3V typ.

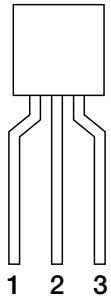
Package

MMP-3A (PST574□M)
TO-92A (PST574□)
*□contains detection voltage rank.

Applications

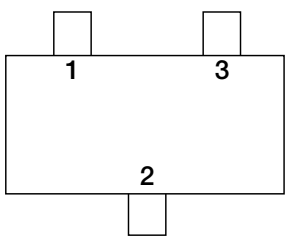
1. Reset circuits in microcomputers, CPUs and MPUs (especially multi-CPU sets)
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.

Pin Assignment



TO-92A

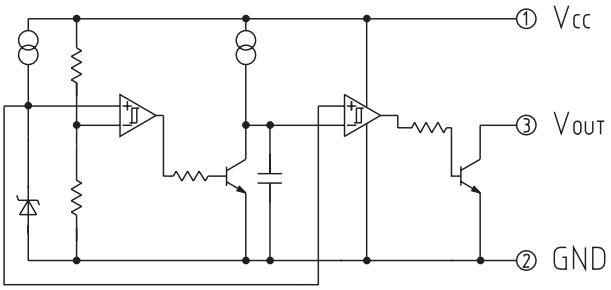
1	V_{CC}
2	GND
3	V_{OUT}



MMP-3A

1	V_{CC}
2	GND
3	V_{OUT}

Equivalent Circuit Diagram



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	Tstg	−40~+125	°C
Operating temperature	Topr	−20~+75	°C
Power supply voltage	Vcc max.	−0.3~10	V
Allowable loss	Pd	200 (MMP-3A) 300 (TO-92A)	mW

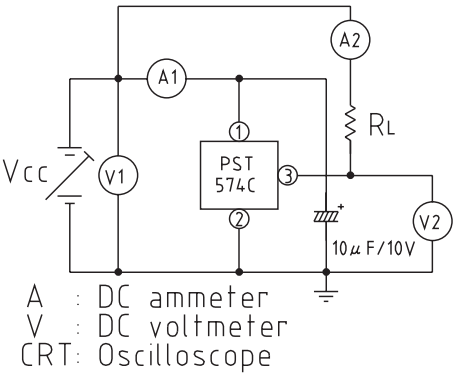
Electrical Characteristics (Ta=25°C) (Except where noted otherwise, resistance unit is Ω)

Item	Symbol	Measurement circuit	Measurement conditions		Min.	Typ.	Max.	Units
Detection voltage	Vs	1	RL=470 VOL≦0.4V Vcc=H→L	PST574C	4.3	4.5	4.7	V
				PST574D	4.0	4.2	4.4	
				PST574E	3.7	3.9	4.1	
				PST574F	3.4	3.6	3.8	
				PST574G	3.1	3.3	3.5	
				PST574H	2.9	3.1	3.3	
				PST574I	2.75	2.90	3.05	
				PST574J	2.55	2.70	2.85	
				PST574K	2.35	2.50	2.65	
				PST574L	2.15	2.30	2.45	
Hysteresis voltage	⊿Vs	1	RL=470, Vcc=L→H→L		25	50	100	mV
Detection voltage temperature coefficient	Vs/⊿T	1	RL=470, Ta=−20°C~+75°C			±0.01		%/°C
Low-level output voltage	VOL	1	Vcc=Vs min.−0.05V, RL=470			0.1	0.4	V
Output leakage current	IOH	1	Vcc=7.5V				±0.1	μA
Circuit current while on	ICCL	1	Vcc=Vs min.−0.05V, RL=∞			400	650	μA
Circuit current while off	ICCH	1	Vcc=Vs typ./0.85V, RL=∞			7.5	12.0	μA
"H"transport delay time	tpLH	2	✶1 RL=4.7kΩ, CL=100pF		250	400	600	μS
"L"transport delay time	tpHL	2	✶1 RL=4.7kΩ, CL=100pF			6	20	μS
Operation limit voltage	VopL	1	RL=4.7kΩ, VOL≦0.4V			0.65	0.85	V
Output current while on Ⅰ	IOL Ⅰ	1	Vcc=Vs min.−0.05V, RL=0		8	30		mA
Output current while on Ⅱ	IOL Ⅱ	1	✶2 Ta=−20°C~+75°C, RL=0		5			mA

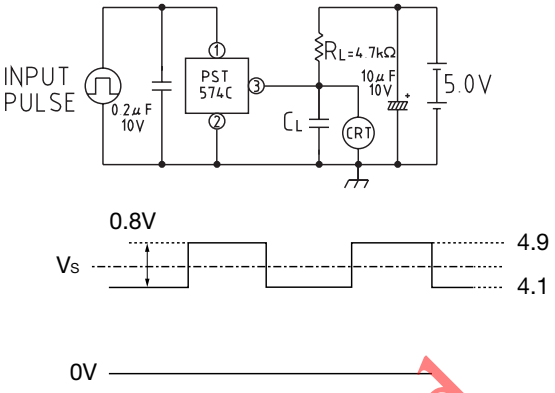
✶1 : tpLH : Vcc=(Vs typ.−0.4V)→(Vs typ.+0.4V), tpHL : Vcc=(Vs typ.+0.4V)→(Vs typ.-0.4V)
✶2 : Vcc=Vs min.−0.15V

Measuring Circuit

[1]



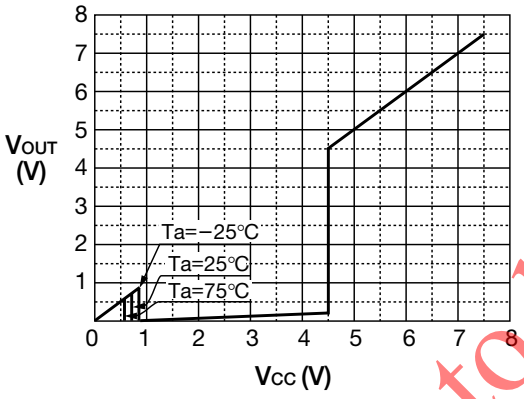
[2]



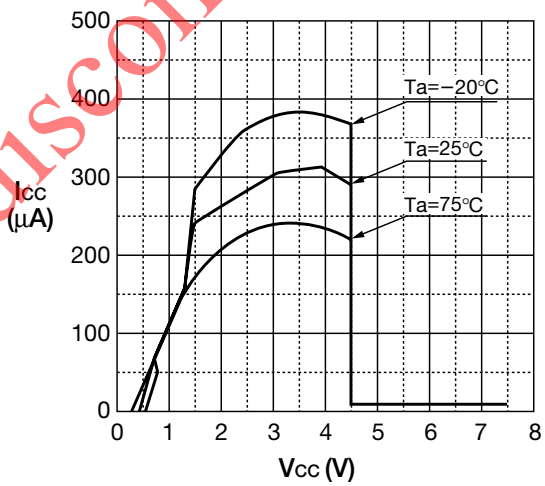
Note: Input model is an example for PST574C.

Characteristics (Example: PST574C)

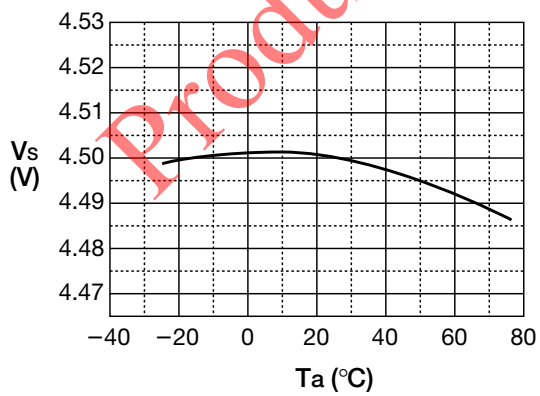
Vcc vs. VOUT



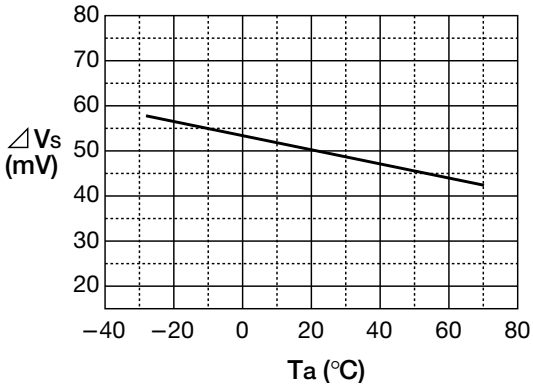
Vcc vs. Icc



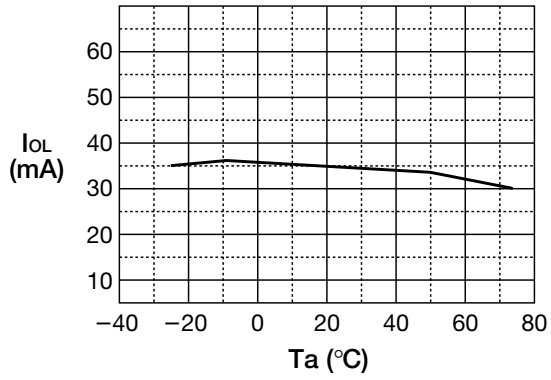
Vs vs. Ta



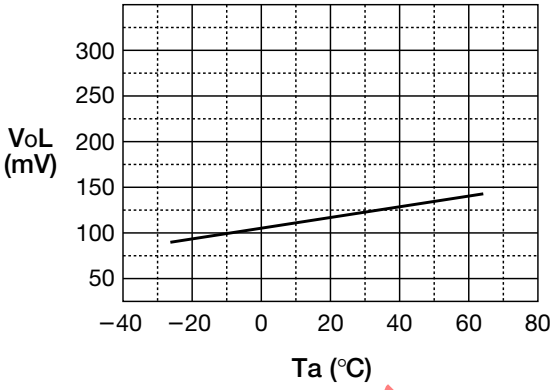
⊿Vs vs. Ta



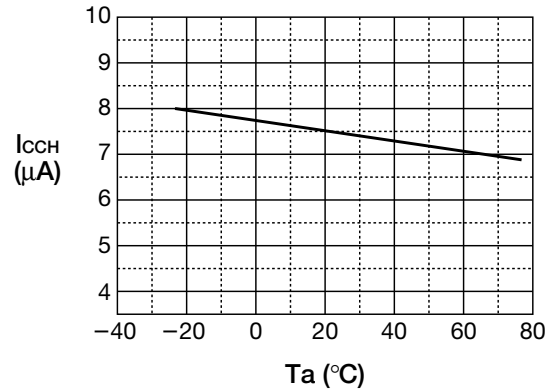
IoL vs. Ta



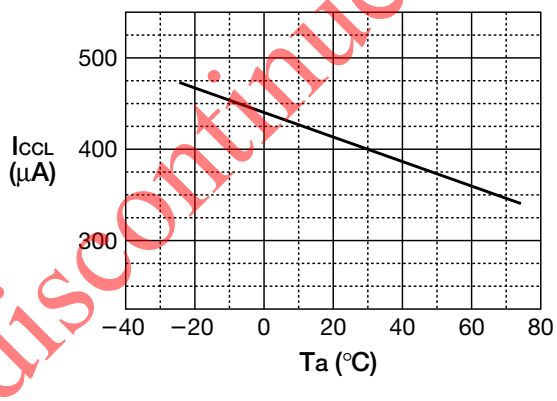
VoL vs. Ta



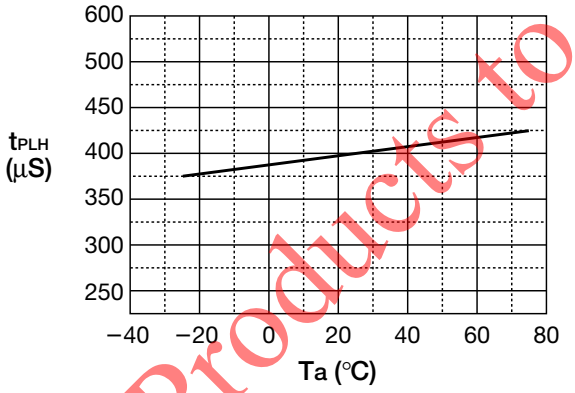
ICCH vs. Ta



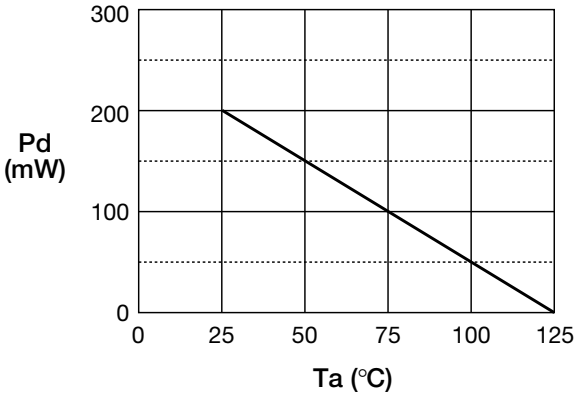
ICCL vs. Ta



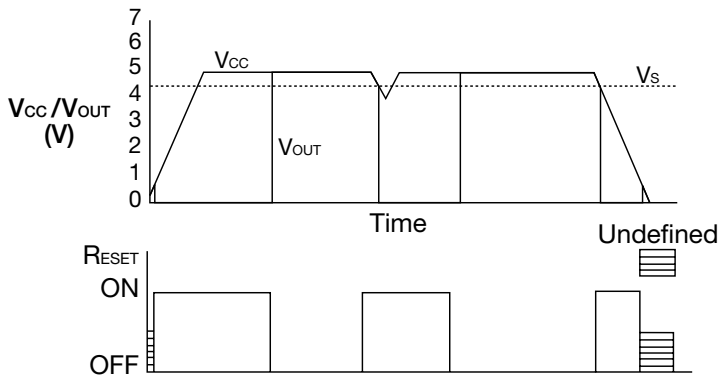
tPLH vs. Ta



Pd vs. Ta

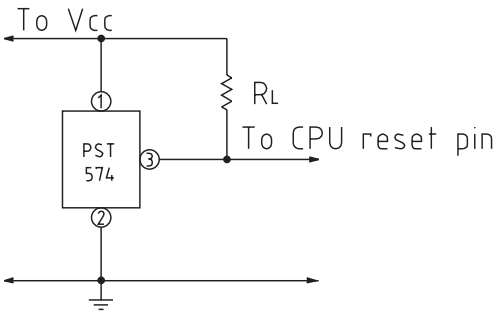


Timing Chart



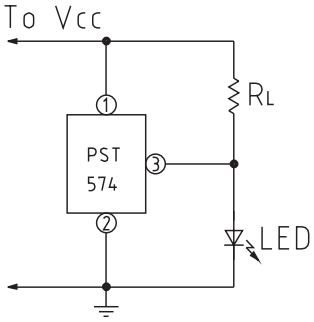
Application circuits

1. Normal hard reset



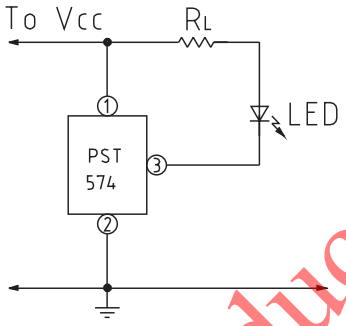
Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

2. Battery checker (LED ON for high voltage)



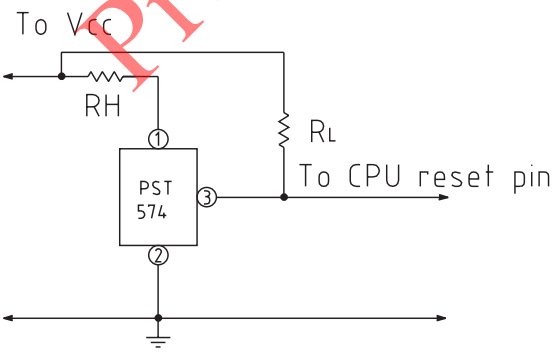
Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

3. Battery checker (LED ON for low voltage)



Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

4. Hysteresis voltage UP method



When increasing hysteresis voltage for stable system operation, determine RH as follows and connect externally.
However, I_{CCH} is −5000PPM/°C, so perform temperature compensation at RH when using over a wide temperature range.
Hysteresis voltage UP amount (ΔV_{sup}) is
$\Delta V_{sup} \fallingdotseq RH \times I_{CCL}$
Total hysteresis voltage (ΔV_{stotal}) is
$\Delta V_{stotal} \fallingdotseq V_s + \Delta V_{sup}$
(Operation will be destabilized if RH is raised too much.)

Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.