

MC14526B

Presettable 4-Bit Down Counters

The MC14526B binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

This device is presettable, cascadable, synchronous down counter with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

This complementary MOS counter can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Design: Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in} , V_{out}	-0.5 to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	I_{in} , I_{out}	± 10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Operating Temperature Range	T_A	-55 to +125	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$
Lead Temperature (8-Second Soldering)	T_L	260	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

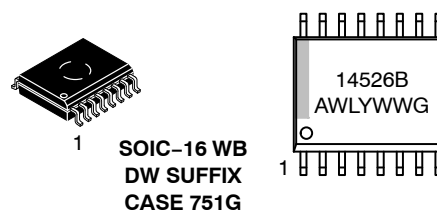
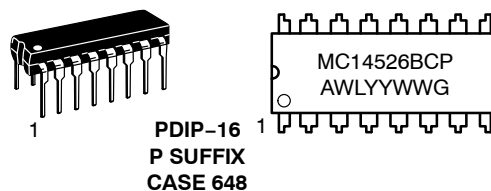
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

FUNCTION TABLE

Inputs					Output	Resulting Function
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	
X	H	X	L	L	L	Asynchronous reset*
X	H	X	H	L	H	Asynchronous reset
X	H	X	X	H	H	Asynchronous reset
X	L	X	H	X	L	Asynchronous preset
L	L	H	L	X	L	Decrement inhibited
			L	X	L	Decrement inhibited
H	L	L	L	L	L	No change** (inactive edge)
			L	L	L	No change** (inactive edge)
			L	L	L	Decrement**
			L	L	L	Decrement**

X = Don't Care

NOTES:

* Output "0" is low when reset goes high only if PE and CF are low.

** Output "0" is high when reset is low, only if CF is high and count is 0000.

PIN DESCRIPTIONS

Preset Enable (Pin 3) — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

Inhibit (Pin 4) — A high level on the Inhibit input prevents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

Clock (Pin 6) — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

Reset (Pin 10) — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the "0" output to go high.

"0" (Pin 12) — The "0" (Zero) output issues a pulse one clock period wide when the counter reaches terminal count (Q0 = Q1 = Q2 = Q3 = low) if Cascade Feedback is high and Preset Enable is low. When presetting the counter to a value

other than all zeroes, the "0" output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

Cascade Feedback (Pin 13) — If the Cascade Feedback input is high, a high level is generated at the "0" output when the count is all zeroes. If Cascade Feedback is low, the "0" output depends on the Preset Enable input level. See the Function Table.

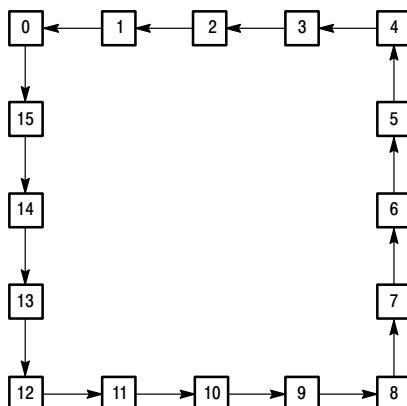
P0, P1, P2, P3 (Pins 5, 11, 14, 2) — These are the preset data inputs. P0 is the LSB.

Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1) — These are the synchronous counter outputs. Q0 is the LSB.

VSS (Pin 8) — The most negative power supply potential. This pin is usually ground.

VDD (Pin 16) — The most positive power supply potential. VDD may range from 3.0 to 18 V with respect to VSS.

STATE DIAGRAM
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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
	"1" Level	V _{IH}	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2	- - - -	-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8	- - - -	-1.7 -0.36 -0.9 -2.4	- - - -	mAdc
	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	
Input Current		I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)			5.0	-	5.0	-	0.005	5.0	-	150	μAdc
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)			5.0	I _T = (1.7 μA/kHz) f + I _{DD}							μAdc
			10	I _T = (3.4 μA/kHz) f + I _{DD}							
			15	I _T = (5.1 μA/kHz) f + I _{DD}							

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

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SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Note 5)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL} (Figures 4, 5)	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time (Inhibit Used as Negative Edge Clock) Clock or Inhibit to Q t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$ Clock or Inhibit to "0" t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 155 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	t_{PLH} , t_{PHL} (Figures 4, 5, 6)	5.0 10 15	- - -	550 225 160	1100 450 320	ns
Propagation Delay Time Pn to Q	t_{PLH} , t_{PHL} (Figures 4, 7)	5.0 10 15	- - -	260 120 100	520 240 200	ns
Propagation Delay Time Reset to Q	t_{PHL} (Figure 8)	5.0 10 15	- - -	250 110 80	500 220 160	ns
Propagation Delay Time Preset Enable to "0"	t_{PHL} , t_{PLH} (Figures 4, 9)	5.0 10 15	- - -	220 100 80	440 200 160	ns
Clock or Inhibit Pulse Width	t_w (Figures 5, 6)	5.0 10 15	250 100 80	125 50 40	- - -	ns
Clock Pulse Frequency (with PE = low)	f_{max} (Figures 4, 5, 6)	5.0 10 15	- - -	2.0 5.0 6.6	1.5 3.0 4.0	MHz
Clock or Inhibit Rise and Fall Time	t_r , t_f (Figures 5, 6)	5.0 10 15	- - -	- - -	15 5 4	μs
Setup Time Pn to Preset Enable	t_{su} (Figure 1)	5.0 10 15	90 50 40	40 15 10	- - -	ns
Hold Time Preset Enable to Pn	t_h (Figure 2)	5.0 10 15	30 30 30	-15 -5 0	- - -	ns
Preset Enable Pulse Width	t_w (Figure 3)	5.0 10 15	250 100 80	125 50 40	- - -	ns
Reset Pulse Width	t_w (Figure 8)	5.0 10 15	350 250 200	175 125 100	- - -	ns
Reset Removal Time	t_{rem} (Figure 8)	5.0 10 15	10 20 30	-110 -30 -20	- - -	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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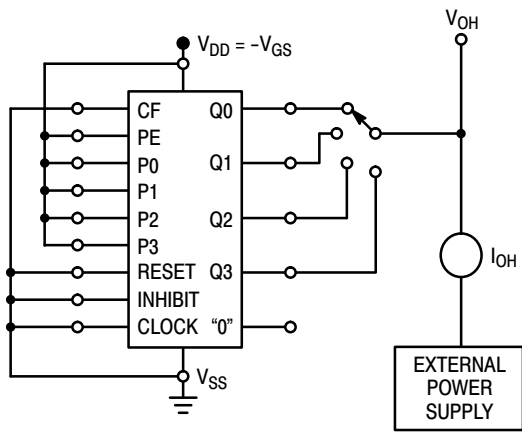


Figure 1. Typical Output Source Characteristics Test Circuit

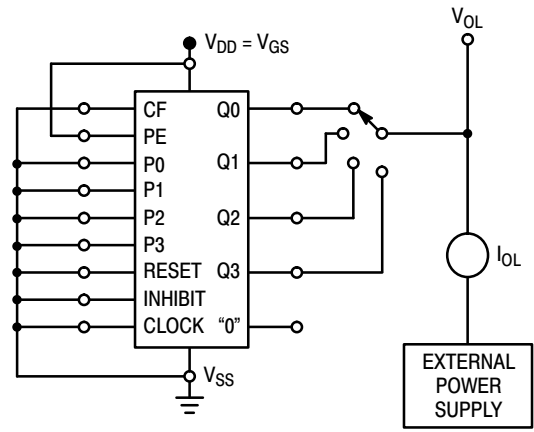


Figure 2. Typical Output Sink Characteristics Test Circuit

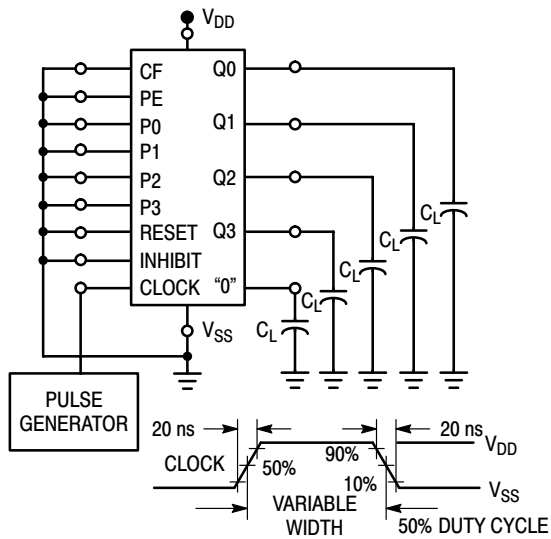
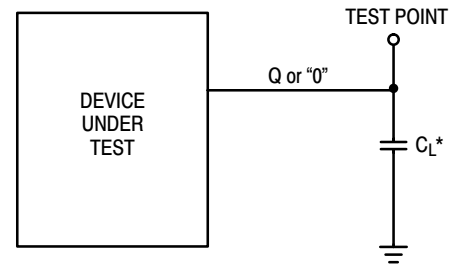


Figure 3. Power Dissipation



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

SWITCHING WAVEFORMS

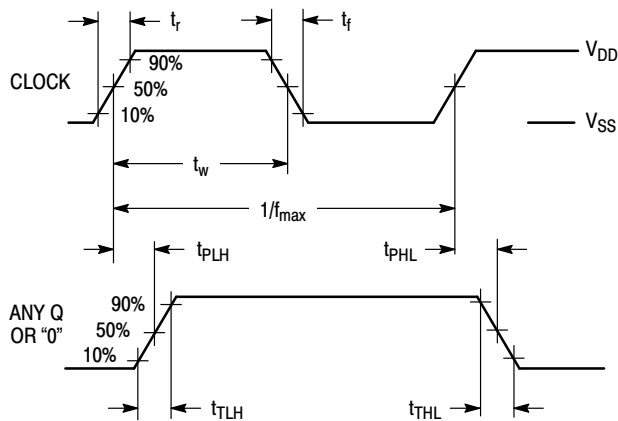


Figure 5.

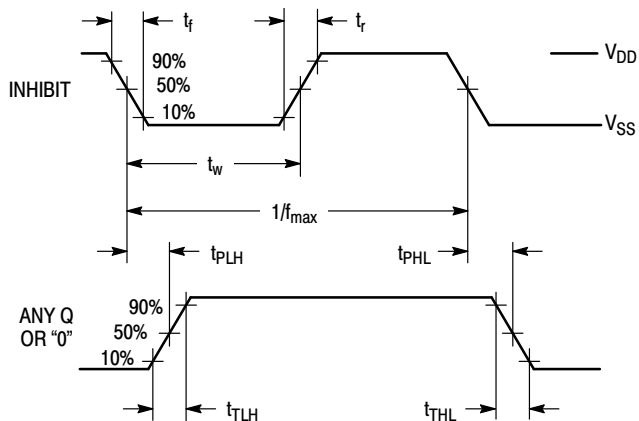


Figure 6.

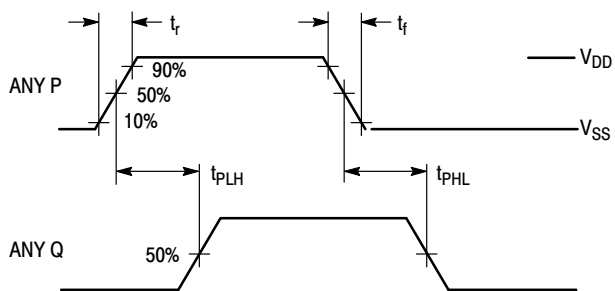


Figure 7.

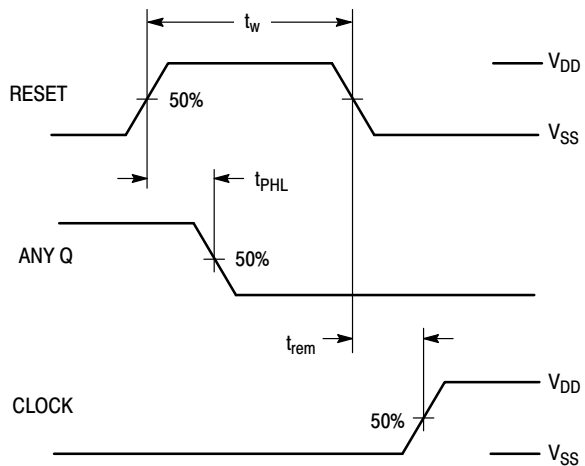


Figure 8.

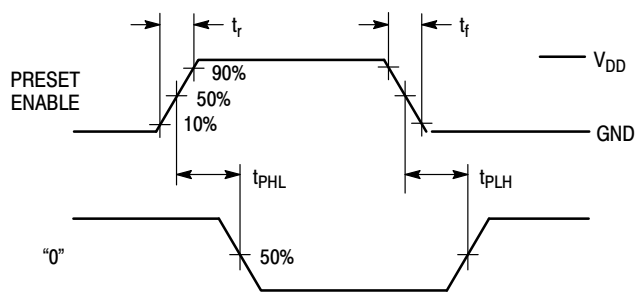


Figure 9.

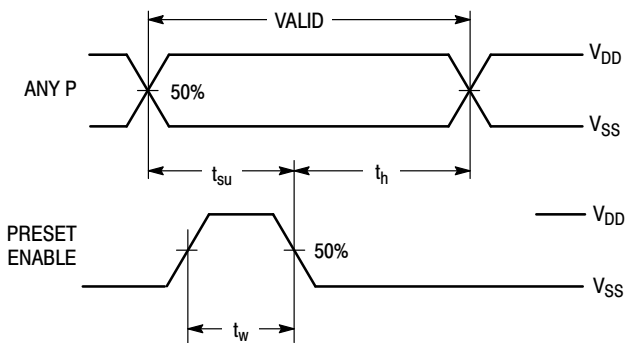


Figure 10.

MC14526B

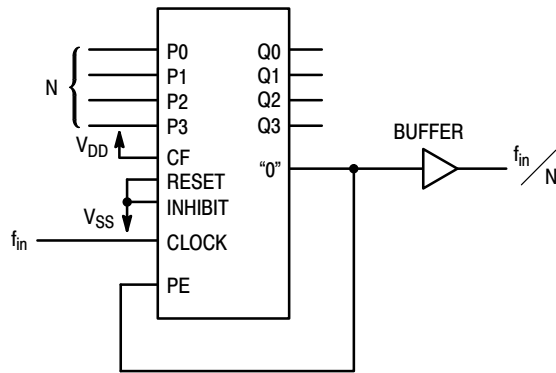


Figure 11. ÷ N Counter

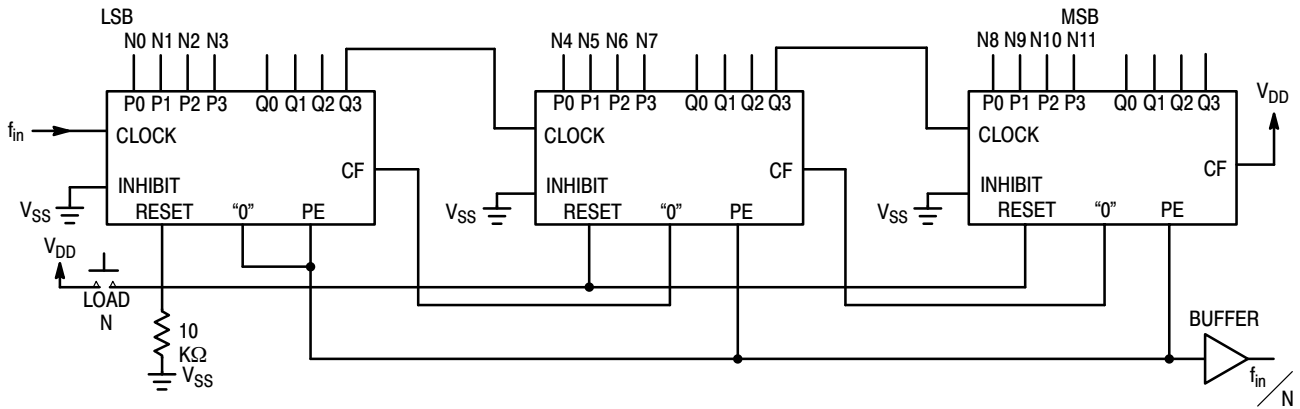


Figure 12. 3 Stages Cascaded

ORDERING INFORMATION

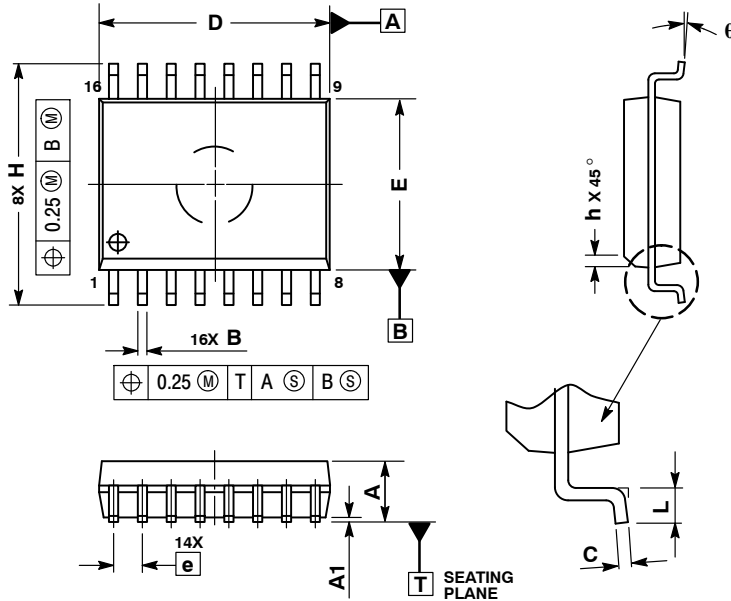
Device	Package	Shipping†
MC14526BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14526BDWG	SOIC-16 (Pb-Free)	47 Units / Rail
MC14526BDWR2G	SOIC-16 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14526B

PACKAGE DIMENSIONS

SOIC-16 WB
CASE 751G-03
ISSUE D

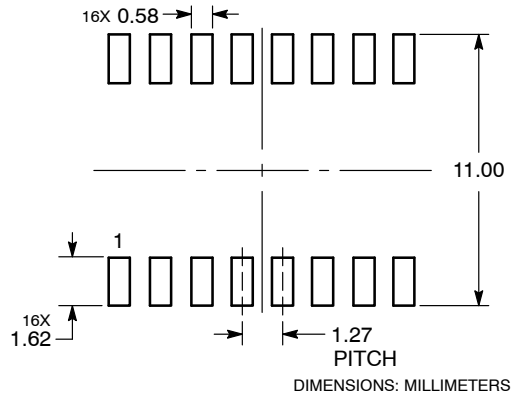


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °

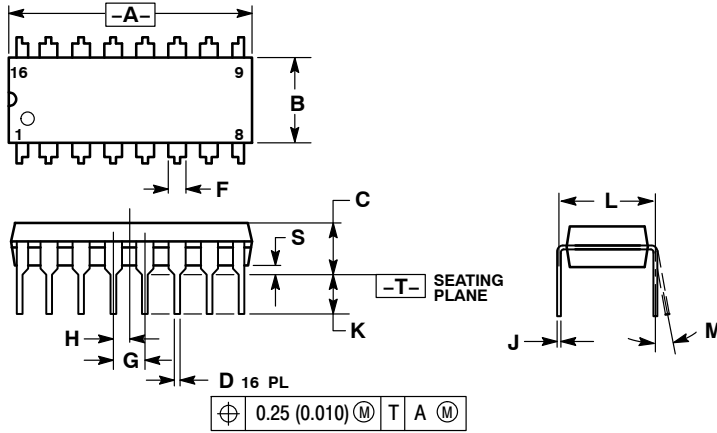
SOLDERING FOOTPRINT



MC14526B

PACKAGE DIMENSIONS

PDIP-16
CASE 648-08
ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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