ADC1443D series

Dual channel 14-bit ADC; 125, 160 or 200 Msps; JESD204B-compliant CGVxpress serial outputs

Rev. 3.4 — 10 October 2012 **Data sheet**

1. General description

The ADC1443D is a dual channel 14-bit Analog-to-Digital Converter (ADC) with JESD204B interface (which is backward compatible with the JESD204A interface) optimized for high dynamic performance and low power consumption at sample rates up to 200 Msps. Pipelined architecture and output error correction ensure that the ADC1443D is accurate enough to guarantee zero missing codes over the entire operating range.

Supplied from a single 1.8 V source, the ADC1443D has serial outputs compliant with the JESD204B standard over a configurable number of lanes (1 or 2). Multiple Device Synchronization (MDS) allows sample-accurate synchronization of the data outputs of multiple ADC devices. It guarantees a maximum skew of one clock period between as many as 16 output lanes from up to eight ADC1443D devices.

An integrated Serial Peripheral Interface (SPI) allows easy configuration of the ADC. The device also includes a programmable full-scale to allow a flexible input voltage range of 1 V (p-p) to 2 V (p-p).

With excellent dynamic performance from the baseband to input frequencies of up to 1 GHz (typical), the ADC1443D is ideal for use in undersampled multi-carrier, multistandard communication system applications. Using a pipelined architecture, an output error correction scheme ensures that the ADC1443D is accurate enough to guarantee zero missing codes over the entire operating range.

The ADC1443D is available in an HLQFN56 package (8 mm × 8 mm outline). It is supported with customer demo boards. This device is also available in a 12-bit resolution variant with a choice of maximum sampling frequency (125, 160 or 200 Msps).

2. Features and benefits

- Dual channel 14-bit resolution ADC
- Sampling rate up to 200 Msps
- JESD204B Device Subclass 0, 1 and 2 compliant with harmonic clocking and deterministic latency support
- ADC Multiple Device Synchronization (MDS)
- Assured interworking/interoperability with SerDes based FPGAs
- SNR = 70.6 dBFS (typical); f_s = 154 Msps; f_i = 190 MHz
- SFDR = 86 dBc (typical); f_s = 154 Msps; f_i = 190 MHz
- IMD3 = 88 dBc (typical); f_s = 154 Msps; f_{i1} = 188.5 MHz; f_{i2} = 191.5 MHz
- Analog input bandwidth of 1 GHz (typical)
- Pin to pin compatible with ADC1413D series

- Two JESD204B serial output lanes, up to 5 Gbps typical
- Single 1.8 V supply
- Flexible input voltage range from 1 V (p-p) to 2 V (p-p) by 1 dB steps
- Clock input divider from 1 to 8 supports harmonic clocking
- Duty Cycle Stabilizer (DCS)
- Offset binary, two's complement and Gray output data
- Typical power dissipation = 0.9 W; f_s = 154 Msps
- Power-down and sleep modes
- Industrial temperature range from –40 °C to +85 °C
- Serial Peripheral Interface (SPI) for configuration control and status monitoring
- HLQFN56 package; 8 × 8 mm

3. Applications

- Wireless infrastructure: LTE, TD-LTE, WiMAX, MC-GSM, CDMA, WCDMA, TD-SCDMA
- Software defined radio
- Medical non-invasive scanners
- Scientific particle detectors
- Microwave backhaul transceivers
- Aerospace and defense communications and radar systems
- Industrial signal analysis instruments
- General-purpose high-speed applications

4. Ordering information

Table 1. Ordering information

Type number	f_s (Msps)	Package		
		Name	Description	Version
ADC1443D200HD	200	HLQFN56	plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm	SOT935-2
ADC1443D160HD	160	HLQFN56	plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm	SOT935-2
ADC1443D125HD	125	HLQFN56	plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm	SOT935-2

5. Block diagram

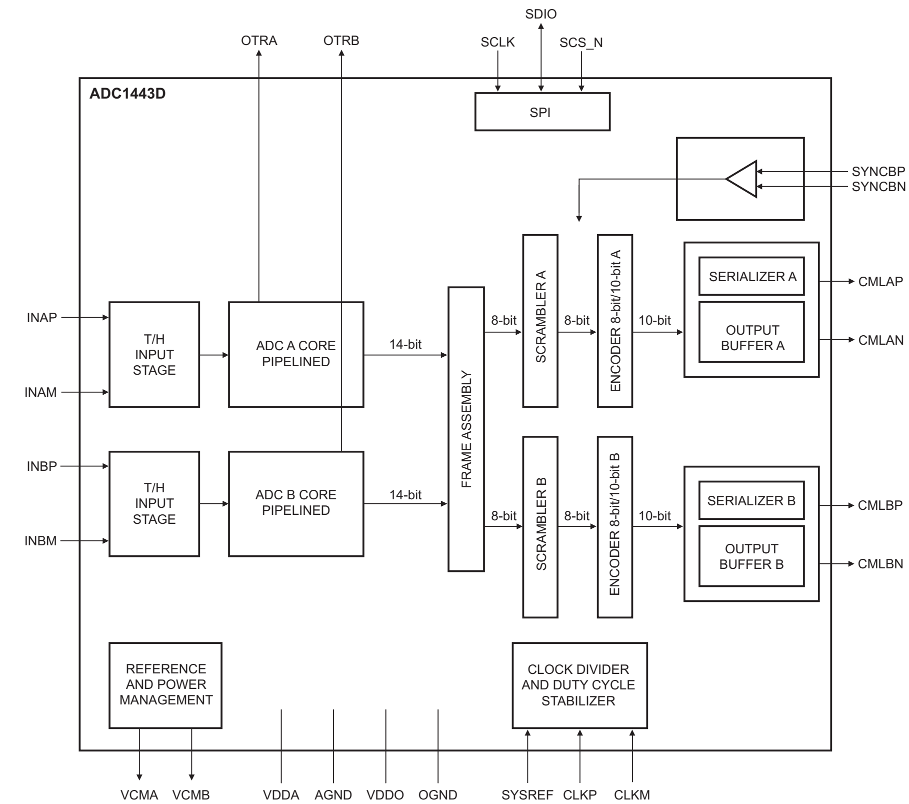


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

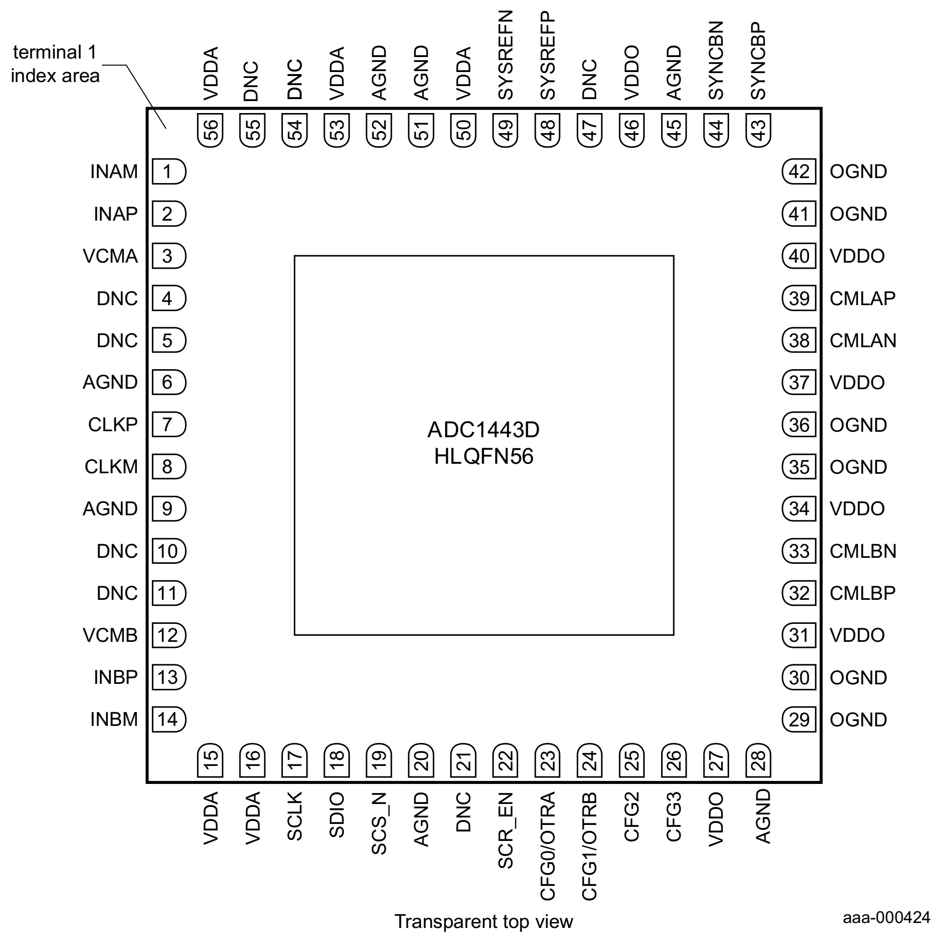


Fig 2. Pin configuration (SOT935-2)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
INAM	1	I	channel A complementary analog input
INAP	2	I	channel A analog input
VCMA	3	O	channel A output common voltage
DNC	4	-	do not connect
DNC	5	-	do not connect
AGND	6	G	analog ground
CLKP	7	I	clock input
CLKN	8	I	complementary clock input
AGND	9	G	analog ground
DNC	10	-	do not connect
DNC	11	-	do not connect
VCMB	12	O	channel B output common voltage
INBP	13	I	channel B analog input
INBM	14	I	channel B complementary analog input
VDDA	15	P	analog power supply
VDDA	16	P	analog power supply
SCLK	17	I	SPI clock
SDIO	18	I/O	SPI data IO
SCS_N	19	I	SPI chip select
AGND	20	G	analog ground
DNC	21	-	do not connect
SCR_EN	22	I	scrambler enable
CFG0/OTRA	23	I/O	configuration pin 0/OuT of Range A (OTRA)
CFG1/OTRB	24	I/O	configuration pin 1/OuT of Range B (OTRB)
CFG2	25	I/O	configuration pin 2
CFG3	26	I/O	configuration pin 3
VDDO	27	P	digital output power supply
AGND	28	G	analog ground
OGND	29	G	digital output ground
OGND	30	G	digital output ground
VDDO	31	P	digital output power supply
CMLBP	32	O	channel B output
CMLBN	33	O	channel B complementary output
VDDO	34	P	digital output power supply
OGND	35	G	digital output ground
OGND	36	G	digital output ground
VDDO	37	P	digital output power supply
CMLAN	38	O	channel A complementary output
CMLAP	39	O	channel A output

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
VDDO	40	P	digital output power supply
OGND	41	G	digital output ground
OGND	42	G	digital output ground
SYNCBP	43	I	JESD204B SYNC synchronization signal from receiver
SYNCBN	44	I	complementary SYNC from receiver
AGND	45	G	analog ground
VDDO	46	P	digital power
DNC	47	-	do not connect
SYSREFP	48	I	positive clock synchronization
SYSREFN	49	I	negative clock synchronization
VDDA	50	P	analog power supply
AGND	51	G	analog ground
AGND	52	G	analog ground
VDDA	53	P	analog power supply
DNC	54	-	do not connect
DNC	55	-	do not connect
VDDA	56	P	analog power supply
AGND	EXP	G	Expose PAD

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.3	+2.1	V
V_{DDO}	output supply voltage		–0.3	+2.1	V
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDO}$	–0.8	+0.8	V
V_I	input voltage	pins INP, INM, CLKP and CLKM; referenced to AGND	–0.3	V_{DDA} + 0.3	V
		pins OTR, SCS_N, SDIO, SCLK, CFG, SCR_EN, SYSREFP, SYSREFN, SYNCBP, and SYNCBN; referenced to AGND	–0.3	V_{DDO} + 0.3	V
V_O	output voltage	pin VCM; referenced to AGND	–0.3	V_{DDA} + 0.3	V
		pins CMLP, and CMLN; referenced to OGND	–0.3	V_{DDO} + 0.3	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	22.7	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	9.3	K/W

[1] In compliance with JEDEC test board, in free air.

9. Static characteristics

Table 5. Static characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		1.7	1.8	1.9	V
V_{DDO}	output supply voltage		1.7	1.8	1.9	V
I_{DDA}	analog supply current	f_s = 185 Msps; f_i = 190 MHz	-	410	<tbd>	mA
I_{DDO}	output supply current	f_s = 185 Msps; f_i = 190 MHz	-	173	<tbd>	mA

Table 5. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{tot}	total power dissipation	f_i = 190 MHz				
		ADC1443D125; f_s = 125 Msps	-	0.71	0.9	W
		ADC1443D160; f_s = 154 Msps	-	0.9	<tbd>	W
		ADC1443D200; f_s = 185 Msps	-	1.05	<tbd>	W
		Power-down mode	-	10	-	mW
		Sleep mode	-	115	-	mW
Clock inputs: pins CLKP and CLKM (AC-coupled; peak-to-peak)						
$V_{i(clk)}$	clock input voltage	LVPECL	-	±0.8	-	V
		LVDS	-	±0.35	-	V
		SINE differential	±0.5	±1.5	-	V
		LVCMOS single	-	V_{DDA}	-	V
C_I	input capacitance		-	1.2	-	pF
Logic inputs						
I_{IL}	LOW-level input current	absolute value	-	30	-	µA
I_{IH}	HIGH-level input current	absolute value	-	70	-	µA
C_I	input capacitance		-	1.2	-	pF
pins SYSREFP, SYSREFN, SYNCBP, and SYNCBN						
$V_{i(cm)}$	common-mode input voltage		0.925	1.2	1.475	V
$V_{i(dif)}$	differential input voltage		0.2	0.7	-	V
pins SCS_N, SDIO, SCLK, SCR_EN and CFG						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDO}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDO}$	-	V_{DDO}	V
Logic output: pins CFG and SDIO						
V_{OL}	LOW-level output voltage		0	-	0.2	V
V_{OH}	HIGH-level output voltage		V_{DDO}-0.2	-	V_{DDO}	V
Digital outputs: pins CMLAP, CMLAN, CMLBP, and CMLBN						
$V_{O(cm)}$	common-mode output voltage	default current	-	1.4	-	V
$V_{O(dif)}$	differential output voltage	default current; peak-to-peak	-	800	-	mV
Analog inputs: pins INP and INM						
I_I	input current		-	±5	-	µA
R_I	input resistance	f_i = 190 MHz	-	<tbd>	-	Ω
C_I	input capacitance	f_i = 190 MHz	-	5	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{INP} = V_{INM}$	<tbd>	0.9	<tbd>	V
B_i	input bandwidth		-	1	-	GHz
$V_{I(dif)}$	differential input voltage	peak-to-peak; full-scale	1	-	2	V
Common-mode output voltage: pins VCMA and VCMB						
$V_{O(cm)}$	common-mode output voltage		-	0.9	-	V
$I_{O(cm)}$	common-mode output current	T_{amb} = 25 °C	-	-	1	mA

Table 5. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Accuracy						
INL	integral non-linearity	f_s = 185 Msps; f_i = 4.43 MHz	<tbd>	4.4	<tbd>	LSB
DNL	differential non-linearity	f_s = 185 Msps; f_i = 4.43 MHz; guaranteed no missing codes	<tbd>	–0.24 +0.48	<tbd>	LSB
E_{offset}	offset error		-	<tbd>	-	mV
E_G	gain error	full-scale	-	<tbd>	-	%
$M_{G(CTC)}$	channel-to-channel gain matching		-	<tbd>	-	%
Supply						
PSRR	power supply rejection ratio	<tbd> mV (p-p) on V_{DDA}	-	<tbd>	-	dB

[1] Typical values measured at $V_{DDA} = V_{DDO}$ = 1.8 V; T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = –40 °C to +85 °C at $V_{DDA} = V_{DDO}$ = 1.8 V; $V_{I(dif)}$ = 2 V; $V_{INP} – V_{INM}$ = –1 dBFS; unless otherwise specified.

10. Dynamic characteristics

10.1 Dynamic characteristics

Table 6. Dynamic characteristics[1]

Symbol	Parameter	Conditions	ADC1443D125 (f_s = 125 Msps)			ADC1443D160 (f_s = 154 Msps)			ADC1443D200 (f_s = 185 Msps)			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
α_{2H}	second harmonic level	f_i = 5 MHz	-	-87	-	-	-84	-	-	<tbd>	-	dBc
		f_i = 70 MHz	-	-85	-	-	-82	-	-	<tbd>	-	dBc
		f_i = 140 MHz	-	-92	-	-	-85	-	-	<tbd>	-	dBc
		f_i = 170 MHz	-	-83	-	-	-83	-	-	<tbd>	-	dBc
		f_i = 190 MHz	-	-82	-	-	-86	-	-	<tbd>	-	dBc
		f_i = 230 MHz	-	-78	-	-	-80	-	-	<tbd>	-	dBc
α_{3H}	third harmonic level	f_i = 5 MHz	-	-100	-	-	-88	-	-	<tbd>	-	dBc
		f_i = 70 MHz	-	-97	-	-	-90	-	-	<tbd>	-	dBc
		f_i = 140 MHz	-	-88	-	-	-89	-	-	<tbd>	-	dBc
		f_i = 170 MHz	-	-94	-	-	-90	-	-	<tbd>	-	dBc
		f_i = 190 MHz	-	-96	-	-	-87	-	-	<tbd>	-	dBc
		f_i = 230 MHz	-	-95	-	-	-85	-	-	<tbd>	-	dBc
SFDR	spurious-free dynamic range	f_i = 5 MHz	-	87	-	-	84	-	-	<tbd>	-	dBc
		f_i = 70 MHz	-	85	-	-	82	-	-	<tbd>	-	dBc
		f_i = 140 MHz	-	92	-	-	85	-	-	<tbd>	-	dBc
		f_i = 170 MHz	-	83	-	-	83	-	-	<tbd>	-	dBc
		f_i = 190 MHz	-	82	-	-	86	-	-	<tbd>	-	dBc
		f_i = 230 MHz	-	78	-	-	80	-	-	<tbd>	-	dBc
THD	total harmonic distortion	f_i = 5 MHz	-	-86.5	-	-	-82.3	-	-	<tbd>	-	dBc
		f_i = 70 MHz	-	-84.2	-	-	-80	-	-	<tbd>	-	dBc
		f_i = 140 MHz	-	-85.3	-	-	-82.8	-	-	<tbd>	-	dBc
		f_i = 170 MHz	-	-81.8	-	-	-81.7	-	-	<tbd>	-	dBc
		f_i = 190 MHz	-	-81.4	-	-	-81.9	-	-	<tbd>	-	dBc
		f_i = 230 MHz	-	-77.5	-	-	-78.5	-	-	<tbd>	-	dBc

Table 6. Dynamic characteristics[1] *...continued*

Symbol	Parameter	Conditions	ADC1443D125 (f_s = 125 Msps)			ADC1443D160 (f_s = 154 Msps)			ADC1443D200 (f_s = 185 Msps)			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IMD3	third-order intermodulation distortion	f_{i1} = 3.5 MHz; f_{i2} = 6.5 MHz	-	91	-	-	90	-	-	<tbd>	-	dBc
		f_{i1} = 68.5 MHz; f_{i2} = 71.5 MHz	-	90	-	-	89	-	-	<tbd>	-	dBc
		f_{i1} = 138.5 MHz; f_{i2} = 141.5 MHz	-	89	-	-	88	-	-	<tbd>	-	dBc
		f_{i1} = 168.5 MHz; f_{i2} = 171.5 MHz	-	91	-	-	88	-	-	<tbd>	-	dBc
		f_{i1} = 188.5 MHz; f_{i2} = 191.5 MHz	-	88	-	-	87	-	-	<tbd>	-	dBc
		f_{i1} = 228.5 MHz; f_{i2} = 231.5 MHz	-	87	-	-	87	-	-	<tbd>	-	dBc
SNR	signal-to-noise ratio	f_i = 5 MHz	-	72.6	-	-	71.9	-	-	<tbd>	-	dBFS
		f_i = 70 MHz	-	72.4	-	-	71.7	-	-	<tbd>	-	dBFS
		f_i = 140 MHz	-	72.1	-	-	71.3	-	-	<tbd>	-	dBFS
		f_i = 170 MHz	-	71.6	-	-	70.8	-	-	<tbd>	-	dBFS
		f_i = 190 MHz	-	71.2	-	-	70.6	-	-	<tbd>	-	dBFS
		f_i = 230 MHz	-	70.6	-	-	70	-	-	<tbd>	-	dBFS
ENOB	effective number of bits	f_i = 5 MHz	-	11.7	-	-	11.4	-	-	<tbd>	-	bit
		f_i = 70 MHz	-	11.7	-	-	11.4	-	-	<tbd>	-	bit
		f_i = 140 MHz	-	11.7	-	-	11.3	-	-	<tbd>	-	bit
		f_i = 170 MHz	-	11.5	-	-	11.3	-	-	<tbd>	-	bit
		f_i = 190 MHz	-	11.5	-	-	11.2	-	-	<tbd>	-	bit
		f_i = 230 MHz	-	11.3	-	-	11.1	-	-	<tbd>	-	bit
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 140 MHz	-	95	-	-	95	-	-	<tbd>	-	dBc
		f_i = 230 MHz	-	90	-	-	90	-	-	<tbd>	-	dBc

[1] Typical values measured at V_{DDA} = V_{DDO} = 1.8 V; T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = –40 °C to +85 °C at V_{DDA} = V_{DDO} = 1.8 V; $V_{I(dif)}$ = 2 V; V_{INP} – V_{INM} = –1 dBFS; unless otherwise specified.

10.2 Timing

10.2.1 Clock timing

Table 7. Clock and digital output timing characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{lat(data)}$	data latency time		-	42	-	clock cycles
t_{wake}	wake-up time	from Power-down mode	-	<tbd>	-	ns
		from Sleep mode	-	<tbd>	-	ns
		from high impedance	-	<tbd>	-	ns
Clock timing						
f_s	sampling rate	ADC1443D125	60	-	125	MHz
		ADC1443D160	125	-	160	MHz
		ADC1443D200	160	-	200	MHz
f_{clk}	clock frequency		60	-	800	MHz
δ_{clk}	clock duty cycle		30	-	70	%
$t_{d(s)}$	sampling delay time		-	<tbd>	-	ns

[1] Typical values measured at $V_{DDA} = V_{DDO} = 1.8$ V; $T_{amb} = 25$ °C. Minimum and maximum values are across the full temperature range $T_{amb} = -40$ °C to 85 °C at $V_{DDA} = V_{DDO} = 1.8$ V; $V_{I(dif)} = 2$ V; $V_{INP} - V_{INM} = -1$ dBFS; unless otherwise specified.

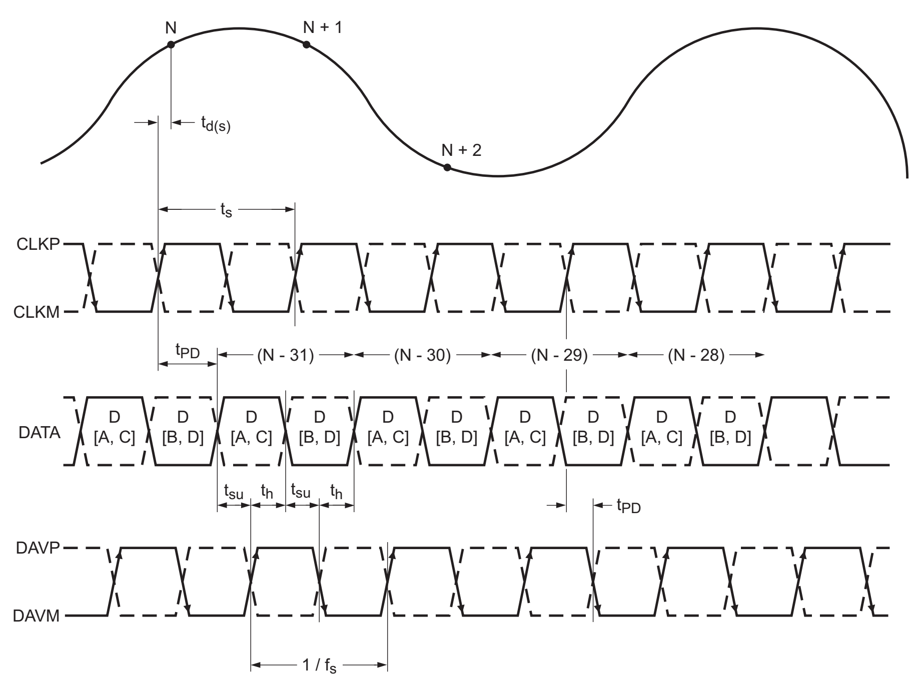


Fig 3. Clock and digital output timing

10.2.2 SYSREF timing

Table 8. SYSREF timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time		<tbd>	-	-	ns
t_h	hold time		<tbd>	-	-	ns

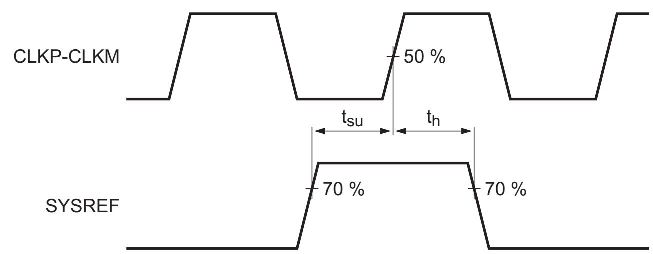


Fig 4. SYSREF timing

10.2.3 SPI timing

Table 9. SPI timing characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		40	-	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		16	-	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		16	-	-	ns
t_{su}	set-up time	SDIO to SCLK HIGH	5	-	-	ns
		SCS_N to SCLK HIGH	5	-	-	ns
t_h	hold time	SDIO to SCLK HIGH	2	-	-	ns
		SCS_N to SCLK HIGH	2	-	-	ns
f_{clk}	clock frequency		-	-	25	MHz

[1] Typical values measured at $V_{DDA} = V_{DDO} = 1.8$ V; $T_{amb} = 25$ °C. Minimum and maximum values are across the full temperature range $T_{amb} = -40$ °C to +85 °C at $V_{DDA} = V_{DDO} = 1.8$ V

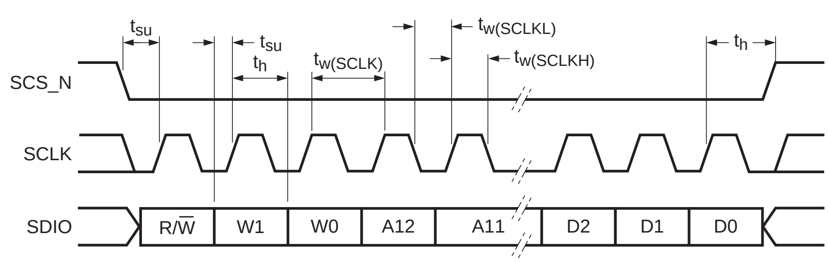


Fig 5. SPI timing

10.3 Typical dynamic performances[1]

10.3.1 Typical FFT at 122.88 Msps

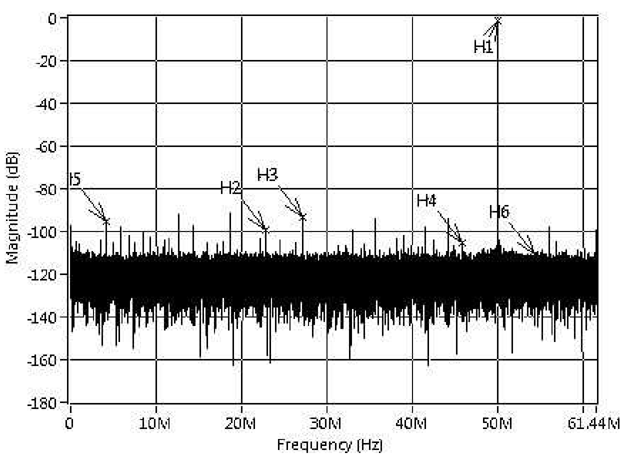


Fig 6. 1-tone FFT: –1 dBFS; f_i = 50 MHz; f_s = 122.88 Msps

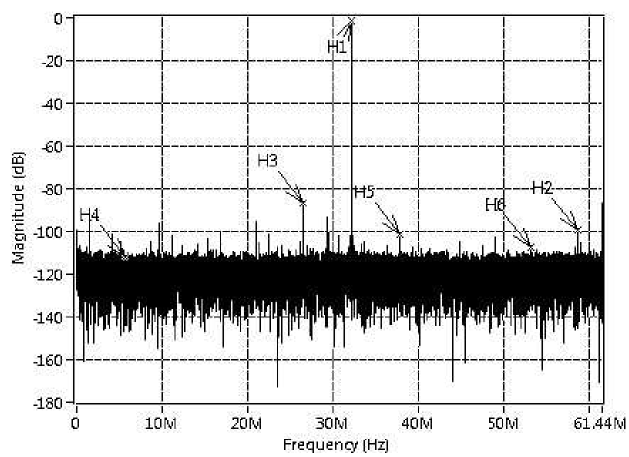


Fig 7. 1-tone FFT: –1 dBFS; f_i = 155 MHz; f_s = 122.88 Msps

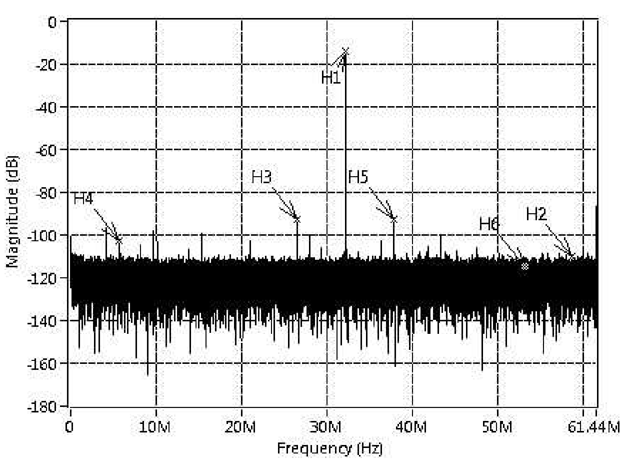


Fig 8. 1-tone FFT: –14 dBFS; f_i = 155 MHz; f_s = 122.88 Msps

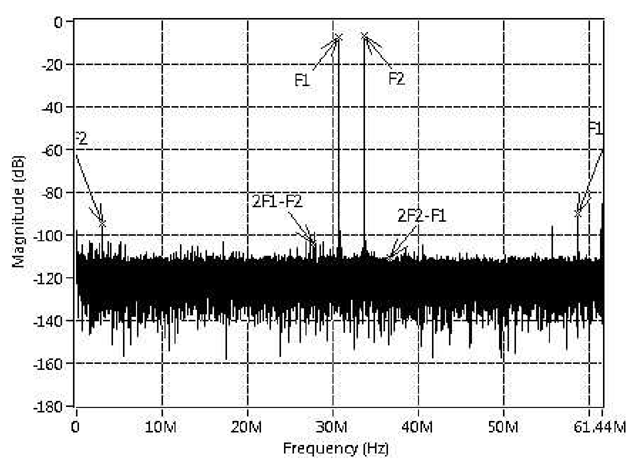


Fig 9. SNR as a function of full-scale amplitude: –1 dBFS; f_i = 190 MHz; f_s = 185 Msps

1. Typical values measured at $V_{DDA} = V_{DDO}$ = 1.8 V; T_{amb} = 25 °C

10.3.2 Typical FFT at 153.6 Msps

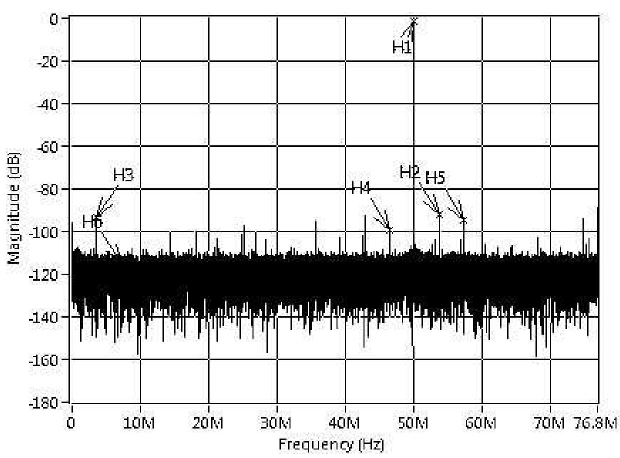


Fig 10. 1-tone FFT: –1 dBFS; f_i = 50 MHz; f_s = 153.6 Msps

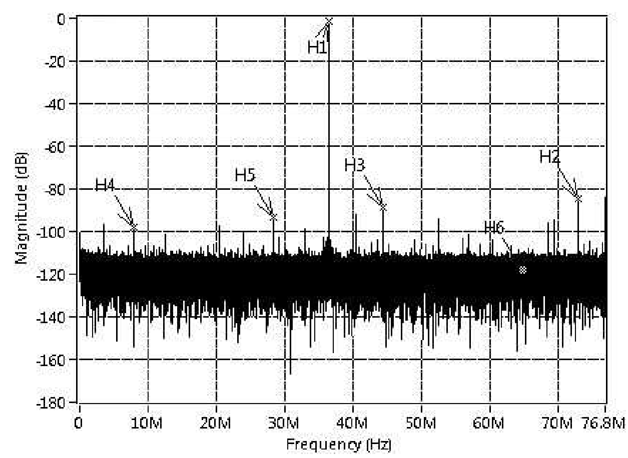


Fig 11. 1-tone FFT: –1 dBFS; f_i = 190 MHz; f_s = 153.6 Msps

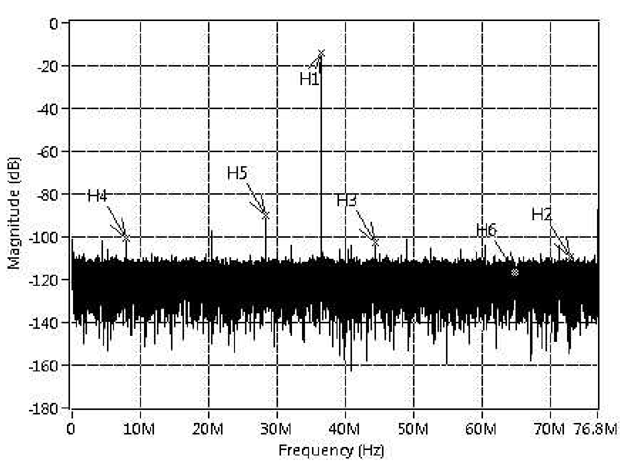


Fig 12. 1-tone FFT: –14 dBFS; f_i = 190 MHz; f_s = 153.6 Msps

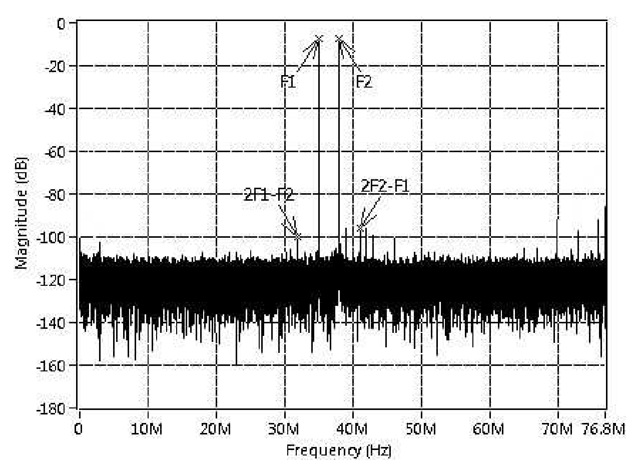


Fig 13. 2-tone FFT: –7 dBFS; f_{i1} = 188.5 MHz; f_{i2} = 191.5 MHz; f_s = 153.6 Msps

10.3.3 Typical SNR performances

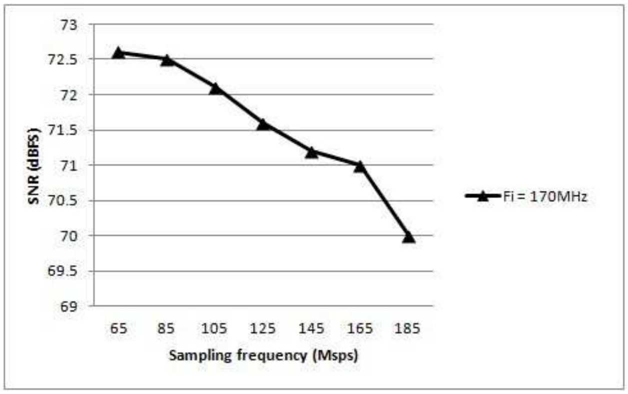


Fig 14. SNR as a function of sampling frequency: –1 dBFS; f_i = 170 MHz

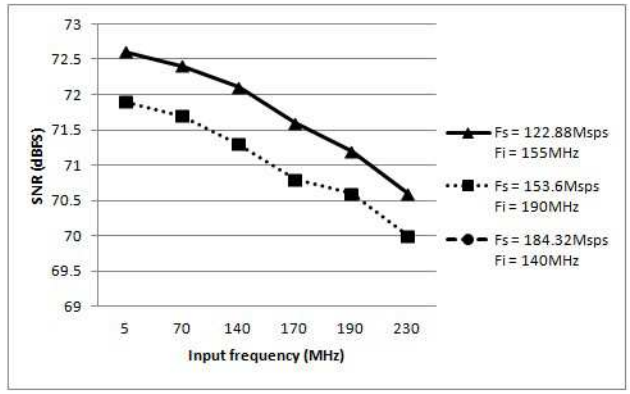


Fig 15. SNR as a function of input frequency: –1 dBFS

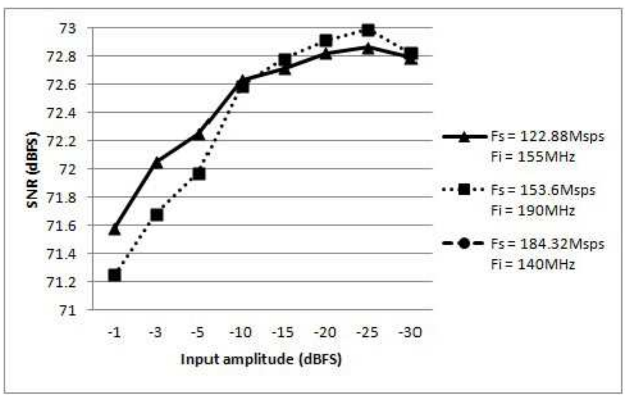


Fig 16. SNR as a function of input amplitude: f_i = 190 MHz; f_s = 185 Msps; $V_{I(dif)}$ = 2 V

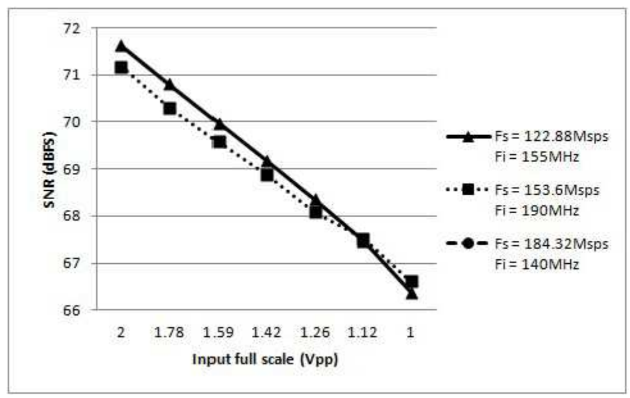


Fig 17. SFDR as a function of full-scale amplitude: –1 dBFS; f_i = 190 MHz; f_s = 185 Msps

10.3.4 Typical SFDR performances

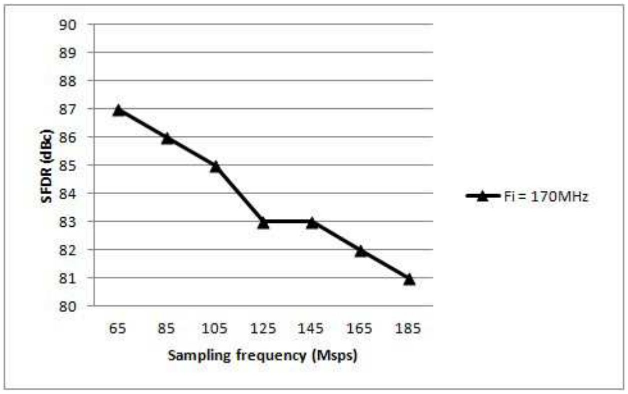


Fig 18. SFDR as a function of sampling frequency: –1 dBFS; f_i = 170 MHz

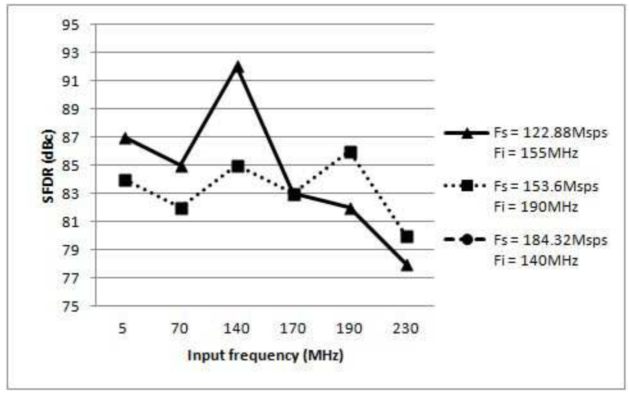


Fig 19. SFDR as a function of input frequency: –1 dBFS

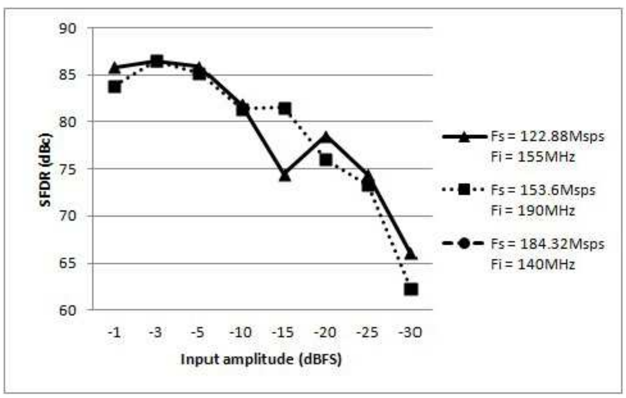


Fig 20. SFDR as a function of input amplitude: $V_{I(dif)}$ = 2 V

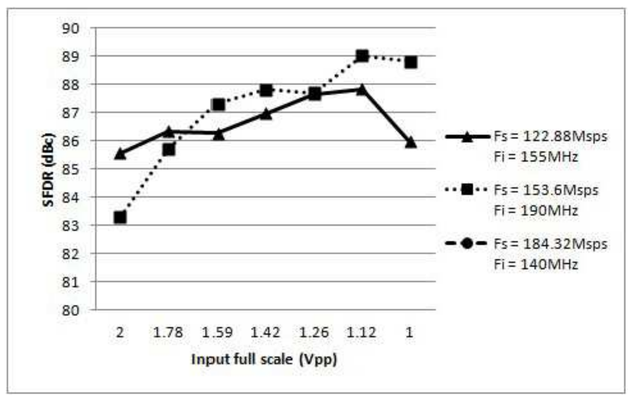


Fig 21. SFDR as a function of full-scale amplitude: –1 dBFS

10.3.5 Typical IMD3 performances

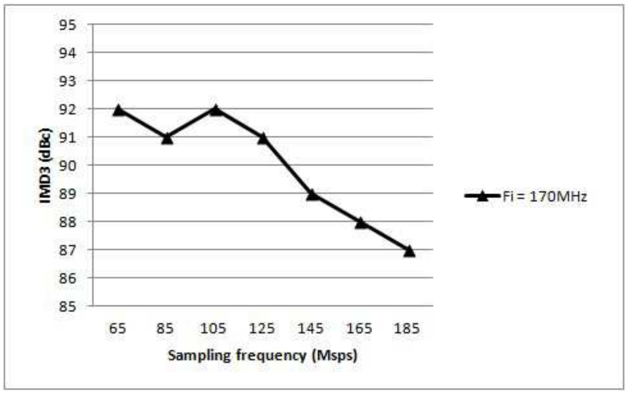


Fig 22. IMD3 as a function of sampling frequency: –7 dBFS; f_{i1} = 168.5 MHz; f_{i2} = 171.5 MHz

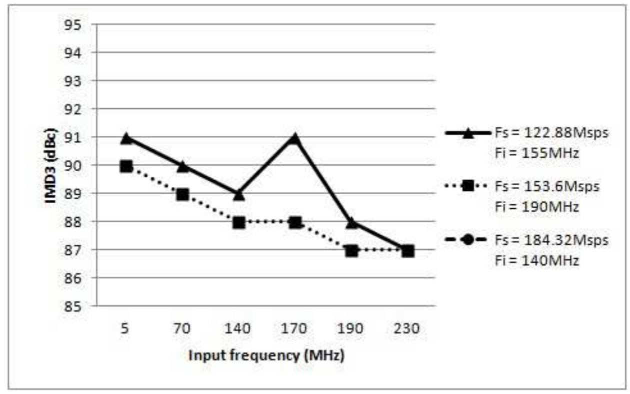


Fig 23. IMD3 as a function of input frequency: –7 dBFS; 3 MHz spacing

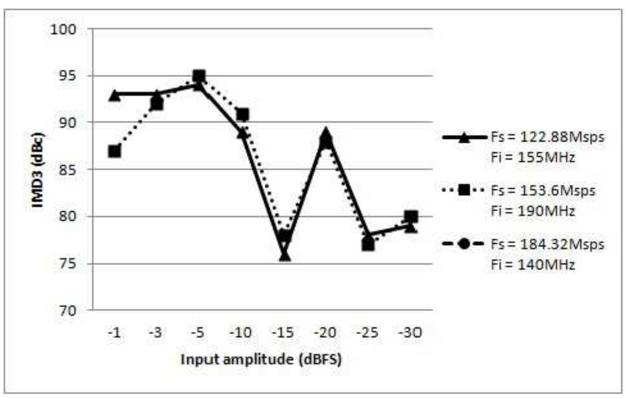


Fig 24. IMD3 as a function of input amplitude: 3 MHz spacing; $V_{I(dif)}$ = 2 V

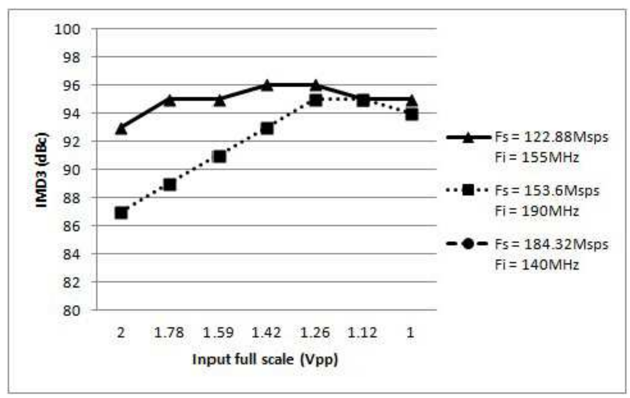


Fig 25. IMD3 as a function of full-scale amplitude: –7 dBFS; 3 MHz spacing

11. Application information

11.1 Analog inputs

11.1.1 Input stage

The analog input of the ADC1443D supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with respect to the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM.

The equivalent circuit of the sample and hold input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics, is shown in Figure 26.

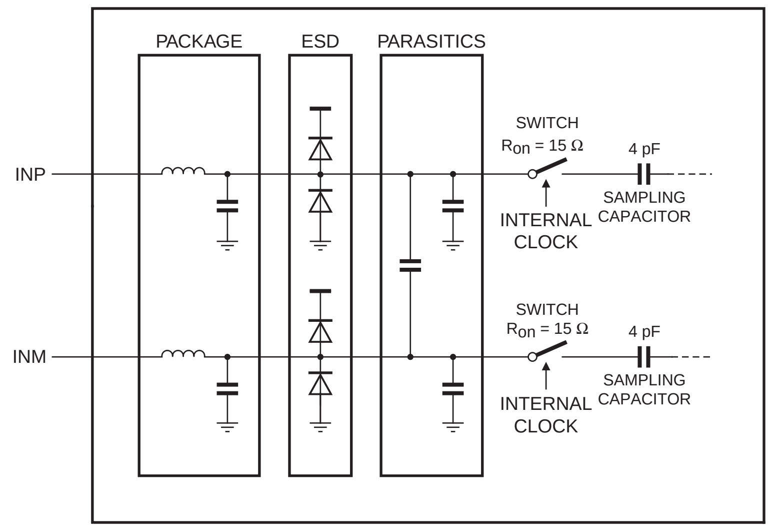


Fig 26. Input sampling circuit

The sample phase occurs when the internal sampling clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the sampling clock signal becomes LOW, the device enters the hold phase and the voltage information is transmitted to the ADC core.

11.1.2 Common-mode input voltage ($V_{I(cm)}$)

Set the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM externally to 0.9 V for optimal performance.

11.1.3 Pin VCM

When the input stage is AC-coupled, pin VCM can be used to set the common-mode reference for the analog inputs, for instance, via a transformer middle point. Connect a 0.1 μF filter capacitor between pin VCM and ground to ensure a low-noise common-mode output voltage.

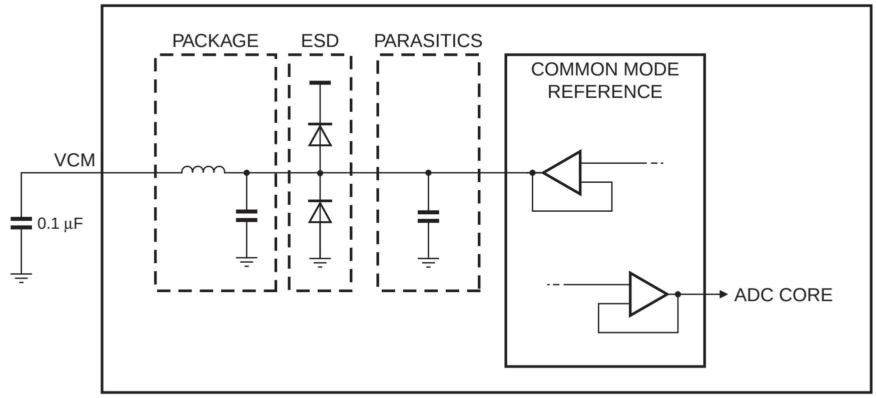


Fig 27. Equivalent schematic of the common-mode reference circuit

11.1.4 Programmable full-scale

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) by programming internal reference gain between 0 dB and –6 dB in 1 dB steps. The full-scale range can be set independently via bits INTREF[2:0] of the SPI local registers (see Table 10 and Table 24).

Table 10. Reference gain control
Default values are shown highlighted.

INTREF[2:0]	Level (dB)	Full-scale (V (p-p))
000	**0**	**2**
001	–1	1.78
010	–2	1.59
011	–3	1.42
100	–4	1.26
101	–5	1.12
110	–6	1
111	reserved	x

11.1.5 Anti-kickback circuitry

An anti-kickback circuitry (RC-filter in Figure 28) is required to counteract the effects of the charge injection generated by the sampling capacitance.

The RC-filter is also used to filter noise from the signal before it reaches the sampling stage. It is recommended that the capacitor has a value that maximizes noise attenuation without degrading the settling time excessively.

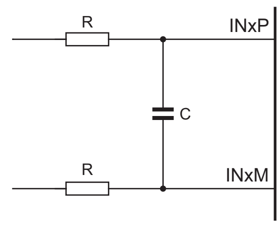


Fig 28. Anti-kickback circuit

The input frequency determines the component values. Select values that do not affect the input bandwidth. The value given in the following tablme are advised for 50Ω impedances system

Table 11. RC coupling versus input frequency; typical values

Input frequency range (MHz)	R (Ω)	C (pF)
0 to 50	25	12
50 to 200	10	3.9
200 to 300	6.8	3

11.1.6 Transformer

The input frequency determines the configuration of the transformer circuit. The configuration shown in Figure 29 is suitable for a baseband application.

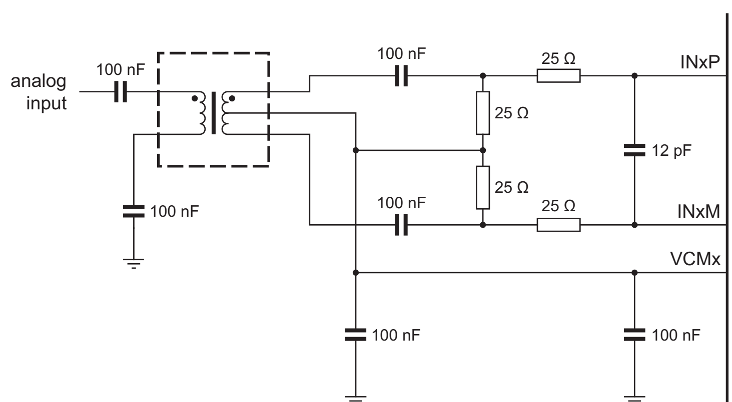


Fig 29. Single transformer configuration (baseband)

The configuration shown in Figure 30 is recommended for high-frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

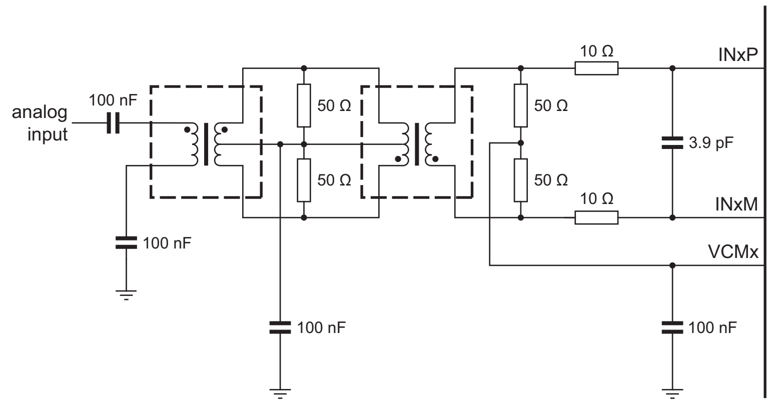


Fig 30. Dual transformer configuration (high IF)

11.2 Clock input

11.2.1 Drive modes

The ADC1443D series can be driven differentially (LVPECL, LVDS or SINE). A single-ended LVCMOS signal connected to either pin CLKP or pin CLKM can also drive the device (connect the complementary pin to ground using a capacitor). The LVPECL is recommended for an optimal performance.

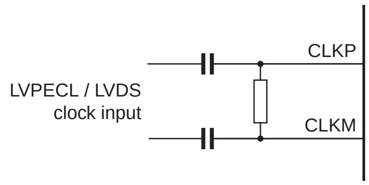
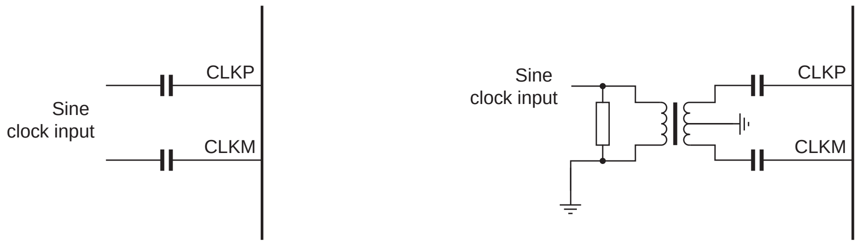


Fig 31. LVPECL/LVDS differential clock input



a. Differential sine clock input

b. Single-ended sine clock input (with transformer)

Fig 32. Sine clock input

Fig 33. LVCMOS single-ended clock input

Single-ended or differential clock inputs can be selected via bit DIFF_SE of SPI. If single-ended is enabled, the input pin (pin CLKM or pin CLKP) is selected using control bit SE_SEL (see Table 23).

11.2.2 Equivalent input circuit

Figure 34 shows the equivalent circuit of the input clock buffer. The input signal must be AC-coupled and the common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.

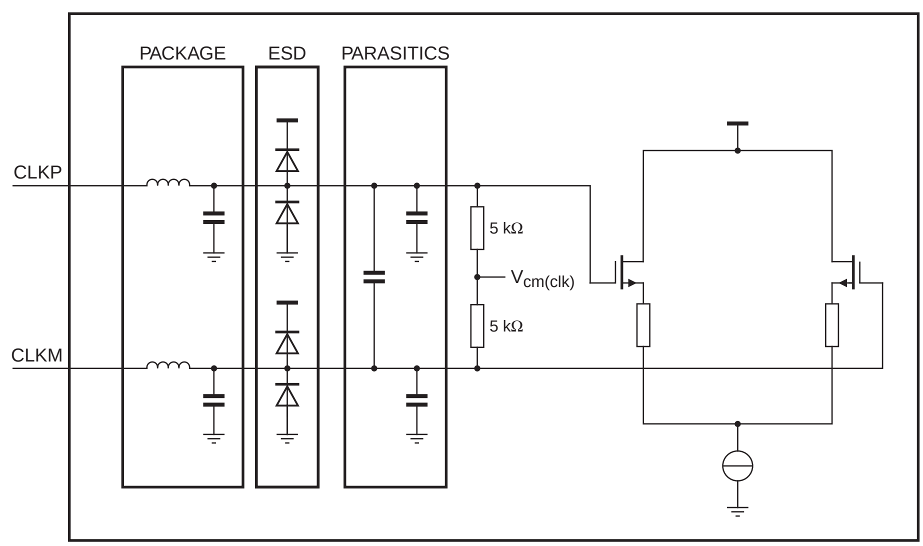


Fig 34. Equivalent input circuit

11.2.3 JESD204B harmonic clocking

The ADC1443D contains an input clock divider that divides the incoming clock (clock frequency fclk) by a factor of 1 to 8. The output of this divider is the sampling clock (sampling frequency fs) (see bits CLK_DIV[1:0] in Table 23). This feature allows a higher clock frequency to be delivered to the ADC1443D and hence get a better jitter performance, leading to a better SNR result.

The ADC1443D should not be fed with a clock higher than 250Msps if the clock divider is not enabled, otherwise there is a risk of metastability.

Two options are allowed, either to program first the clock divider before enabling the Harmonic Clock, or to power-up the ADC1443 in « Power Down» mode by setting the CFG_SETUP[3:0] to «1111» see Table 16 , then program the clock divider to the wanted value and then «wake-up» the ADC using the SPI register IP_CFG_SETUP Table 36, with the wanted configuration.

11.2.4 JESD204B Deterministic Latency (pins SYSREFN and SYSREFP or SYNCBP and SYNCBN)

In the JESD204B standard 3 subclasses have been defined.

Subclass 0: No deterministic latency is required (equivalent to the JESD204A)

Subclass 1: Deterministic latency is wanted and is realized through the dedicated SYSREF pins.

The deterministic latency can be controlled with a single-ended or a differential SYSREF signal.

When SYSREF is active (High by default), it resets the clock divider phase registers. In a multi-device application and when the clock divider factor is higher than 1, the ADC1443D synchronization aligns all sampling clock edges (see Table 8 and Figure 4).

On top of this, the SYSREF pins launch an internal LMFC counter (Local Multi-frame counter), which has a period of a multi-frame F*K (F: number of octets per frame, K: number of frames per multi-frame) see table Table 16 for examples.

When a SYNC request occurs at SYNCBP/N , the ADC1443 will start the ILA sequence at an edge of the LMFC .
At the receiver side, the different lanes are aligned using the ILA and the ADC1443D releases the data at an LMFC boundary.

The receiver and the ADC1443D are nowboth starting an LMFC and ensuring an alignment based on this clock, which allow a deterministic latency.

Subclass2 : Behaviour is similar to Subclass1, but, instead of using a dedicated SYSREF signal, the SYNCBP/N is used for both SYNC request and deterministic latency.

The rising edge of the SYNCBP/N start the LMFC, while the falling edge set the SYNC request and hence start the Initial Lane Alignement according to the JEDEC JESD204B standard.

11.3 Digital outputs

11.3.1 Digital output buffers

The JESD204A/JESD204B standard specifies that both the receiver and the transmitter must be provided by the same supply if they are connected in DC-coupling.

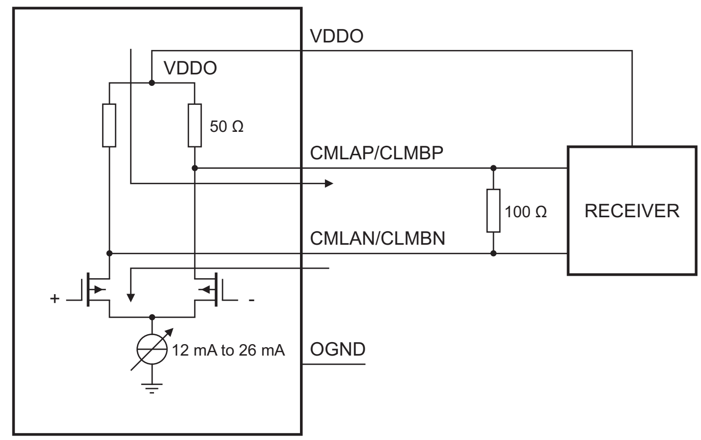


Fig 35. JESD204A/JESD204B serial output - DC-coupled

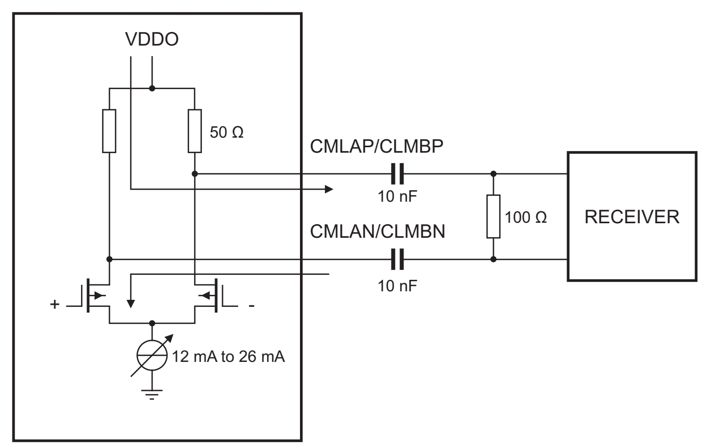


Fig 36. JESD204A/JESD204B serial output - AC-coupled

11.3.2 JESD204A/JESD204B serializer

11.3.2.1 Digital JESD204A/JESD204B formatter

The block placed after the ADC1443D cores is used to implement all functionalities of the JESD204A/JESD204B standard. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly parameterized and can be configured in various ways depending on the sampling frequency and the number of lanes used.

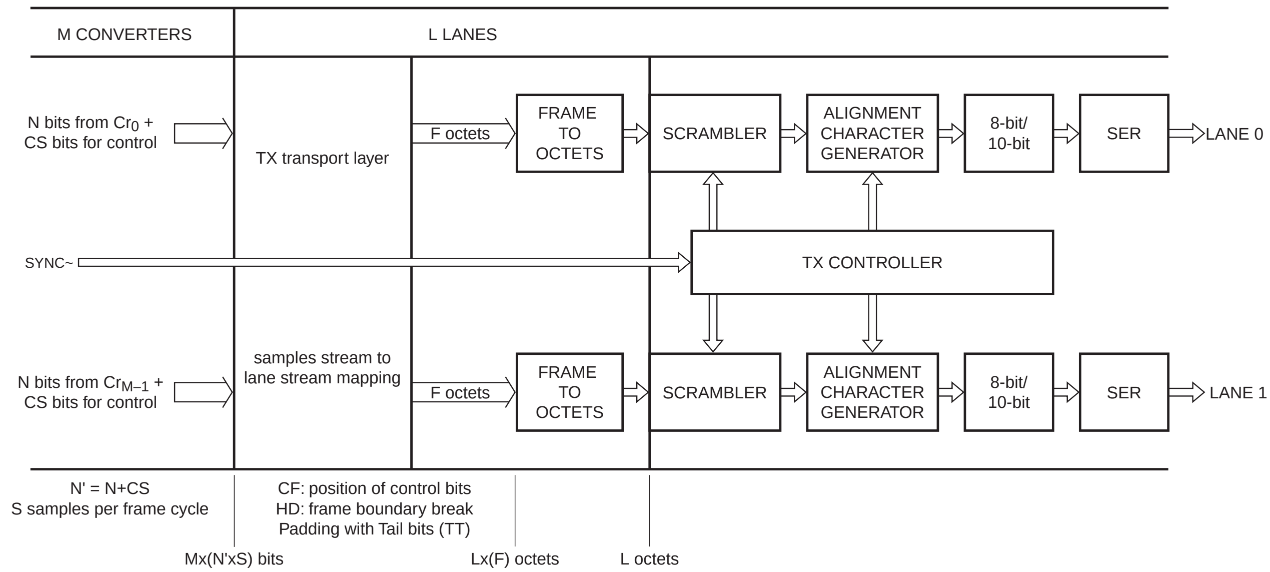


Fig 37. General overview of the JESD204A/JESD204B serializer

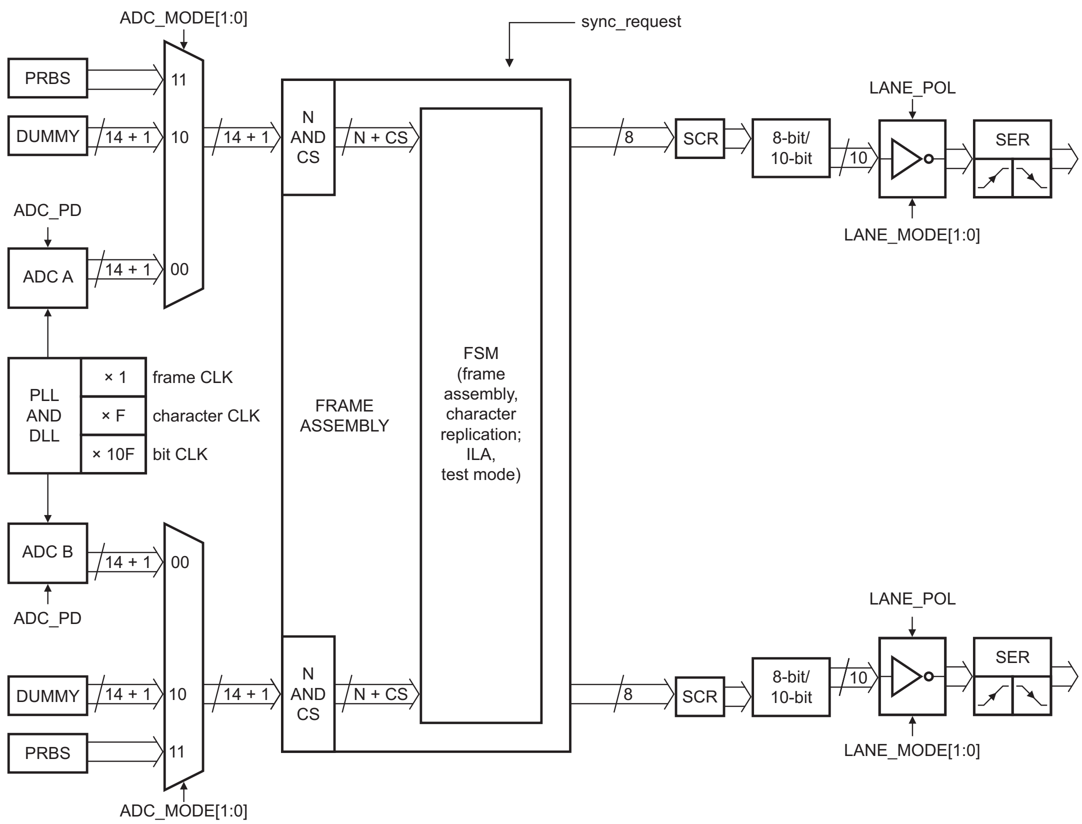


Fig 38. Detailed view of the JESD204A/JESD204B serializer with debug functionalities

11.3.3 OuT-of-Range (OTR)

An out-of-range signal is provided on pins OTRA and OTRAB.

The latency of OTR is 31 clock cycles. The OTR response can be speeded up by enabling fast OTR using SPI local registers (bit FAST_OTR in Table 31). In this mode, the latency of OTR is reduced to only 11 clock cycles. The fast OTR detection threshold (below full-scale) can be programmed using the SPI local registers (bits FAST_OTR_DET[2:0] in Table 31).

Table 12. Fast OTR register threshold

FAST_OTR_DET[2:0]	Detection level (dB)
000	–18.06
001	–14.54
010	–12.04
011	–8.52
100	**–6.02**
101	–4.08
110	–2.5
111	–1.16

11.3.4 Digital offset

By default, the ADC1443D delivers an output code that corresponds to the analog input. However, it is possible to add a digital offset to the output code using the SPI local registers (bits DIG_OFFSET[5:0] in see Table 13 and Table 27). The digital offset adjustment is coded in two's complement.

Table 13. Digital offset adjustment

Default values are shown highlighted.

DIG_OFFSET[5:0]	Digital offset adjustment (LSB)
10 0000	–32
10 0001	–31
...	...
11 1111	–1
00 0000	**0**
00 0001	+1
...	...
01 1110	+30
01 1111	+31

11.3.5 Test patterns

The ADC1443D can be configured to transmit a number of predefined test patterns using the SPI local registers (bits TEST_PAT_SEL[2:0] in Table 14 and Table 28). The selected test pattern is transmitted regardless of the analog input.

Table 14. Digital test pattern selection
Default values are shown highlighted.

TEST_PAT_SEL[2:0]	Digital test pattern
000	**Off**
001	Mid code
010	Min code
011	Max code
100	Toggle ‘1111..1111’/’0000..0000’
101	Custom test pattern
110	‘0101..0101’
111	‘1010..1010’

A custom test pattern can be defined using the SPI local registers (bits TEST_PAT_USER[13:6] in Table 29 and bits TEST_PAT_USER[5:0] in Table 30).

11.3.6 Output data format selection

The ADC1443D output data format can be selected (offset binary, two’s complement or gray code) using the SPI local registers (bits DATA_FORMAT[1:0] in Table 26).

11.3.7 Output codes versus input voltage

Table 15. Output codes

$V_{INP} - V_{INM}$	Offset binary	Two’s complement	Gray code	OTR
< –1	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000	1
–1	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000	0
–0.99987793	00 0000 0000 0001	10 0000 0000 0001	00 0000 0000 0001	0
–0.99975586	00 0000 0000 0010	00 0000 0000 0010	00 0000 0000 0011	0
...	...	...	...	0
–0.00024414	01 1111 1111 1110	11 1111 1111 1110	01 0000 0000 0001	0
–0.00012207	01 1111 1111 1111	11 1111 1111 1111	01 0000 0000 0000	0
+0.00012207	10 0000 0000 0000	00 0000 0000 0000	11 0000 0000 0000	0
+0.0.00024414	10 0000 0000 0001	00 0000 0000 0001	11 0000 0000 0001	0
...	...	...	...	0
+0.99975586	11 1111 1111 1101	01 1111 1111 1101	10 0000 0000 0011	0
+0.99987793	11 1111 1111 1110	01 1111 1111 1110	10 0000 0000 0001	0
+1	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	0
> +1	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	1

11.4 Configuration pins (CFG0, CFG1, CFG2, CFG3)

The configuration pins are only active as inputs at start-up. The values on those pins are read once to set up the device. Then the pins become outputs (OTRA and OTRB). SPI applies any change in the configuration.

N.B: for harmonic clocking uses, the CFG pins must be set to «1111», to start the ADC in power down mode and hence avoid any issue that comes from delivering a high frequency clock before setting the clock division.

Table 16. JESD204A/JESD204B configuration table

CFG_SETUP[3:0]		ADC A	ADC B	Lane 0	Lane 1	F[1]	HD[1]	K[1]	M[1]	L[1]	Comment	CS[1]	CF[1]	S[1]
0	0000	**ON**	**ON**	**ON**	**ON**	2	0	9	2	2	(F × K) ≥ 17	1	0	1
1	0001	**ON**	**ON**	**ON**	OFF	4	0	5	2	1	(F × K) ≥ 17	1	0	1
2	0010	**ON**	**ON**	OFF	**ON**	4	0	5	2	1	(F × K) ≥ 17	1	0	1
3	0011	reserved												
4	0100	reserved												
5	0101	**ON**	OFF	**ON**	OFF	2	0	9	1	1	(F × K) ≥ 17	1	0	1
6	0110	**ON**	OFF	OFF	**ON**	2	0	9	1	1	(F × K) ≥ 17	1	0	1
7	0111	OFF	**ON**	**ON**	OFF	2	0	9	1	1	(F × K) ≥ 17	1	0	1
8	1000	OFF	**ON**	OFF	**ON**	2	0	9	1	1	(F × K) ≥ 17	1	0	1
9	1001	**ON**	OFF	**ON**	**ON**	1	1	17	1	2	(F × K) ≥ 17	1	0	1
10	1010	OFF	**ON**	**ON**	**ON**	1	1	17	1	2	(F × K) ≥ 17	1	0	1

Table 16. JESD204A/JESD204B configuration table *…continued*

CFG_SETUP[3:0]		ADC A	ADC B	Lane 0	Lane 1	F[1]	HD[1]	K[1]	M[1]	L[1]	Comment	CS[1]	CF[1]	S[1]
11	1011	reserved												
12	1100	reserved												
13	1101	reserved												
14	1110	reserved												
15	1111	OFF	OFF	OFF	OFF	2	0	9	2	2	chip power-down	1	0	1

[1] F: Octets per frame clock cycle
HD: High-density mode
K: Frame per multi-frame
M: Converters per device
L: Lane per converter device
CS: Number of control bits per conversion sample
CF: Control words per frame clock cycle and link
S: Number of samples transmitted per single converter per frame cycle

11.5 Serial Peripheral Interface (SPI)

11.5.1 Register description

The ADC1443D serial interface is a synchronous serial communications port, which allows easy interfacing with many commonly used microprocessors. It provides access to the registers controlling the operation of the chip.

The register bits are either global or local functions:

- A global function operates over the full IC behavior. A local function operates on one or several previously selected channels only. If a channel is selected, the next WRITE command in the local registers applies to the selected channel. The WRITE command has no impact on channels that are not selected. This makes it possible to apply different configurations on each channel by first selecting a specific channel and then all the related settings.
- Select only one channel during a READ operation of the local registers. If several channels are selected, the READ operation occurs on the channel A.

Programming all registers at the same time is required:

- The IC allows the storage of a set of settings for the addresses 06h to 23h, which enables the configuration of all registers simultaneously by setting bit TRANSFER to HIGH (see Table 33). This bit is autoclearing. This function can be disabled using SPI (bit TRANS_DIS in Table 33). The registers are then updated at each WRITE operation.
- The transfer function does not apply to a READ operation.

The SPI interface is configured as a 3-wire type: pin SDIO is the bidirectional pin, pin SCLK is the serial clock input and SCS_N is the chip select pin.

A LOW level on pin SCS_N initiates each READ/WRITE operation. A minimum of 3 bytes is transmitted (two instruction bytes and at least 1 DATA byte; see Table 18).

Table 17. Instruction bytes for the SPI

Bit:	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Description	R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

- Bit R/$\overline{W}$ indicates whether it is a READ (when HIGH) or a WRITE (when LOW) operation.
- Bits W1 and W0 indicate the number of bytes to be transferred after both instruction bytes (see Table 18).

Table 18. Number of data bytes transferred

W1	W0	Number of bytes transferred
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 or more bytes

- Bits A12 to A0 indicate the address of the register being accessed. If it concerns a multiple byte transfer, this address is the first register accessed. An address counter is increased to access subsequent addresses.

The steps for a data transfer are:

1. Communication starts with the first rising edge on pin SCLK after a falling edge on pin SCS_N.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data. Its length varies, but it is always a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on pin SCS_N indicates the end on data transmission.

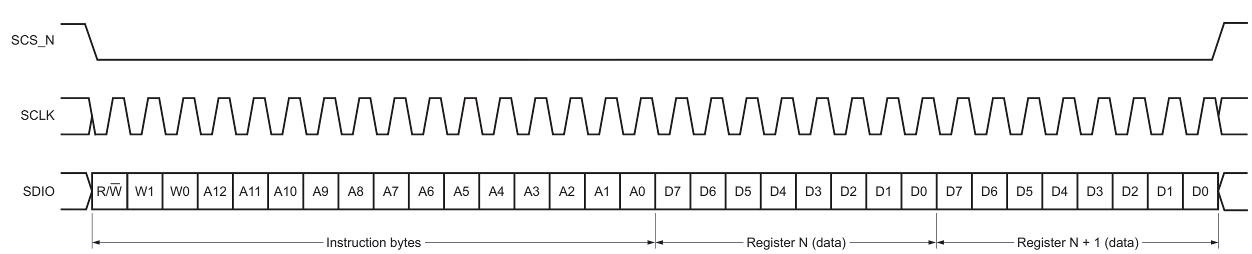


Fig 39. SPI mode timing

11.5.2 Register allocation map

Table 19 shows an overview of all registers.

Table 19. Register allocation map

Addr. (hex)	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ADC control registers											
0000h	CHIP_RST	RW	SW_RST[7:0]								0000 0000
0001h	CHIP_ID	R	CHIP_ID[7:0][1]								0100 0011
0005h	CHIP_RST	R/W	SW_RST	-	-	-	-	-	-	-	0000 0000
0006h [2]	OP_MODE	R/W	-	-	-	-	-	-	OP_MODE[1:0][3]		0000 0000
0007h	CLK_CFG	R/W	-	-	-	SE_SEL	DIFF_SE	CLK_DIV[2:0]			0000 0000
0008h	INTERNAL_ REF	R/W	-	-	-	-	-	INTREF[2:0]			0000 0000
0009h	CHANNEL_ SEL	R/W	-	-	-	-	-	-	ADC_B	ADC_A	0000 1111
0011h	OUTPUT_ CFG	R/W	-	-	-	-	-	DATA_ SWAP	DATA_FORMAT[1:0]		0000 0000
0013h	DIG_OFFSET	R/W	DIG_OFFSET[5:0]						-	-	0000 0000
0014h	TEST_CFG_1	R/W	-	-	-	-	-	TEST_PAT_SEL[2:0]			0000 0000
0015h	TEST_CFG_2	R/W	TEST_PAT_USER[13:6]								0000 0000
0016h	TEST_CFG_3	R/W	TEST_PAT_USER[5:0]						-	-	0000 0000
0017h	OTR_CFG	R/W	-	-	-	RESERVED	FAST_ OTR	FAST_OTR_DET[2:0]			0001 0100
0043h	DCS_CTRL	R/W	-	SYSREF_SE	-	-	-	-	DIV_RESET _POL	DIV_RESE T_SEL	11000100
00FFh	TRANS_CFG	R/W	TRANS_ DIS	TRANSFER	-	-	-	-	-	-	0000 0000
JESD204A/JESD204B control											
0801h	IP_STATUS	R	RXSYNC_ ERR_FLG	RESERVED[5:0]						PLL_LOCK	0000 0000
0802h	IP_RST	R/W	SW_ RST	-	-	-	ASSEMBLER_ SW_RST	-	-	-	0000 0000
0803h	IP_CFG_ SETUP	R/W	-	-	-	-	CFG_STP[3:0]				0000 ****

Table 19. Register allocation map *…continued*

Addr. (hex)	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0805h	IP_CTRL1	R/W	RESERVED	TRISTATE_ CFG_PAD	SYNC_ POL	SYNC_SE	EN_ RXSYNC_ERR	RESERVED[2:0]			0000 0000
0806h	IP_CTRL2	R/W	RESERVED[5:0]						SWP_ ‘LANE_1_2	SWP_ ADC_0_1	0000 ****
080Bh	IP_PRBS_ CTRL	R/W	RESERVED[5:0]						PRBS_TYPE[1:0]		0000 0000
0810h	JESD204B_C TRL1	R/W	LMFC_perio dic_rst	LMFC_reset_ en	-	-	-	-	-	-	0000 0000
0811h	JESD204B_C TRL2	R/W	DCS_periodi c_rst	DCS_reset_e n	-	-	-	-	-	-	0000 0000
0812h	JESD204B_C TRL3	R/W	-	-	-	-	sync_at_lmfc_e n	-	sync_captur e_path	-	0000 0000
0816h	IP_DEBUG_ OUT1	R/W	-	-	-	-	-	-	PAT_OUT[9:8]		0000 0010
0817h	IP_DEBUG_ OUT2	R/W	PAT_OUT[7:0]								1010 1010
0818h	IP_DEBUG_ IN1	R/W	PAT_IN[15:8]								1010 1010
0819h	IP_DEBUG_ IN2	R/W	PAT_IN[7:0]								0000 0010
081Bh	IP_ TESTMODE	R/W	RESERVED	LOOP_ ALIGN	DIS_REPL_ CHAR	BYP_ ALIGN	RESERVED[3:0]				0*00 0000
081Ch	IP_EXPERT_ DOOR	R/W	KEY[7:0]								0000 0000
081Eh	SYSREF_CFG	R/W	-	-	-	-	-	SYSREF_E N	SYSREF_S E		0000 0000
0822h	CFG_3_ SCR_L	R/W	SCR[0]	RESERVED[5:0]						L[0]	0000 0000(?)
086Bh	OUTBUF00_ SWING	R/W	RESERVED[4:0]			SWING[3:0]					0000 01**
086Ch	OUTBUF03_ SWING	R/W	SWING_SPARE[2:0]			SWING[3:0]					0000 01**

Table 19. Register allocation map *...continued*

Addr. (hex)	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0871h	LANE00_0_ CTRL	R/W	RESERVED[2:0]			LANE_MODE[1:0]		LANE_POL	RESERVED	LANE_ PD	0000 000*
0872h	LANE01_0_ CTRL	R/W	RESERVED[2:0]			LANE_MODE[1:0]		LANE_POL	RESERVED	LANE_ PD	0000 000*
0890h	ADC00_0_ CTRL	R/W	-	-	ADC_MODE[1:0]		-	-	-	ADC_ PD	0000 0000
0891h	ADC01_0_ CTRL	R/W	-	-	ADC_MODE[1:0]		-	-	-	ADC_ PD	0000 0000

[1] The READ-ONLY and RESERVED registers.

[2] The registers influenced by the TRANSFER function.

[3] The LOCAL registers.

11.5.3 Detailed register description

The tables in this section contain detailed descriptions of the registers.

11.5.3.1 ADC control registers

Table 20. CHIP_RESET register (address 0000h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	SW_RST	R/W	-	resets global and local registers for any value “1” written at any bit (autoclear).

Table 21. CHIP_RESET register (address 0005h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W		resets global and local registers
			0	**no reset**
			1	performs a reset to the default values (autoclear)
6 to 0	-	-	-	not used

Table 22. OP_MODE register (address 0006h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-	-	-	not used
1 to 0	OP_MODE[1:0][1]	R/W		operating mode for the selected channel
			00	**normal (power-up)**
			01	power-down
			10	sleep
			11	not used

[1] Local register.

Table 23. CLK_CFG register (address 0007h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	-	-	-	not used
4	SE_SEL	R/W		single-ended clock input pin selection
			0	**CLKP**
			1	CLKM
3	DIFF_SE	R/W		differential/single-ended clock input selection
			0	**fully differential**
			1	single-ended

Table 23. CLK_CFG register (address 0007h) bit description *...continued*

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
2 to 0	CLK_DIV[1:0]	R/W		clock divider selection
			000	**divide by 1**
			001	divide by 2
			010	divide by 3
			011	divide by 4
			100	divide by 5
			101	divide by 6
			110	divide by 7
			111	divide by 8

Table 24. INTERNAL_REF register (address 0008h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	-	not used
2 to 0	INTREF[2:0][1]	R/W	-	see Table 10

[1] Local register

Table 25. CHANNEL_SEL register (address 0009h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-	-	-	not used
1	ADC_B	R/W		channel B selection for next SPI operation in local registers
			0	not selected
			1	**selected**
0	ADC_A	R/W		channel A selection for next SPI operation in local registers
			0	not selected
			1	**selected**

Table 26. OUTPUT_CFG register (address 0011h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	-	not used
2	DATA_SWAP[1]	R/W		output data bits swapped
			0	**no swapping**
			1	MSBs swapped with LSBs

Table 26. OUTPUT_CFG register (address 0011h) bit description *…continued*

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
1 to 0	DATA_FORMAT[1:0:][1]	R/W		output data format
			00	**offset binary**
			01	two’s complement
			10	gray code
			11	offset binary

[1] Local register

Table 27. DIG_OFFSET register (address 0013h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	DIG_OFFSET[7:0][1]	R/W	-	see Table 13
1 to 0	-	-	-	not used

[1] Local register

Table 28. TEST_CFG_1 register (address 0014h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	-	not used
2 to 0	TEST_PAT_SEL[2:0][1]	R/W	-	see Table 14

[1] Local register

Table 29. TEST_CFG_2 register (address 0015h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	TEST_PAT_USER[13:6][1]	R/W	-	custom digital test pattern (bits 13 to 6)

[1] Local register

Table 30. TEST_CFG_3 register (address 0016h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	TEST_PAT_USER[5:0][1]	R/W	-	custom digital test pattern (bits 5 to 0)
1 to 0	-	-	-	not used

[1] Local register

Table 31. OTR_CFG register (address 0017h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	-	-	-	not used
4	RESERVED	R/W	1	reserved

Table 31. OTR_CFG register (address 0017h) bit description *…continued*
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
3	FAST_OTR[1]	R/W		Selection OTR full-scale/ fast OTR
			0	OTR full-scale
			1	**fast OTR**
2 to 0	FAST_OTR_DET[2:0][1]	R/W	-	

[1] Local register

Table 32. DCS_CTRL register (address 0043h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	-	-	1	not used, set allways to 1
6	-	-	1	not used, set allways to 1
5 to 2	-	-	-	not used
1	DIV_RESET_POL	R/W		Polarity of the DCS reset
			1	Rising edge (Subclass 1)
			0	falling edge (Subclass 2)
0	DIV_RESET_SEL	R/W		DCS reset selection
			0	SYNCBP/N is used (Subclass2)
			1	SYSREFP/N is used (Subclass1)

[1] Local register

Table 33. TRANS_CFG register (address 00FFh) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	TRANS_DIS	R/W		disable transfer function
			0	**transfer function active**
			1	registers updated on a WRITE command
6	TRANSFER	R/W		updates the registers with the written settings
			0	**settings are stored**
			1	registers updated (autoclear)
5 to 0	-	-	-	not used

11.5.3.2 JESD204A/JESD204B control registers

Table 34. IP_STATUS register (address 0801h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	RXSYNC_ERR_FLG	R	0	RX synchronization error 0: no error 1: synchronization error has occurred
6 to 1	RESERVED[5:0]	R	000000	reserved
0	PLL_LOCK	R	0	JEDEC PLL lock 0: unlocked 1: locked

Table 35. IP_RESET register (address 0802h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W	0	software reset: All JESD subblocks and registers are reset
6 to 4	-	-	000	not used
3	ASSEMBLER_SW_RST	R/W	0	Only the RXSYNC_ERR_FLG register bit and the frame assembler subblock are reset
2 to 0	-	-	000	not used

Table 36. IP_CFG_SETUP register (address 0803h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3 to 0	CFG_SETUP[3:0]	R/W	****	see Table 38

Table 37. Serial frequency computation information

CFG_SETUP	ADC sampling frequency (Mbps)	Lane 0 serial frequency (Gbps)	Lane 1 serial frequency (Gbps)
0000	FS	20 × FS	20 × FS
0001	FS	40 × FS	0
0010	FS	0	40 × FS
0011	reserved		
0100	reserved		
0101	FS	20 × FS	0
0110	FS	0	20 × FS
0111	FS	20 × FS	0
1000	FS	0	20 × FS
1001	FS	10 × FS	10 × FS
1010	FS	10 × FS	10 × FS
1011	reserved		
1100	reserved		

Table 37. Serial frequency computation information

CFG_SETUP	ADC sampling frequency (Mbps)	Lane 0 serial frequency (Gbps)	Lane 1 serial frequency (Gbps)
1101	reserved		
1110	reserved		
1111	FS	0	0

Table 38. JESD204A/JESD204B configuration table

CFG_SETUP[3:0]		ADC[0]	ADC[1]	Lane 0	Lane 1	F[1]	HD[1]	K[1]	M[1]	L[1]	Comment	CS[1]	CF[1]	S[1]
0	0000	**ON**	**ON**	**ON**	**ON**	2	0	9	2	2	(F × K) ≥ 17	1	0	1
1	0001	**ON**	**ON**	**ON**	OFF	4	0	5	2	1	(F × K) ≥ 17	1	0	1
2	0010	**ON**	**ON**	OFF	**ON**	4	0	5	2	1	(F × K) ≥ 17	1	0	1
3	0011	reserved												
4	0100	reserved												
5	0101	**ON**	OFF	**ON**	OFF	2	0	9	1	1	(F × K) ≥ 17	1	0	1
6	0110	**ON**	OFF	OFF	**ON**	2	0	9	1	1	(F × K) ≥ 17	1	0	1
7	0111	OFF	**ON**	**ON**	OFF	2	0	9	1	1	(F × K) ≥ 17	1	0	1
8	1000	OFF	**ON**	OFF	**ON**	2	0	9	1	1	(F × K) ≥ 17	1	0	1
9	1001	**ON**	OFF	**ON**	**ON**	1	1	17	1	2	(F × K) ≥ 17	1	0	1
10	1010	OFF	ON	ON	ON	1	1	17	1	2	(F × K) ≥ 17	1	0	1
11	1011	reserved												
12	1100	reserved												
13	1101	reserved												
14	1110	reserved												
15	1111	OFF	OFF	OFF	OFF	2	0	9	2	2	chip power-down	1	0	1

[1] F: Octets per frame clock cycle
HD: High-density mode
K: Frame per multi-frame
M: Converters per device
L: Lane per converter device
CS: Number of control bits per conversion sample
CF: Control words per frame clock cycle and link
S: Number of samples transmitted per single converter per frame cycle

Table 39. IP_CTRL1 register (address 0805h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	RESERVED	R/W	0	reserved
6	TRISTATE_CFG_PAD	R/W	(1 > 0)	TriState configuration pad 0: CFG Pads in Output mode (debug feature) 1: CFG Pads in Input mode; operating at power-up (see Table 38)

Table 39. IP_CTRL1 register (address 0805h) bit description *…continued*

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
5	SYNC_POL	R/W	0	synchronization polarity 0: default synchronization polarity used (active LOW) 1: polarity inversion (active HIGH)
4	SYNC_SE	R/W	0	single-ended synchronization 0: differential synchronization 1: single-ended synchronization
3	EN_RXSYNC_ERR	R/W	1	error reporting using synchronization interface 0: disabled 1: enabled
2 to 0	RESERVED	R/W	001	reserved

Table 40. IP_CTRL2 register (address 0806h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	RESERVED	R/W	0000**	reserved
1	SWP_LANE_1_2	R/W	*	swap lanes: if set to logic 1 the lanes are swapped symmetrically (L0 ↔ L1, L1 ↔ L0)
0	SWP_ADC_0_1	R/W	*	if set to logic 1, ADC 0 and ADC1 are swapped at the input of the frame assembler

Table 41. IP_PRBS_CTRL register (address 080Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	RESERVED	-	000000	reserved
1 to 0	PRBS_TYPE[1:0]	R/W	00	defines the type of Pseudo-Random Binary Sequence (PRBS) generator to be used 00; PRBS-7; $1 + x^6 + x^1$ 10; PRBS-23; $1 + x^{18} + x^{23}$

Table 42. JESD204B_CTRL1 register (address 0810h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	LMFC_periodic_rst	R/W	0	defines the LMFC modes 0;LMFC reset is done once 1; LMFC reset is donce at each SYSREF or SYNC
6	LMFC_periodic_rst	R/W	0	enables the LMFC reset 0;LMFC reset is disabled 1; LMFC reset is enabled
5 to 0	-	-	00000	reserved

Table 43. JESD204B_CTRL2register (address 0811h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DCS_periodic_rst	R/W	0	defines the LMFC modes 0;DCS reset is done once 1; DCS reset is donce at each SYSREF or SYNC
6	DCS_periodic_rst	R/W	0	enables the LMFC reset 0;DCS reset is disabled 1; DCS reset is enabled
5 to 0	-	-	00000	reserved

Table 44. JESD204B_CTRL3 register (address 0812h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	reserved
3	sync_at_lmfc_en	R/W	0	define the relation between the SYNC and the LMFC 0;SYNC is fetched directely (JESD204A mode) 1; SYNC is taken at next LMFC boundary (Subclass 1 and Subclass 2)
2	-	-	0	reserved
1	sync_capture_path	R/W	0	SYNC mode 0;JESD204A mode 1; Subclass 1 and Subclass 2
0	-	-	0	reserved

Table 45. IP_DEBUG_OUT1 register (address 0816h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-	-	000000	not used
1 to 0	PATTERN_OUT[9:8]	R/W	10	2 most significant bits of output stage debug word (inserted just before serializer)

Table 46. IP_DEBUG_OUT2 register (address 0817h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	PATTERN_OUT[7:0]	R/W	1010 1010	8 least significant bits of output stage debug word (inserted just before serializer)

Table 47. IP_DEBUG_IN1 register (address 0818h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	PATTERN_IN[15:8]	R/W	1010 1010	8 most significant bits of input stage debug word (inserted in place of ADC data)

Table 48. IP_DEBUG_IN2 register (address 0819h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	PATTERN_IN[7:0]	R/W	0000 0010	8 least significant bits of input stage debug word (inserted in place of ADC data)

Table 49. IP_TESTMODE register (address 081Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	RESERVED	R/W	0	reserved
6	LOOP_ALIGN	R/W	*[1]	ILA sequence is repeated infinitely
5	DIS_REPL_CHAR	R/W	0	no replacement character is placed in the data flow
4	BYP_ALIGN	R/W	0	ILA is bypassed
3 to 0	RESERVED	R/W	0000	reserved

[1] ILA = Initial Lane Alignment Sequence (see JESD204 JEDEC standard).

Table 50. IP_EXPERT_DOOR register (address 081Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	KEY[7:0]	R/W	0000 0000	8-bit key to enable Write access for JESD204 control register

Table 51. SYSREF_CFG register (address 081Eh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	RESERVED	R/W	0000	reserved
3	SYSREF_EN	R/W	0	1 : Enable SYSREFP/N path 0 : Disable SYSREFP/N path
2	SYSREF_SE			1 : SYSREFP is used as single ended SYSREF input 0 : SYSREFP/SYREFN are used as differential pair
1 to 0	RESERVED	R/W	00	reserved

Table 52. CFG_3_SCR_L register (address 0822h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SCR[0]	R/W	0	scrambling enabler
6 to 1	RESERVED	R/W	000000	reserved
0	L[0]	R/W	0	lanes number minus 1 (for example, for two lanes L = 1) 0x4A must be written in the IP_EXPERT_DOOR registers to obtain write access to this register

Table 53. IP_OUTBUF00_SWING register (address 086Bh) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	RESERVED[4:0]	R/W	00000	reserved
2 to 0	SWING[2:0]	R/W		Configurable lane 0 output current
			000	12 mA; ±300 mV (p-p)
			001	14 mA; ±350 mV (p-p)
			010	16 mA; ±400 mV (p-p)
			011	18 mA; ±450 mV (p-p)
			100	20 mA; ±500 mV (p-p)
			101	**22 mA; ±550 mV (p-p)**
			110	24 mA; ±600 mV (p-p)
			111	26 mA; ±650 mV (p-p)

Table 54. IP_OUTBUF01_SWING register (address 086Ch) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	RESERVED[4:0]	R/W	00000	reserved
2 to 0	SWING[2:0]	R/W		Configurable lane 1 output current
			000	12 mA; ±300 mV (p-p)
			001	14 mA; ±350 mV (p-p)
			010	16 mA; ±400 mV (p-p)
			011	18 mA; ±450 mV (p-p)
			100	20 mA; ±500 mV (p-p)
			101	**22 mA; ±550 mV (p-p)**
			110	24 mA; ±600 mV (p-p)
			111	26 mA; ±650 mV (p-p)

Table 55. IP_LANE00_0_CTRL register (address 0871h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	RESERVED[2:0]	R/W	000	reserved
4 to 3	LANE_MODE[1:0]	R/W	00	debug option directly before serializer
				0: normal mode, ADC path
				1: toggle (0/1 toggle sent over the lanes)
				2: A constant (value in IP_DEBUG_OUT) is sent over the lanes
				3: PRBS polynom is sent over the lane
2	LANE_POL	R/W	0	if set to logic 1, lane P/N polarity is inverted
1	RESERVED	R/W	0	reserved
0	LANE_PD	R/W	*	if set to logic 1, lane enters power-down

Table 56. IP_LANE01_0_CTRL register (address 0872h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	RESERVED[2:0]	R/W	000	reserved
4 to 3	LANE_MODE[1:0]	R/W	00	debug option directly before serializer 0: normal mode, ADC path 1: toggle (0/1 toggle sent over the lanes) 2: A constant (value in IP_DEBUG_OUT) is sent over the lanes 3: PRBS polynom is sent over the lane
2	LANE_POL	R/W	0	if set to logic 1, lane P/N polarity is inverted
1	RESERVED	R/W	0	reserved
0	LANE_PD	R/W	*	if set to logic 1, lane enters power-down

Table 57. IP_ADC00_0_CTRL register (address 0890h) bit description
Default settings are shown highlighted.

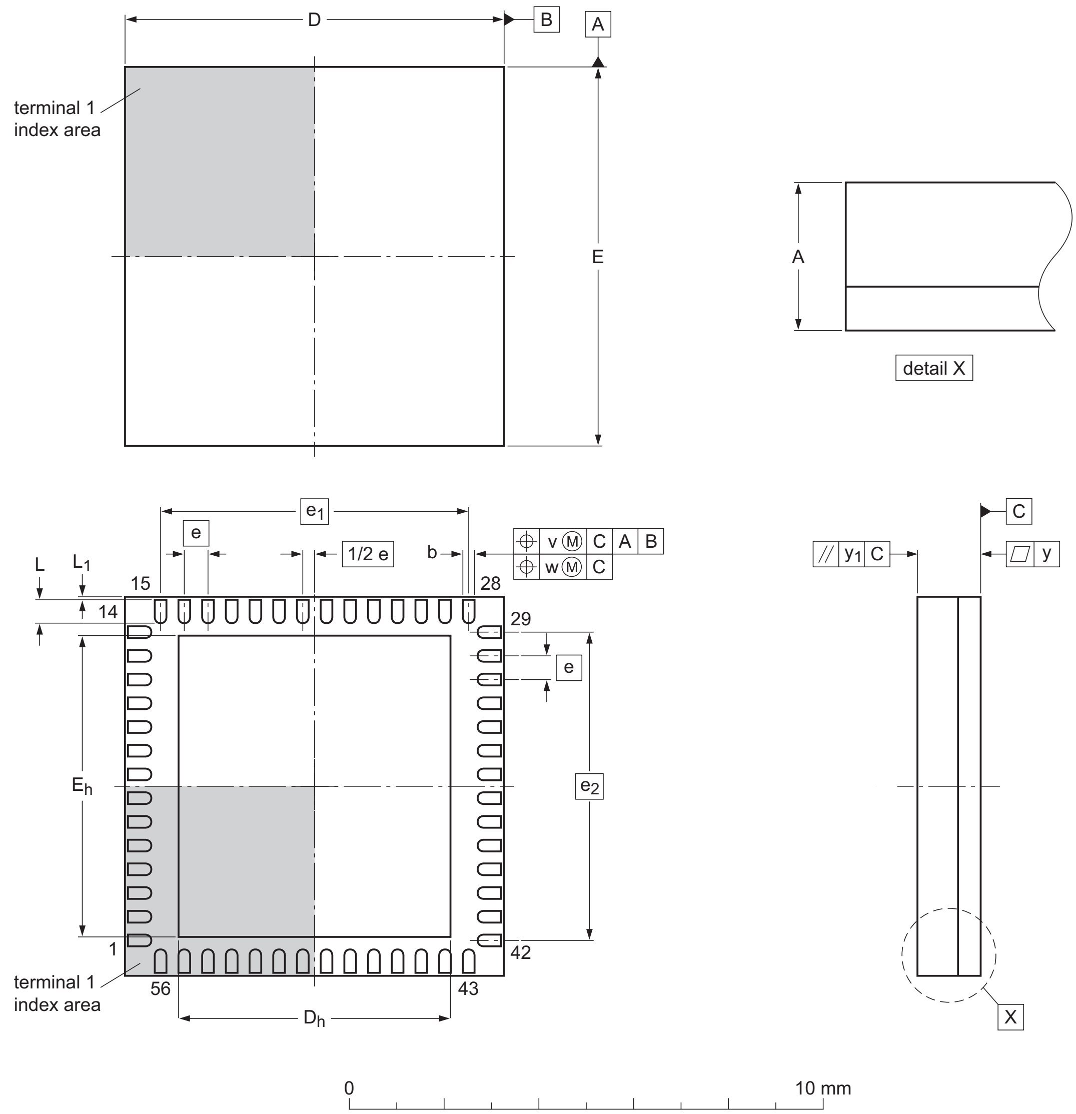
Bit	Symbol	Access	Value	Description
7 to 6	RESERVED	R/W	00	reserved
5 to 4	ADC_MODE[1:0]	R/W	00	debug option to replace ADC core 0, 1: normal mode, ADC path 2: a constant (value in IP_Debug_in) is sent instead of ADC conversion output 3: PRBS polynom is sent instead of ADC
3 to 1	RESERVED	R/W	000	reserved
0	ADC_PD	R/W	0	if set to logic 1, ADC enters power-down

Table 58. IP_ADC01_0_CTRL register (address 0891h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	RESERVED	R/W	00	reserved
5 to 4	ADC_MODE[1:0]	R/W	00	debug option to replace ADC core 0, 1: normal mode, ADC path 2: a constant (value in IP_Debug_in) is sent instead of ADC conversion output 3: PRBS polynom is sent instead of ADC
3 to 1	RESERVED	R/W	000	reserved
0	ADC_PD	R/W	0	if set to logic 1, ADC enters power-down

12. Package outline

HLQFN56R: plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 x 8 x 1.35 mm **SOT935-2**



Dimensions

Unit		A	b	D	D_h	E	E_h	e	e_1	e_2	L	L_1	v	w	y	y_1
	max	1.40	0.30	8.1	5.85	8.1	6.45				0.55	0.10				
mm	nom	1.35	0.25	8.0	5.80	8.0	6.40	0.5	6.5	6.5	0.50	0.05	0.1	0.05	0.05	0.1
	min	1.25	0.20	7.9	5.75	7.9	6.35				0.45	0.00				

sot935-2_po

Outline version	References IEC	References JEDEC	References JEITA		European projection	Issue date
SOT935-2						~~11-08-16~~ 11-08-18

Fig 40. Package outline SOT935-2 (HLQFN56)

13. Abbreviations

Table 59. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
CDMA	Code Division Multiple Access
DAV	DAta Valid
ESD	ElectroStatic Discharge
FFT	Fast Fourier Transform
GSM	Global System for Mobile communications
ILA	Initial Lane Alignment
IMD3	third order InterMoDulation product
LSB	Least Significant Bit
LTE	Long-Term Evolution
LVDS DDR	Low Voltage Differential Signaling Double Data Rate
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
MIMO	Multiple Input Multiple Output
MSB	Most Significant Bit
OTR	OuT-of-Range
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
SNR	Signal-to-Noise Ratio
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide interoperability for Microwave Access

14. Revision history

Table 60. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1443D_SER v.3.4	20121010	Data sheet	-	ADC1443D_SER v.3.3
ADC1443D_SER v.3.3	20120926	Objective data sheet	-	ADC1443D_SER v.3.2
ADC1443D_SER v.3.2	20120918	Objective data sheet	-	ADC1443D_SER v.3.1
ADC1443D_SER v.3.1	20120911	Objective data sheet	-	ADC1443D_SER v.3.0
ADC1443D_SER v.3.0	<tbd>	Objective data sheet	-	ADC1443D_SER v.2.0
Modifications:	• Text and drawings updated throughout entire data sheet.			
ADC1443D_SER v.2.0	20120630	Objective data sheet	-	ADC1443D_SER v.1.1
ADC1443_SER v.1.1	20110928	Objective data sheet	-	ADC1443D_SER v.1
ADC1443D_SER v.1	20110901	Objective data sheet	-	-

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15. Contents

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