Ultra-Low On-Resistance, 6A Dual Load Switch with Soft Start

Features

- **16mΩ(Typical) On-resistance per Channel**
- **6A Continuous Current**
- **Soft Start Time Programmable by External Capacitor**
- **Wide Input Voltage Range (VIN): 0.8V to 5.5V**
- **Supply Voltage Range (VBIAS): 3V to 5.5V**
- **Output Discharge when Switch Disabled**
- **Reverse Current Blocking when Switch Disabled**
- **Over-Temperature Protection**
- **Enable Input**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APL3533 is an ultra-low on-resistance, dual power-distribution switch with external soft start control. It integrates two N-channel MOSFETs that can deliver 6A continuous load current each.

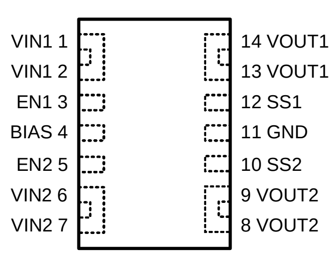
The device integrates over-temperature protection. The over temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 160°C and will automatically turns on the power switch when the temperature drops by 40°C.

The device is available in lead free TDFN2x3-14A packages.

Applications

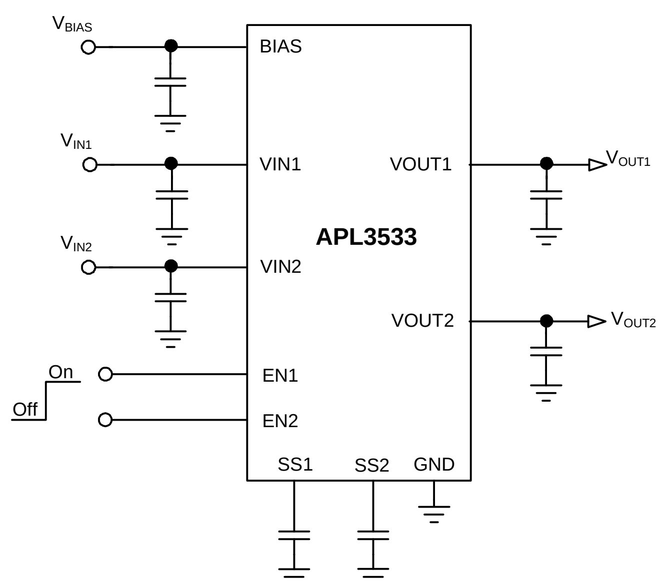
- **Notebook**
- **AIO PC**

Pin Configurations



TDFN2x3-14A
(Top View)

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL3533 □□-□□□ (Assembly Material; Handling Code; TemperatureRange; Package Code)	Package Code QB : TDFN2x3-14A Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3533 QB: L3533 XXXXX	XXXXX-Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{BIAS}	BAIS to GND Voltage	-0.3 ~ 6	V
V_{IN1}, V_{IN2}	VIN1, VIN2 to GND Voltage	-0.3 ~ 6	V
V_{OUT1}, V_{OUT2}	VOUT1, VOUT2 to GND Voltage	-0.3 ~ 6	V
V_{EN1}, V_{EN2}	EN1, EN2 to GND Voltage	-0.3 ~ 6	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)	80	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{BIAS}	BIAS Input Voltage	3.0 ~ 5.5	V
V_{IN1}, V_{IN2}	VIN1, VIN2 Input Voltage	0.8 ~ 5.5	V
I_{OUT}	VOUT1 or VOUT2 Output Current (single channel)	0 ~ 6	A
P_D	Maximum Power Dissipation, T_A=50°C (Note4)	0.94	W
V_{IH}	EN1, EN2 Logic High Input Voltage	1.2 ~ 5.5	V
V_{IL}	EN1, EN2 Logic Low Input Voltage	0 ~ 0.4	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Note 4 : Refer to the thermal consideration on page 15.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN1}= V_{IN2}= 0.8V~5.5V, V_{EN1}= V_{EN2}=V_{BIAS} =5V and T_A= -40~85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3533			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{BIAS}	BIAS Supply Current (both channels)	No load, V_{BIAS}=5V =$V_{EN1,2}$=5V	-	60	90	μA
	BIAS Supply Current (single channel)	No load, V_{BIAS}=5V, V_{EN1}=5V, V_{EN2}=0V	-	50	-	μA
I_{SD}	BIAS Supply Current at Shutdown	No load, V_{BIAS}=5V, $V_{EN1,2}$=0V	-	-	2	μA
I_{OFF}	VIN Off-State Supply Current (per channel)	No load, V_{BIAS}=5V, $V_{EN1,2}$=0V, $V_{IN1,2}$=5V	-	0.1	8	μA
		No load, V_{BIAS}=5V, $V_{EN1,2}$=0V, $V_{IN1,2}$=3.3V	-	0.1	3	μA
		No load, V_{BIAS}=5V, $V_{EN1,2}$=0V, $V_{IN1,2}$=1.8V	-	0.1	2	μA
		No load, V_{BIAS}=5V, $V_{EN1,2}$=0V, $V_{IN1,2}$=0.8V	-	0.1	1	μA
	Reverse Leakage Current (per channel)	$V_{EN1,2}$=0V, $V_{IN1,2}$=0V	-	0.1	16	μA
UNDER-VOLTAGE LOCKOUT (UVLO)						
	Rising BIAS UVLO Threshold	V_{BIAS} rising	1.9	2.4	2.9	V
	BIAS UVLO Hysteresis		-	0.1	-	V
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	I_{OUT}=200mA, T_J= 25°C, Channel 1	-	16	18	mΩ
		I_{OUT}=200mA, T_J= -40~125°C, Channel 1	-	-	24	mΩ
		I_{OUT}=200mA, T_J= 25°C, Channel 2	-	16	18	mΩ
		I_{OUT}=200mA, T_J= -40~125°C, Channel 2	-	-	24	mΩ
	VOUT Discharge Resistance	$V_{EN1,2}$=0V, VOUT1 or VOUT2 force 1V	-	150	180	Ω

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN1}= V_{IN2}= 0.8V~5.5V, V_{EN1}= V_{EN2}=V_{BIAS} =5V and T_A= -40~85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3533			Unit
			Min.	Typ.	Max.	
SOFT-START CONTROL PIN						
	SS Discharge Current	$V_{SS1,2}$=6V, $V_{EN1,2}$=0V, EN2=low, measured at SS1 or SS2	-	560	-	μA
EN INPUT PIN						
	Input Logic High		1.2	-	-	V
	Input Logic Low		-	-	0.4	V
	Input Current		-	-	1	μA
OVERT-TEMPERATURE PROTECTION (OTP)						
	Over-Temperature Threshold	T_J rising	-	160	-	°C
	Over-Temperature Hysteresis		-	40	-	°C

Timing Chart

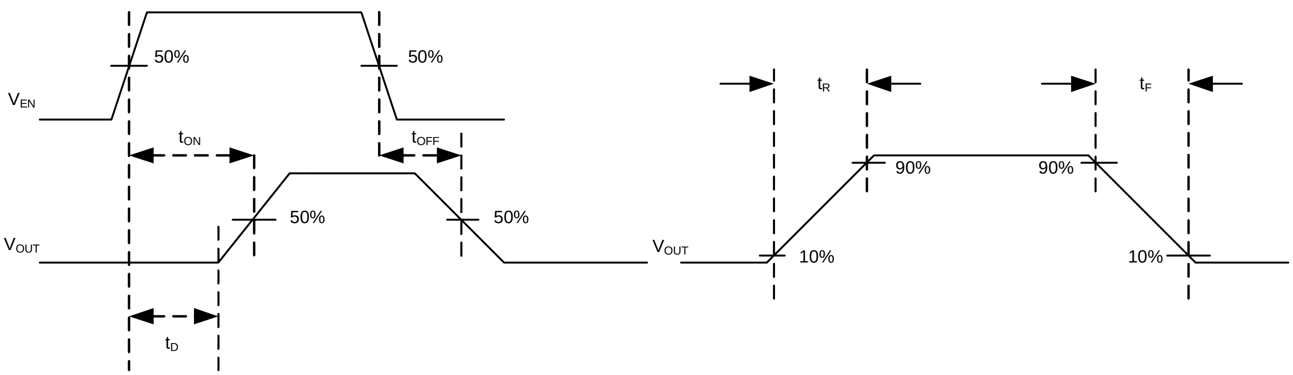
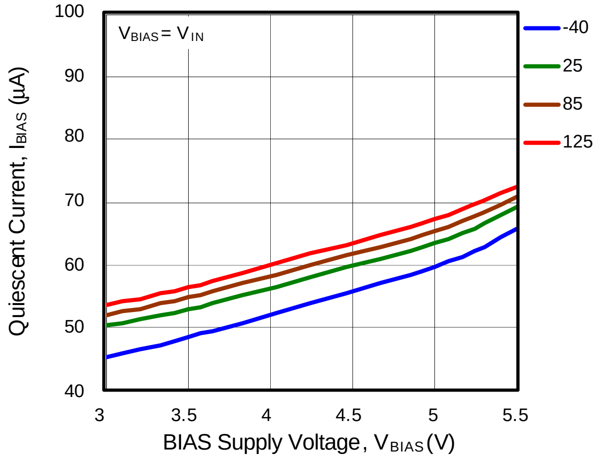


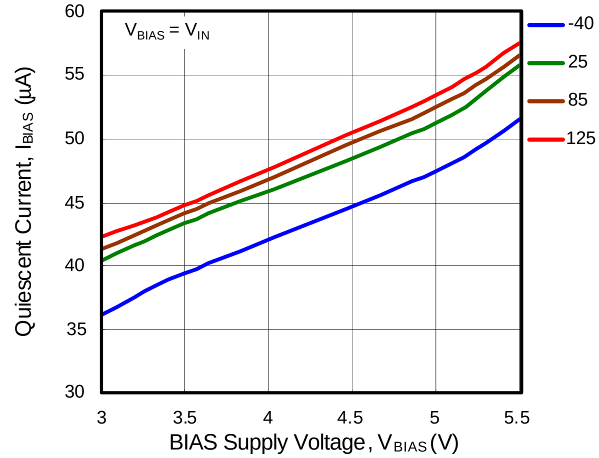
Figure 1. t_{ON}/t_{OFF}, t_R/t_F Waveforms

Typical Operating Characteristics

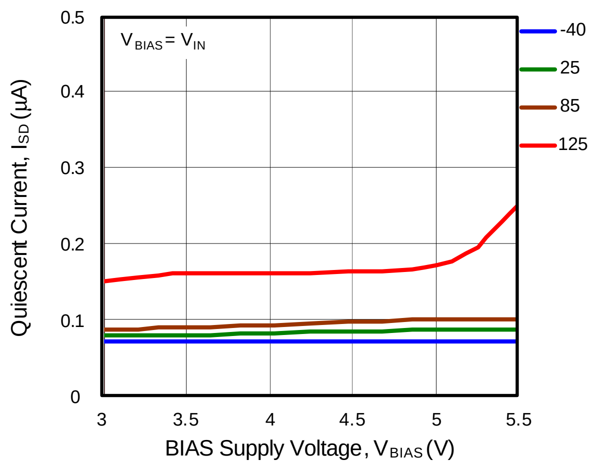
Quiescent Current vs. BIAS Supply Voltage (Both Channels)



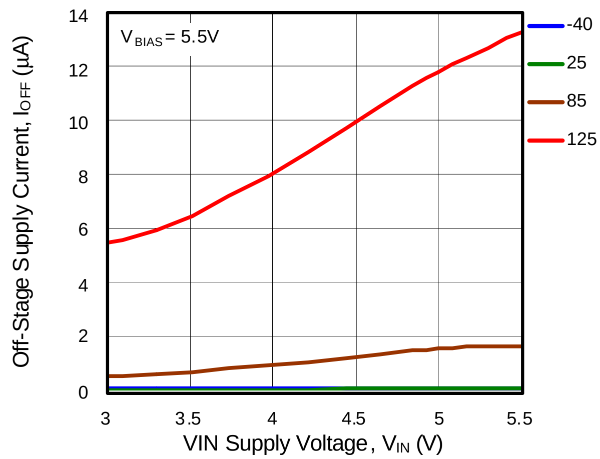
Quiescent Current vs. BIAS Supply Voltage (Single Channel)



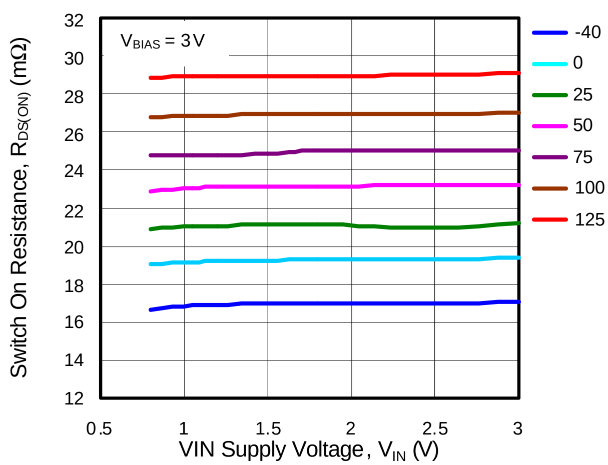
Shutdown Current vs. BIAS Supply Voltage (Both Channels)



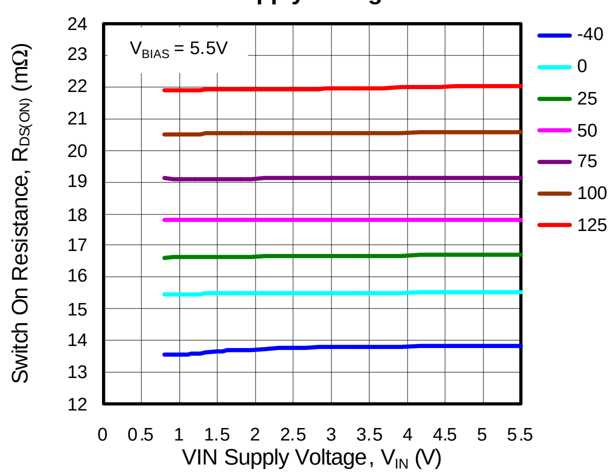
Off-Stage Supply Current vs. VIN Supply Voltage (SINGLE CHANNEL)



Switch On Resistance vs. VIN Supply Voltage

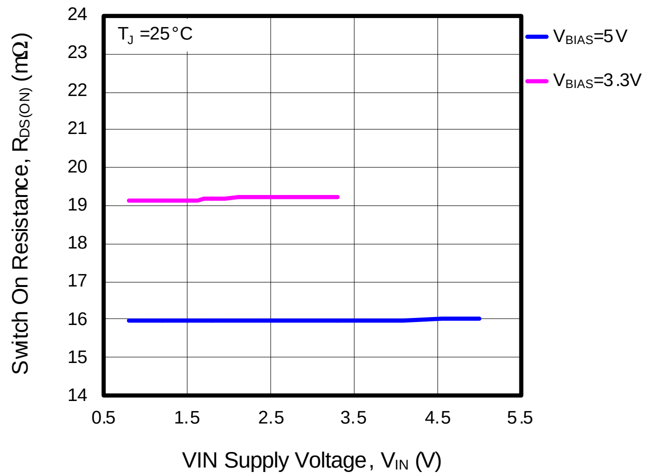


Switch On Resistance vs. VIN Supply Voltage

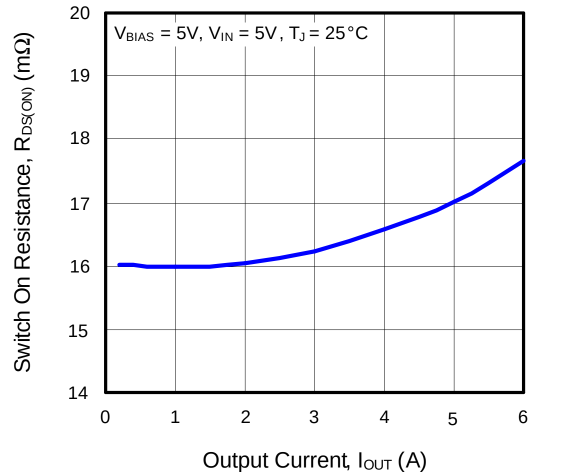


Typical Operating Characteristics

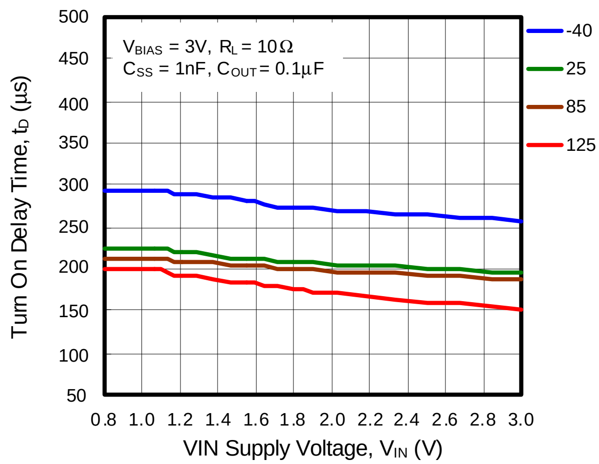
Switch On Resistance vs. VIN Supply Voltage



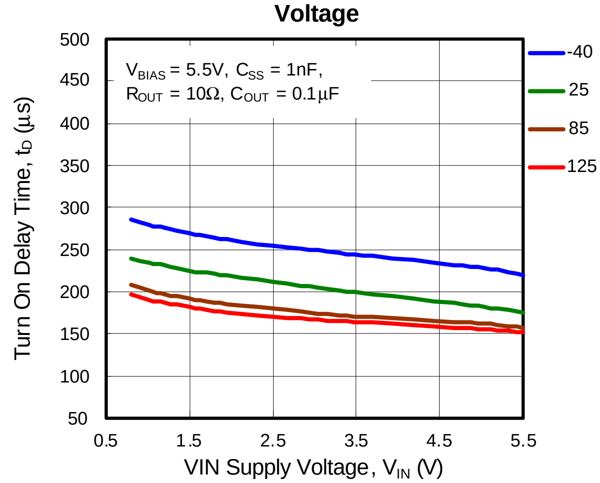
Switch On Resistance vs. Output Current



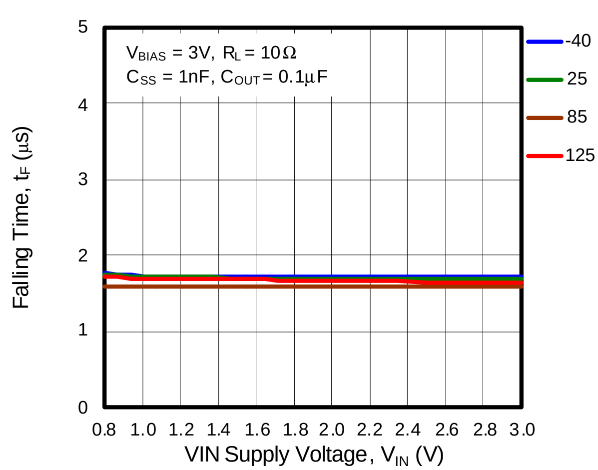
Turn On Delay Time vs. VIN Supply Voltage



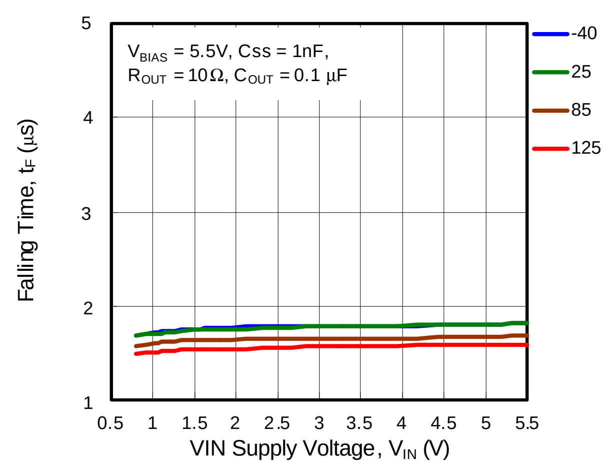
Turn On Delay Time vs. VIN Supply Voltage



Falling Time vs. VIN Supply Voltage

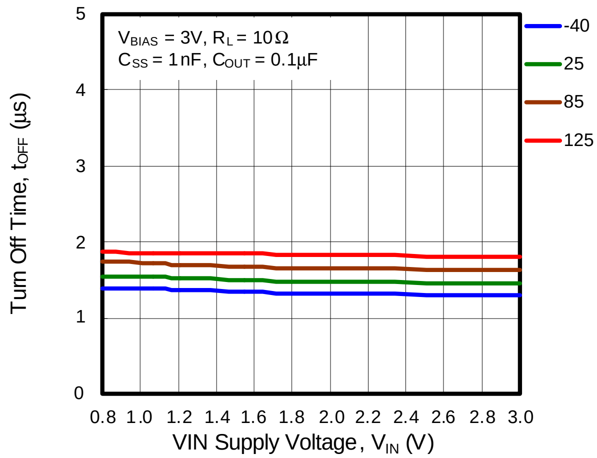


Falling Time vs. VIN Supply Voltage

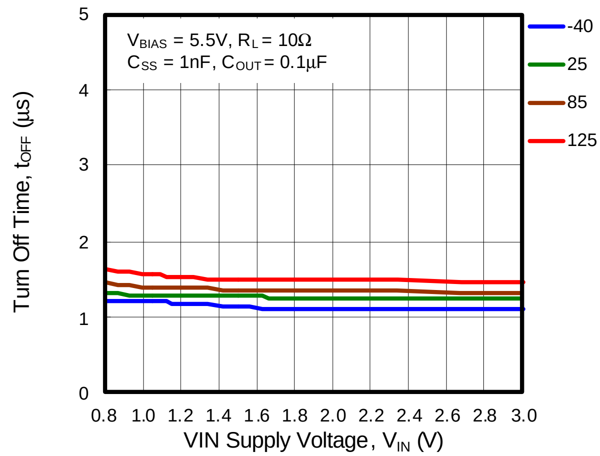


Typical Operating Characteristics

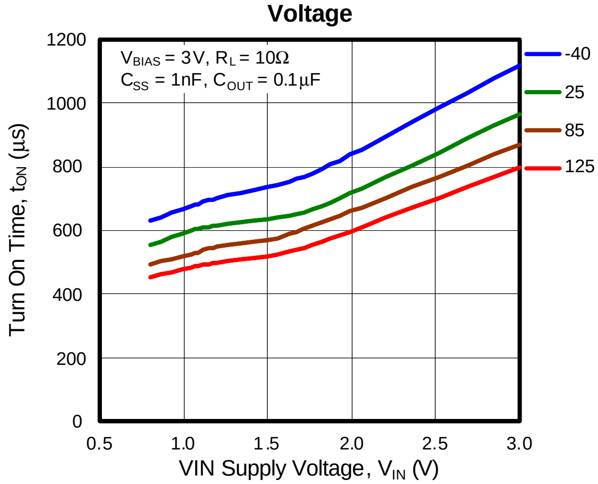
Turn Off Time vs. VIN Supply Voltage



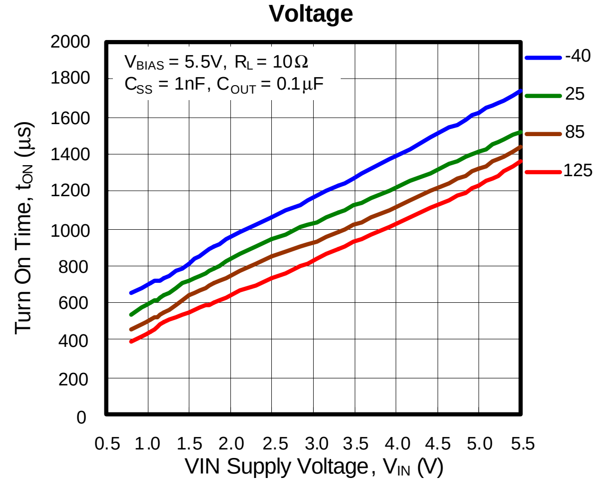
Turn Off Time vs. VIN Supply Voltage



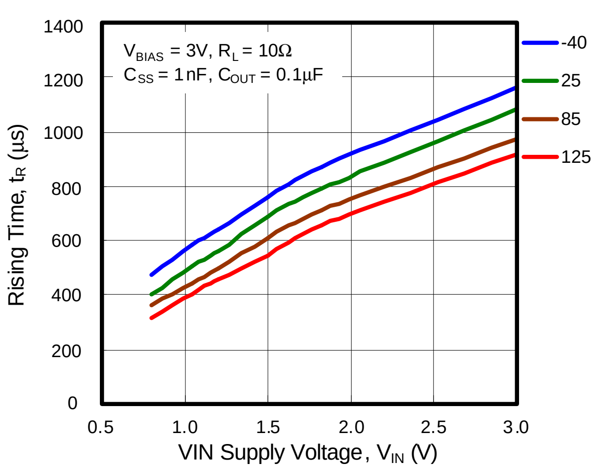
Turn On Time vs. VIN Supply Voltage



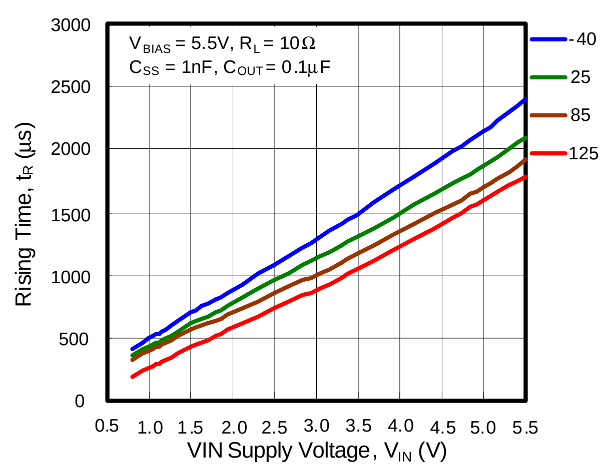
Turn On Time vs. VIN Supply Voltage



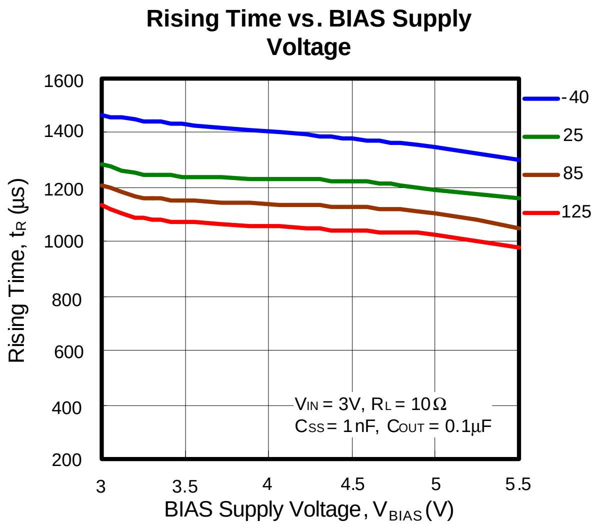
Rising Time vs. VIN Supply Voltage



Rising Time vs. VIN Supply Voltage



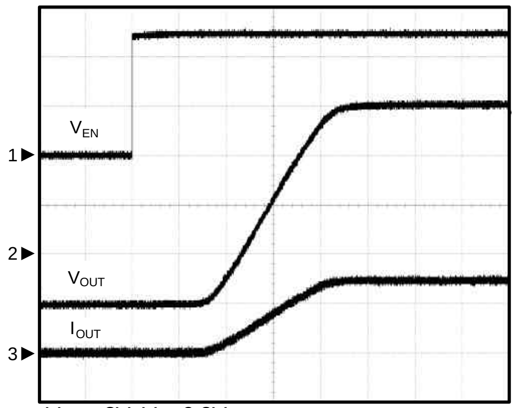
Typical Operating Characteristics



Operating Waveforms

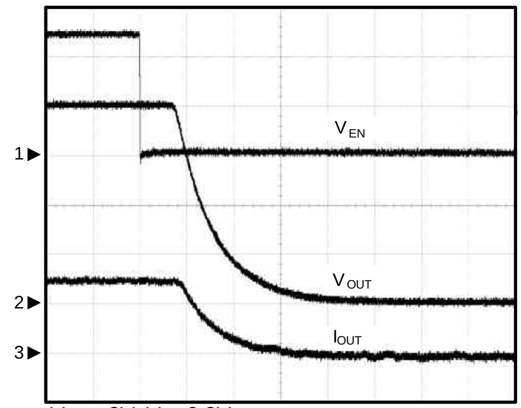
Refer to the typical application circuit. T_A= 25°C unless otherwise specified.

Enable



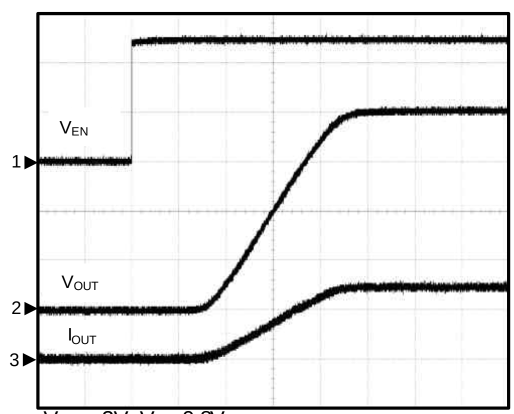
V_{BIAS}=3V, V_{IN}=0.8V
C_{OUT}=0.1µF, C_{SS}=1nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 200mV/Div, DC
CH3: I_{OUT}, 50mA/Div, DC
TIME: 200µs/Div

Shutdown



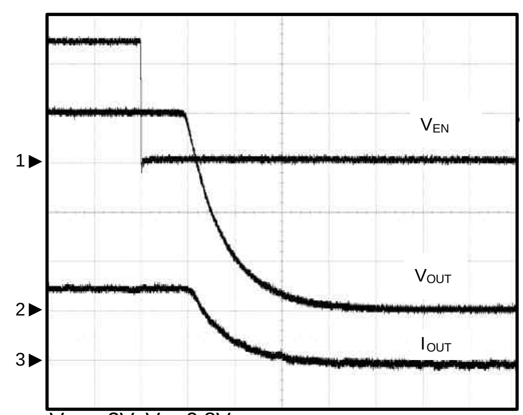
V_{BIAS}=3V, V_{IN}=0.8V
C_{OUT}=0.1µF, C_{SS}=1nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 200mV/Div, DC
CH3: I_{OUT}, 50mA/Div, DC
TIME: 1µs/Div

Enable



V_{BIAS}=3V, V_{IN}=0.8V
C_{OUT}=0.1µF, C_{SS}=1nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 200mV/Div, DC
CH3: I_{OUT}, 50mA/Div, DC
TIME: 200µs/Div

Shutdown

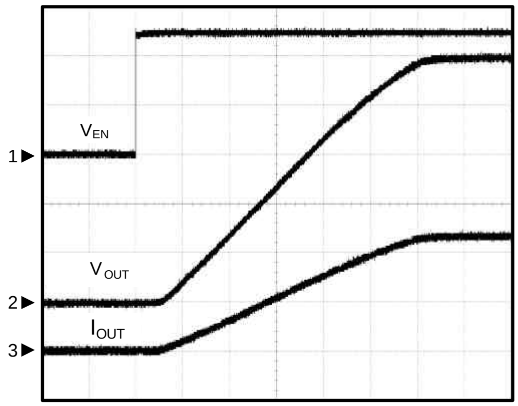


V_{BIAS}=3V, V_{IN}=0.8V
C_{OUT}=0.1µF, C_{SS}=1nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 200mV/Div, DC
CH3: I_{OUT}, 50mA/Div, DC
TIME: 1µs/Div

Operating Waveforms

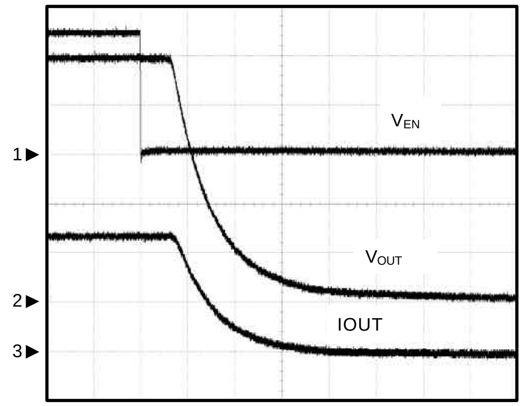
Refer to the typical application circuit. T_A= 25°C unless otherwise specified.

Enable



V_{BIAS}=5V, V_{IN}=5V
C_{OUT}=0.1μF, C_{SS}=1nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: I_{OUT}, 200mA/Div, DC
TIME: 500μs/Div

Shutdown

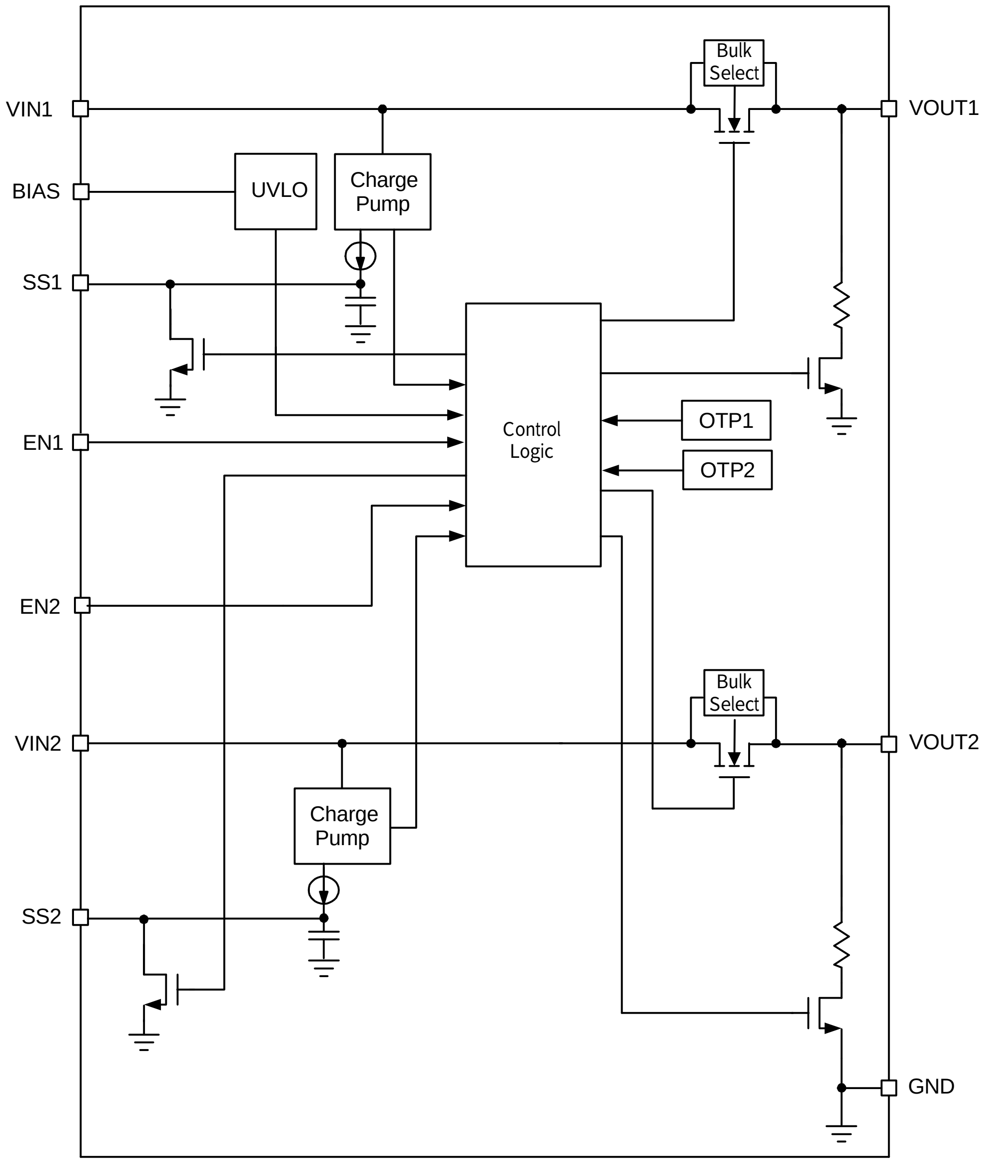


V_{BIAS}=5V, V_{IN}=5V
C_{OUT}=0.1μF, C_{SS}=1nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: I_{OUT}, 200mA/Div, DC

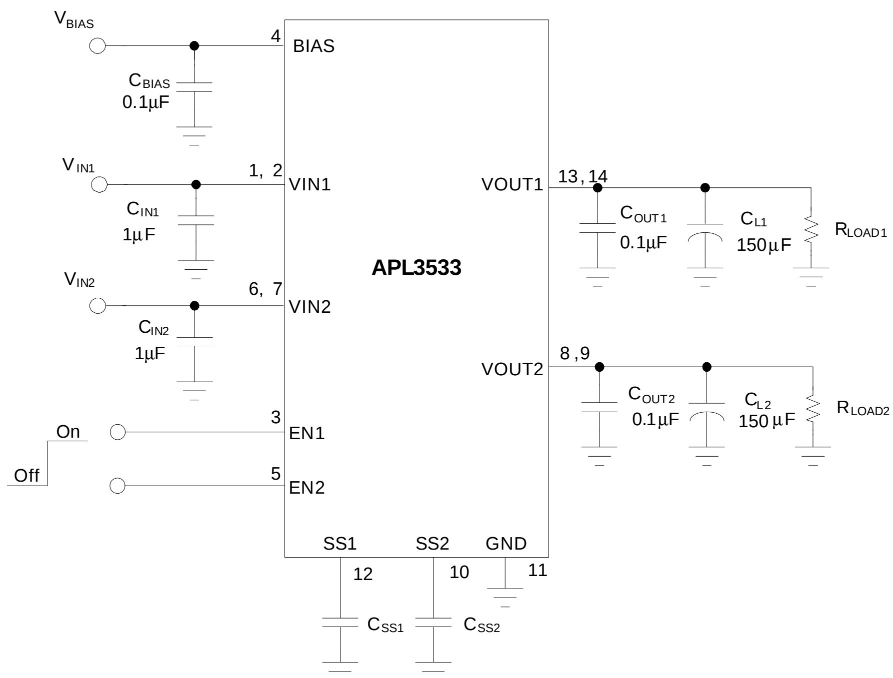
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VIN1	Power supply Input of switch 1. Connect this pin to an external DC supply.
2	VIN1	
3	EN1	Enable input of switch 1. Logic high turns on switch 1. The EN1 pin cannot be left floating.
4	BIAS	Bias voltage input pin for internal control circuitry.
5	EN2	Enable input of switch 2. Logic high turns on switch 2. The EN2 pin cannot be left floating.
6	VIN2	Power supply Input of switch 2. Connect this pin to an external DC supply.
7	VIN2	
8	VOUT2	Switch 2 output.
9	VOUT2	
10	SS2	Soft start control of switch 2. A capacitor from this pin to ground sets the VOUT2's rise slew rate.
11	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
12	SS1	Soft start control of switch 1. A capacitor from this pin to ground sets the VOUT1's rise slew rate.
13	VOUT1	Switch 1 output.
14	VOUT1	

Block Diagram



Typical Application Circuit



C_{SS}(pF)	Soft-Start Time (ms) 10% to 90%, V_{BIAS}=5V, C_L=0.1mF, C_{IN}=1mF, R_L=10W, Typical values are at T_A=25°C						
	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=1.8V	V_{IN}=1.5V	V_{IN}=1.2V	V_{IN}=1.05V	V_{IN}=0.8V
0	112	73	53	49	45	42	38
220	492	322	197	170	146	132	128
330	685	450	270	230	198	180	145
470	911	598	355	307	263	233	188
1000	2030	1280	749	635	538	470	388
2200	4360	2740	1574	1336	1118	1014	797
4700	8780	5540	3218	2696	2289	2037	1624
10000	19060	12011	6862	5700	4806	4301	3410

Note: The table Contains soft-start time values measured on a typical device. The soft-start times shown are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and EN pin is asserted high.

Function Description

VIN Under-voltage Lockout (UVLO)

A under-voltage lockout (UVLO) circuit monitors the VBIAS pins voltage to prevent wrong logic controls. The UVLO function initiates a soft-start process after the BIAS supply voltages exceed rising UVLO voltage threshold during powering on.

Power Switch

The power switch is an N-channel MOSFET with a ultra-low $R_{DS(ON)}$. When IC is in shutdown state ($V_{EN1,2}$=0V), the MOSFET prevents a reverse current flowing from the VOUT back to VIN. When IC is in UVLO state, the internal parasitic diodes connected from VOUT to VIN will be forward biased.

Soft-start

The APL3533 Provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the SS pin to the ground.

Enable Control

The APL3533 has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle.

Over-Temperature Protection (OTP)

When the junction temperature exceeds 160°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 40°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Power Sequencing

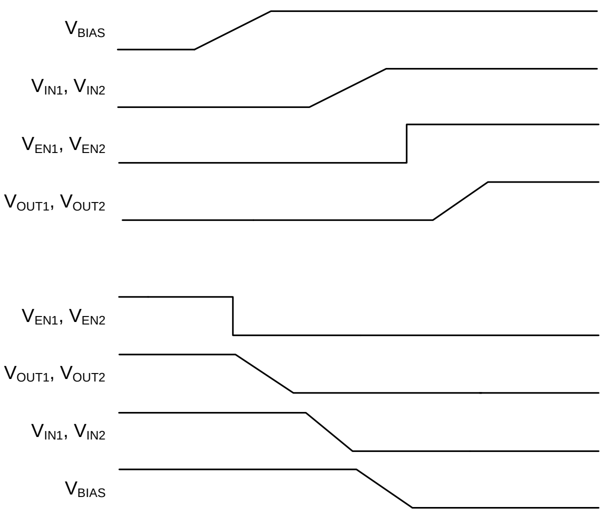


Figure 2. APL3533 Power Sequencing Diagram

The APL3533 has a built-in reverse current blocking circuit to prevent a reverse current flowing through the body diode of power switch from the VOUT back VIN pin when power switch disabled. The reverse current blocking circuit is not active before V_{BIAS} is ready. When IC is in UVLO state, the internal parasitic diodes of power switch connected from VOUT to VIN will be forward biased. Otherwise, VOUT should not be higher than VBIAS, and VBIAS must be higher than the voltage of any other input pin, the reason is that the internal parasitic diodes connected from VOUT to VBIAS will be forward biased.

Capacitor Selection

The APL3533 requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance.

For normal applications (except OTP or output short circuit has occurred), the recommended input capacitance of VIN is 1µF and output capacitance of VOUT is 0.1µF at least. Please place the capacitors near the APL3533 as close as possible.

A bulk output capacitor, placed close to the load, is recommended to support load transient current.

Soft-Start Capacitor

The soft-start capacitor on SS pin can reduce the inrush current and overshoot of output voltage. The capacitor is charge to V_{SS} with a constant current source. This results in a linear charge of the soft-start capacitor and thus the output voltage.

Thermal Consideration

The APL3533 maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air. Assuming the T_A=25°C and maximum T_J=160°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)}=(160-25)/80$$
$$= 1.68(W)$$

For normal operation, do not exceed the maximum operating junction temperature of T_J = 125°C. The calculated power dissipation should be less than:

P_D =(125-25)/80

=1.25(W)..T_A=25°C

P_D =(125-85)/80

=0.5(W)..T_A=85°C

The power dissipation depends on operating ambient temperature for fixed T_J=125°C and thermal resistance θ_{JA}. For APL3533 packages, the Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

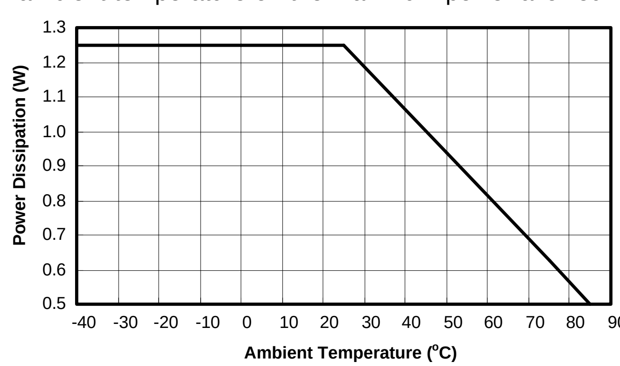


Figure 3. Derating Curves for APL3533 Package

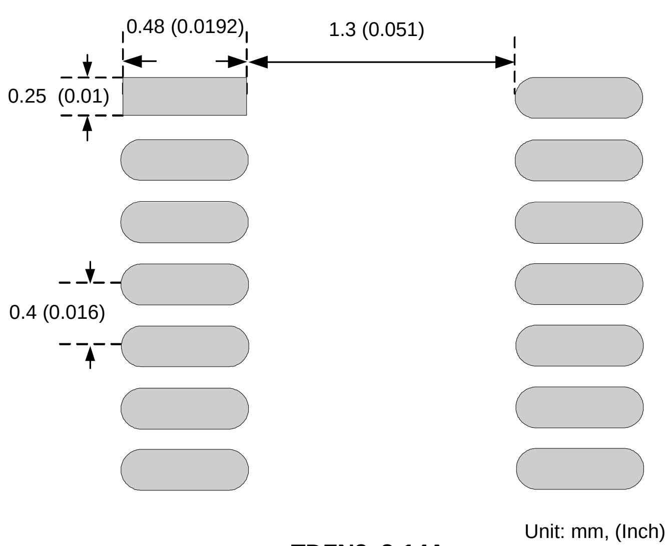
Application Information

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.
3. Locate APL3533 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep VIN and VOUT traces as wide and short as possible.

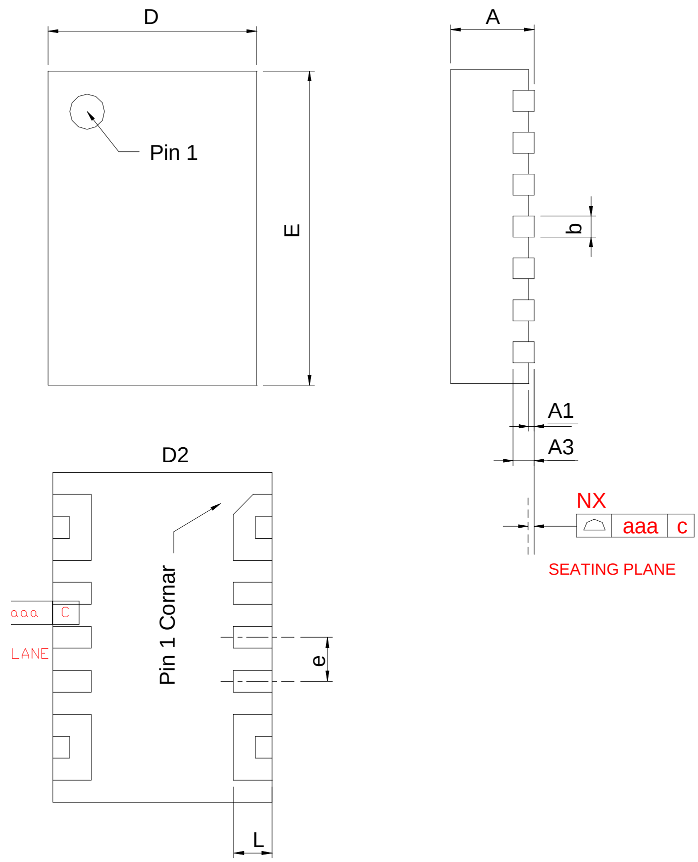
Recommended Minimum Footprint



TDFN2x3-14A

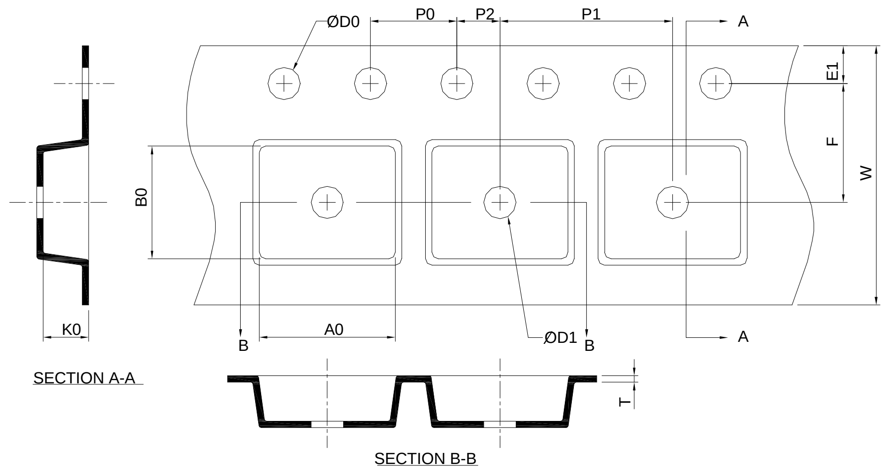
Package Information

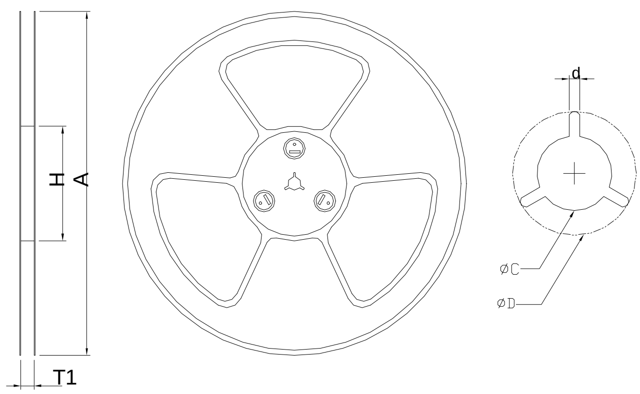
TDFN2x3-14A



SYMBOL	TDFN2x3-14A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.11 REF		0.004 REF	
b	0.15	0.25	0.006	0.010
D	1.90	2.10	0.075	0.083
E	2.90	3.10	0.114	0.122
e	0.40 BSC		0.016 BSC	
L	0.30	0.40	0.012	0.016
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TDFN2x3-14A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.25±0.05	2.30±0.20	3.30±0.20	1.00±0.20

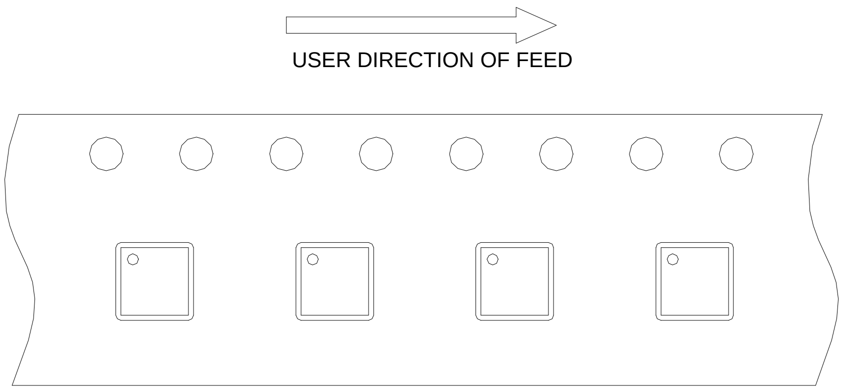
(mm)

Devices Per Unit

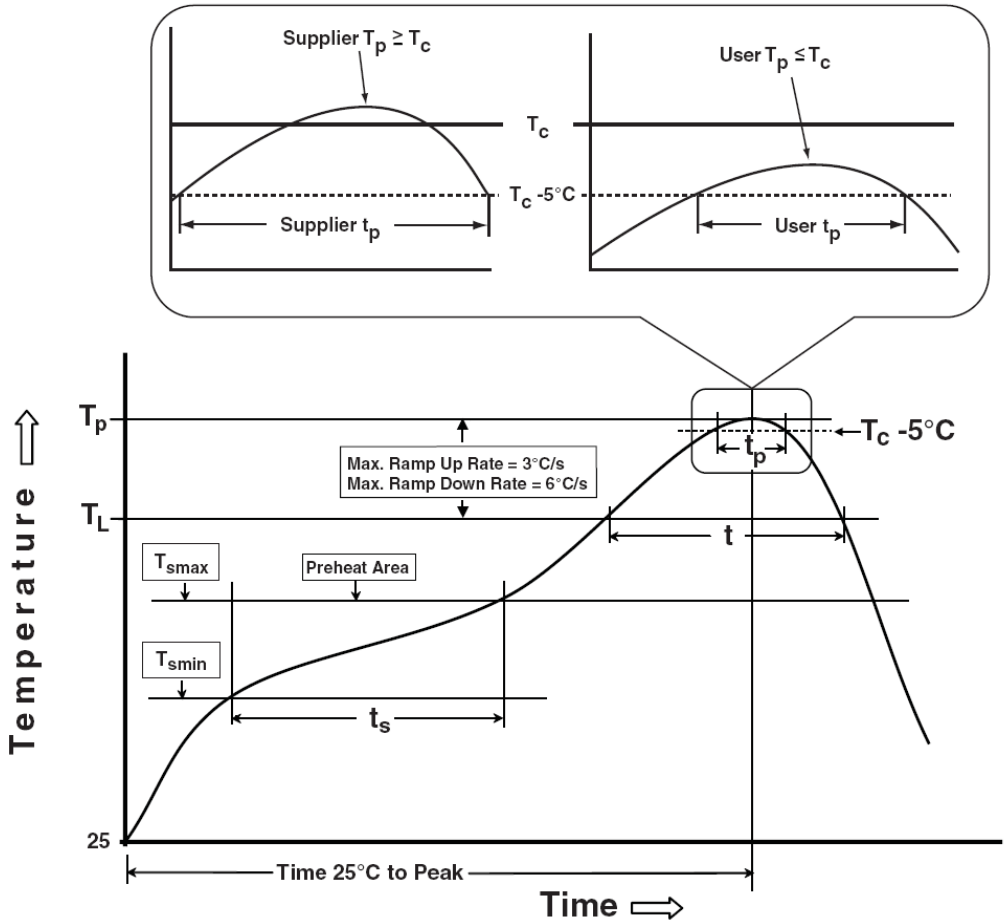
Package Type	Unit	Quantity
TDFN2x3-14A	Tape & Reel	3000

Taping Direction Information

TDFN2x3-14A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838