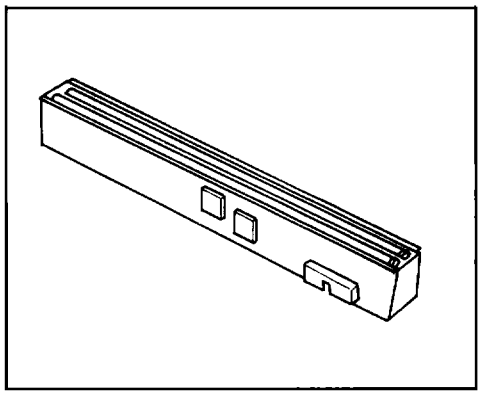
CIPS305MS5A

The CIPS 305MS5A is a contact type linear image sensor module. The device includes rod lens array, LED array and driving circuit. The device contains a row of 4678 photodiodes which provides 400 dots/ Inch resolution across A3 size (297mm) document. The CIPS 305MS5A remarkablely contributes to the realization of compact size copying machine and scanner.



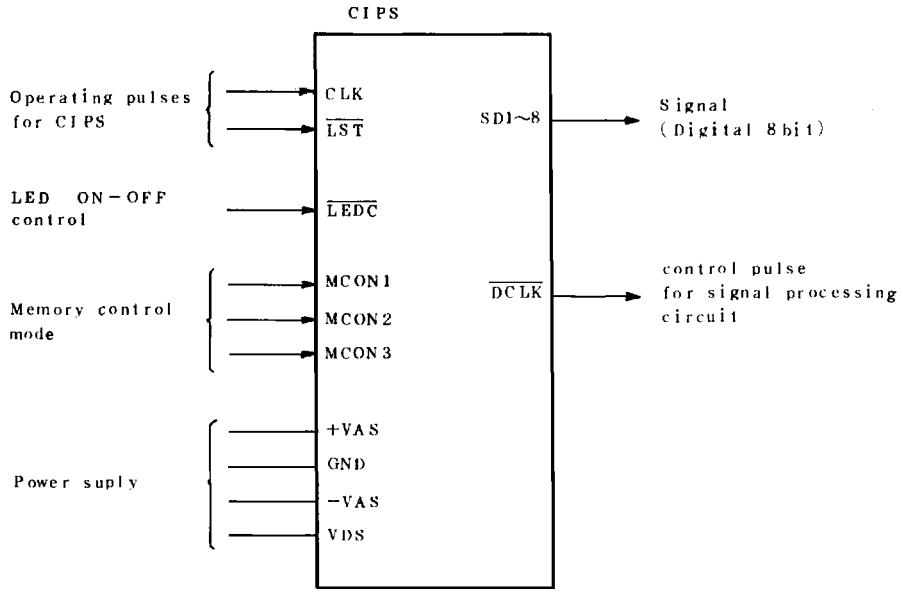
. Effective Sensing Lenght: 297mm
. resolution : 400 DPI
. sensor : TCD120AC
. Optical System : Rod lens Array (Depth of field: ±0.3mm)
. Illumination : Yellow-Green LED Array
. Signal output : Digital 8 bit

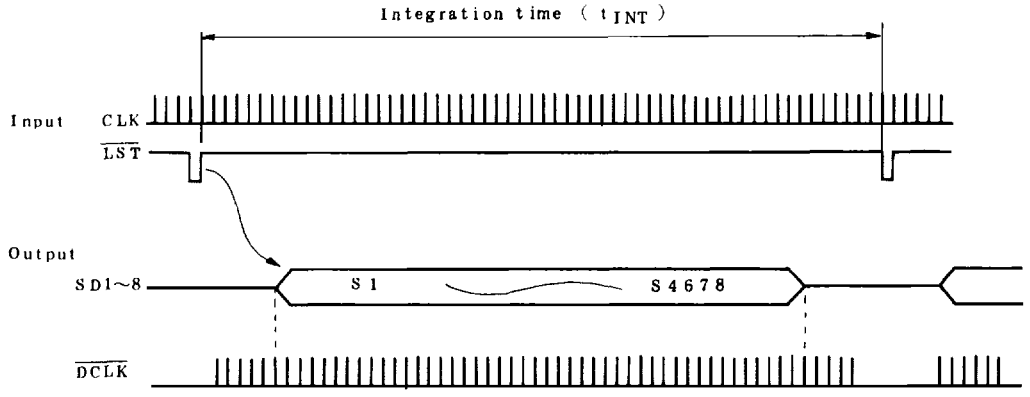
MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Digital Supply Voltage	V_{DS}	-0.5~7.0	V
Analog Supply Voltage	$+V_{AS}$	0~15.0	V
Analog Supply Voltage	$-V_{AS}$	-13~0	V
Input Pulse Voltage	V_{IN}	-0.5~V_{DS}+0.5	V
Operating Temperature	T_{opr}	0~50	°C
Storage Temperature	T_{stg}	-20~60	°C

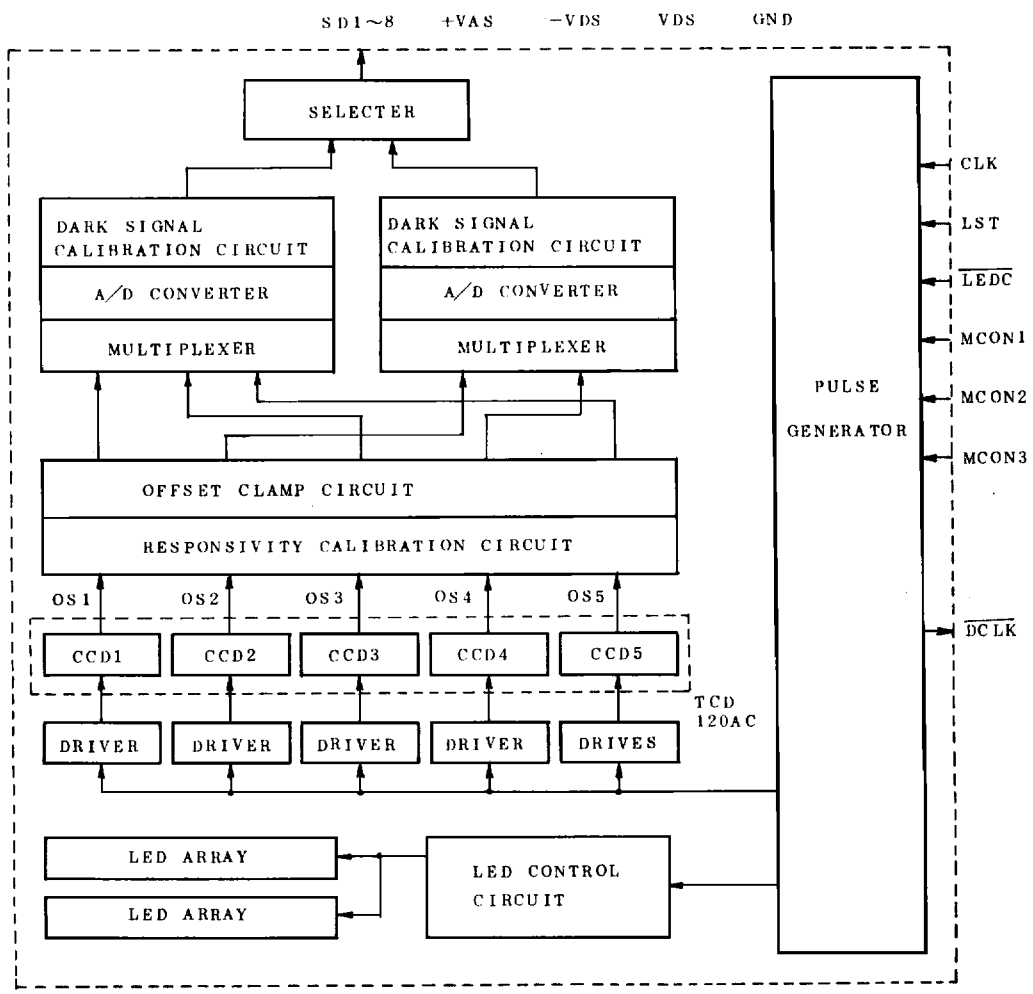
(Note 1): All voltage are respect to GND.

I/O DRAWING


CIPS
Operating pulses for CIPS
CLK
LST
SD1~8
Signal (Digital 8bit)
LED ON-OFF control
LEDC
Memory control mode
MCON1
MCON2
MCON3
DCLK
control pulse for signal processing circuit
Power suply
+VAS
GND
-VAS
VDS


Integration time (tINT)
Input
CLK
LST
Output
SD1~8
S1
S4678
DCLK

BLOCK DIAGRAM



CONNECTOR PIN ARAAY

NO.	SYMBOL	PIN NAME	I/O	REMARKS
1	$-V_{AS}$	Analog Power Supply	-	-12V
2	$-V_{AS}$	Analog Power Supply	-	-12V
3	$+V_{AS}$	Analog Power Supply	-	+12V
4	$+V_{AS}$	Analog Power Supply	-	+12V
5	GND	Ground	-	
6	GND	Ground	-	
7	V_{DS}	Digital Power Supply	-	+5V
8	GND	Ground	-	
9	V_{DS}	Digital Power Supply	-	+5V
10	CLK	Master Clock Pulse	I	8MHz
11	$\overline{LST}$	Line Start Pulse	I	
12	$\overline{LEDC}$	LED Control Pluse	I	
13	MCON3	Line Memory Control	I	
14	MCON2	Line Memory Control	I	
15	MCON1	Line Memory Control	I	
16	GND	Ground	-	
17	SD8	Signal Output	O	MSB
18	SD7	Signal Output	O	
19	SD6	Signal Output	O	
20	SD5	Signal Output	O	
21	SD4	Signal Output	O	
22	SD3	Signal Output	O	
23	SD2	Signal Output	O	
24	SD1	Signal Output	O	LSB
25	$\overline{DCLK}$	Data Clock Pulse	O	2MHz
26	NC	No Connect	-	

CONNECTOR : HIF3F-26PA-2.54DS
(BY HIROSE ELECTRIC CO., LTD.)

OPTICAL/ELECTRICAL CHARACTERISTICS

(Ta=25°C, +V_{AS}=12V, -V_{AS}=-12V, V_{DS}=5V, V_{CLK}=V_{LST}=5V (PULSE)
f_{DCLK}=2MHz, t_{INT} (INTEGRATION TIME)=2.64 msec)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
White Level Output	SD_W	(1), (2)	-	-	213	LSB
Black Level Output	SD_B	(2), (3)	0	-	-	LSB
Photo Response Non Uniformity	PRNU	(1), (5)	-	-	20	%
Moduilation Transfer Function	MTF	(4), (5)	40	60	-	%
Digital Output H-Level Voltage	V_{SDH}	I_{SDH}=-20μA	4.9	5	-	V
Digital Output L-Level Voltage	V_{SDL}	I_{SDL}=20μA	-	0	0.1	V
Analog Current Dissipation	$+I_{AS}$		-	250	300	mA
Analog Current Dissipation	$-I_{AS}$		-	600	720	mA
Digital current Dissipation	I_{DS}		-	200	240	mA

TEST CONDITION

(1) Mesured by white paper (OD=0.07).

(2) Defined as Valid data (S1~S4678)

(3) LED array is off and out light is shutout.

(4) Mesured by 200 cycles/inch pattern.

(5) PRNU and MTF is defined as follows, (S1~S4678)

$$PRNU=\frac{SDmax - SDmin}{SDmax + SDmin}\times 100\ (\%)$$

But SDmax and SDmin are shown in fig. 1.

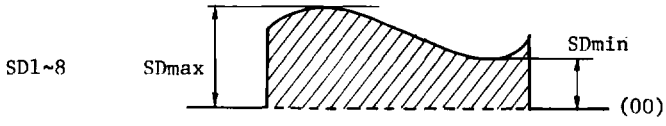


fig. 1 PRNU test condition

$$MTF = \frac{SD'max - SD'min}{SD'max + SD'min} \times 100\ (\%)$$

But, SD'max and SD'min are shown in fig. 2.

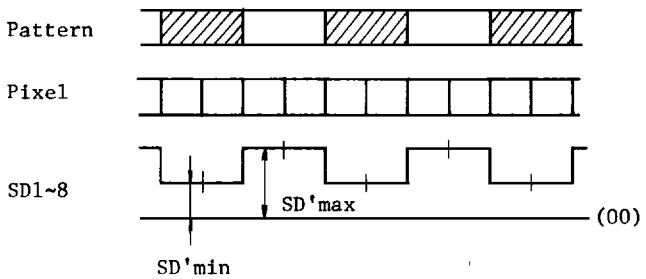


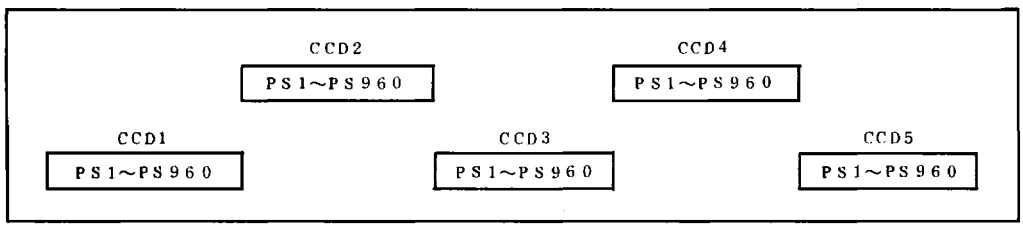
fig. 2 MTF test condition

OPERATING CONDITION (Ta=25°C)

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Master Clock Pulse Voltage	H-Level	V_{CLK}	V_{DS}-1	-	V_{DS}-1	V
	L-Level		0	0.2	0.5	
Line Start Pulse Voltage	H-Level	V_{LST}	V_{DS}-1		V_{DS}-1	V
	L-Level		0	0.2	0.5	
Line Memory Control Voltage	H-Level	V_{MCON}	VDS-1	-	VDS-1	V
	L-Level		0	0.2	0.5	
LED Coltrol Voltage (Note 2)	H-Level	V_{LEDC}	VDS-1	-	VDS-1	V
	L-Level		0	0.2	0.5	
Digital Supply Voltage		V_{DS}	4.5	5	5.5	V
Analog Supply Voltage		$+V_{AS}$	11.5	12	12.5	V
Analog Supply Voltage		$-V_{AS}$	-12.5	-12	-11.5	V
Master Clock Frequency		f_{CLK}	-	8	-	MHz

(Note 2): LED Control Voltage H-Level ... LED Arrays off
L-Level ... LED Arrays on

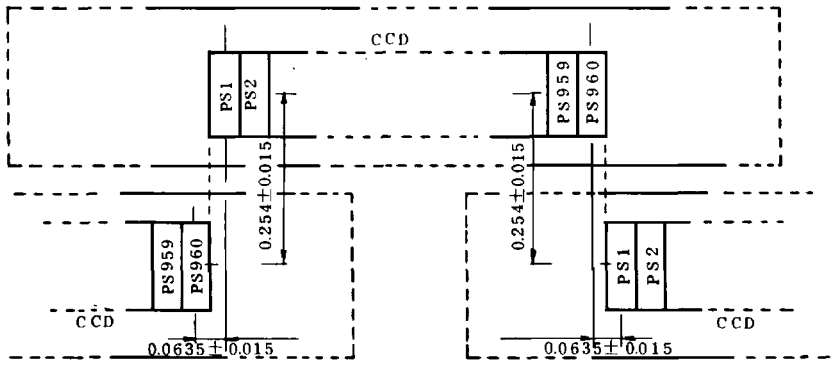
LOCATION OF CCD CHIPS



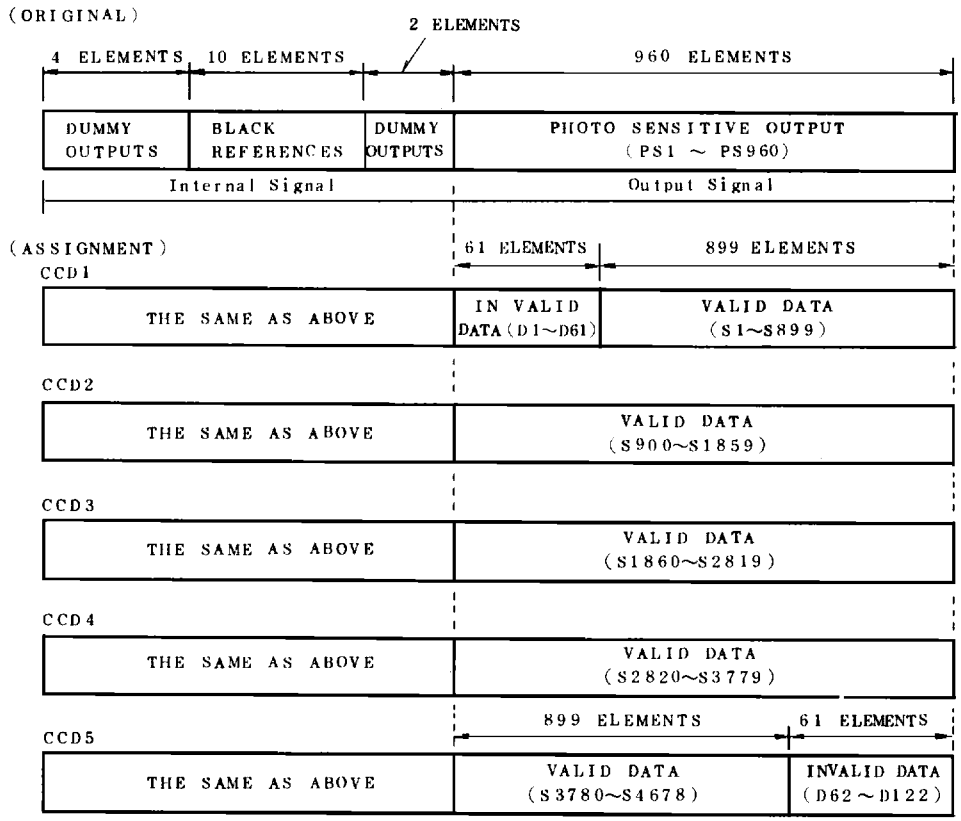
(Photo Sensitive Side)

ARRANGEMENT OF ELEMENTS BETWEEN CHIPS

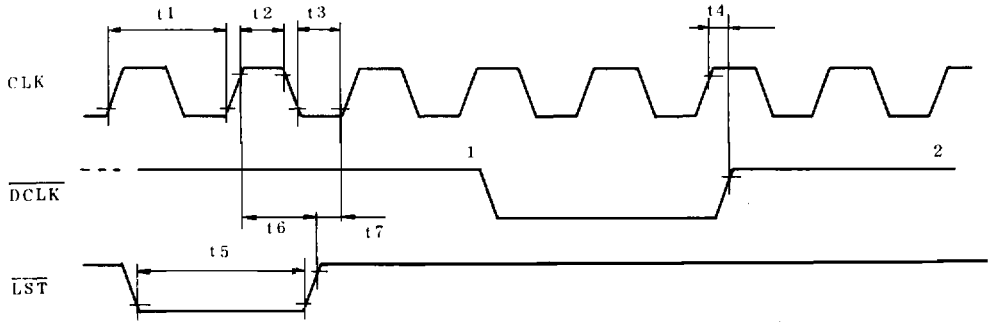
Unit: mm



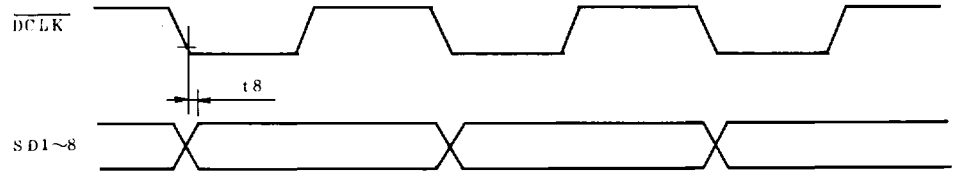
APPRANGEMENT OF ELEMENT ON ONE CHIP



TIMING REQUIREMENTS (1)

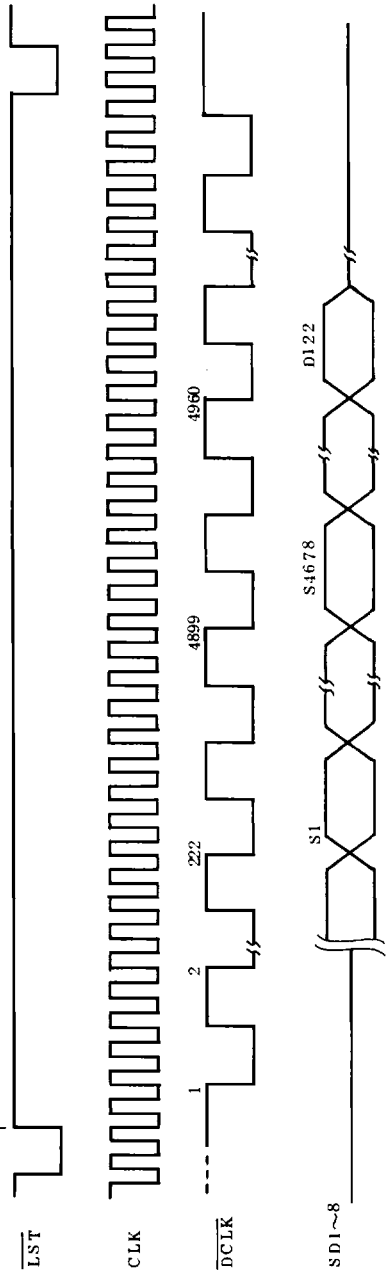


* When $\overline{LST}$ is L-level, $\overline{DCLK}$ is H-level.



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
CLK Period	t1	125	125	-	ns
CLK H-Level Period	t2	30	55	-	ns
CLK L-Level Period	t3	30	55	-	ns
CLK-$\overline{DCLK}$ Pulse Timing	t4	-	100	-	ns
$\overline{LST}$ Pulse Period	t5	50	240	-	ns
CLK-$\overline{LST}$ Pulse Timing	t6	10	-	-	ns
CLK-LST Pulse Timing	t7	10	-	-	ns
Digital Output Delay	t8	-	100	-	ns

TIMING REQUIREMENTS (2)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Integration Time	t9	-	2.64	-	ms

MEMORY CONTROL MODE SELECT OPTION

MODE	CONDITION			SCANNING SPEED (μm/SCAN)	REMARKS
	MCON3	MCON2	MCON1		
0	L	L	L	-	
1	L	L	H	254	(Note 3)
2	L	H	L	127	(Note 3)
3	L	H	H	84.7	(Note 3)
4	H	L	L	63.5	Normal Mode
5	H	L	H	50.8	(Note 4)
6	H	H	L	42.3	(Note 4)
-	H	H	H	-	Prohibition

(Note 3): This mode can be used reduced application.

(Note 4): This mode can be used magnifying application.

CAUTIONS

(1) Individual supply voltages must be sufficient to carry the load.

(2) Input/Output connector must not be connected in reverse.

(3) The rod lens array can be cleaned by gently rubbing the surface with cotton soaked in alcohol.

(4) The Contact Image Sensor should not be subject to mechanical shock. Shock or dropping could damage the optical system or the internal Image Sensor.

DIMENSIONAL OUTLINE

Unit: mm