NEC

MOS INTEGRATED CIRCUIT

# μPD4416016

## 16M-BIT CMOS FAST SRAM
## 1M-WORD BY 16-BIT

### Description

The μPD4416016 is a high speed, low power, 16,777,216 bits (1,048,576 words by 16 bits) CMOS static RAM.

Operating supply voltage is 3.3 V ± 0.3 V.

The μPD4416016 is packaged in a 54-pin plastic TSOP (II).

### Features

- 1,048,576 words by 16 bits organization
- Fast access time : 15 ns (MAX.)
- Byte data control : /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Output Enable input for easy application

<R> **Ordering Information**

| Part number | Package | Supply voltage V | Access time ns (MAX.) | Supply current mA (MAX.) | |
|---|---|---|---|---|---|
| | | | | At operating | At standby |
| μPD4416016G5-A15-9JF | 54-PIN PLASTIC TSOP (II) (10.16 mm (400)) | 3.3 ± 0.3 | 15 | 250 | 10 |
| μPD4416016G5-A15-9JF-A | | | | | |

**Remark** Products with -A at the end of the part number are lead-free products.



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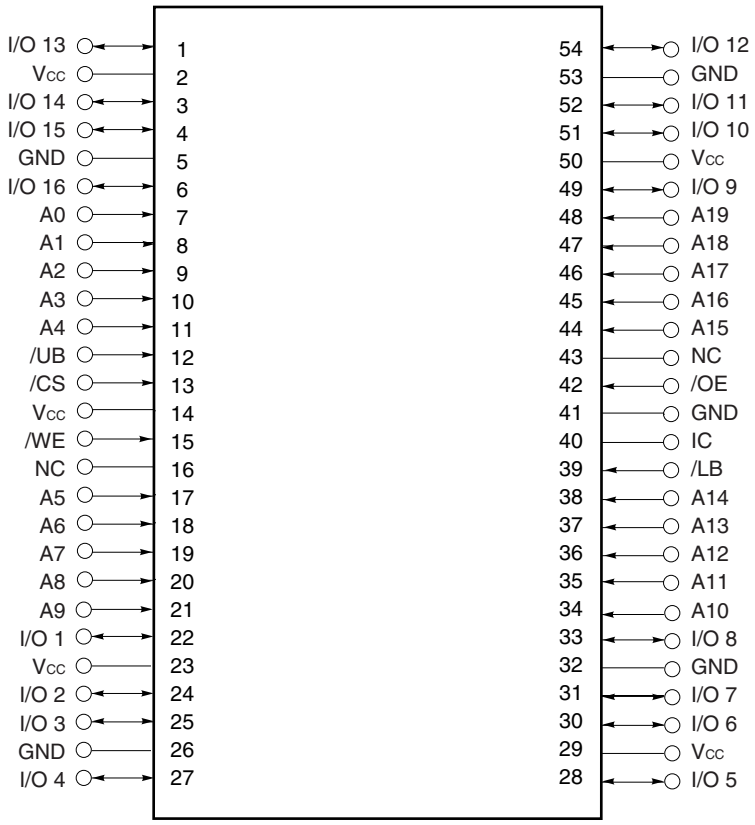
The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

### Pin Configuration (Marking Side)

/xxx indicates active low signal.

**54-PIN PLASTIC TSOP (II) (10.16 mm (400))**

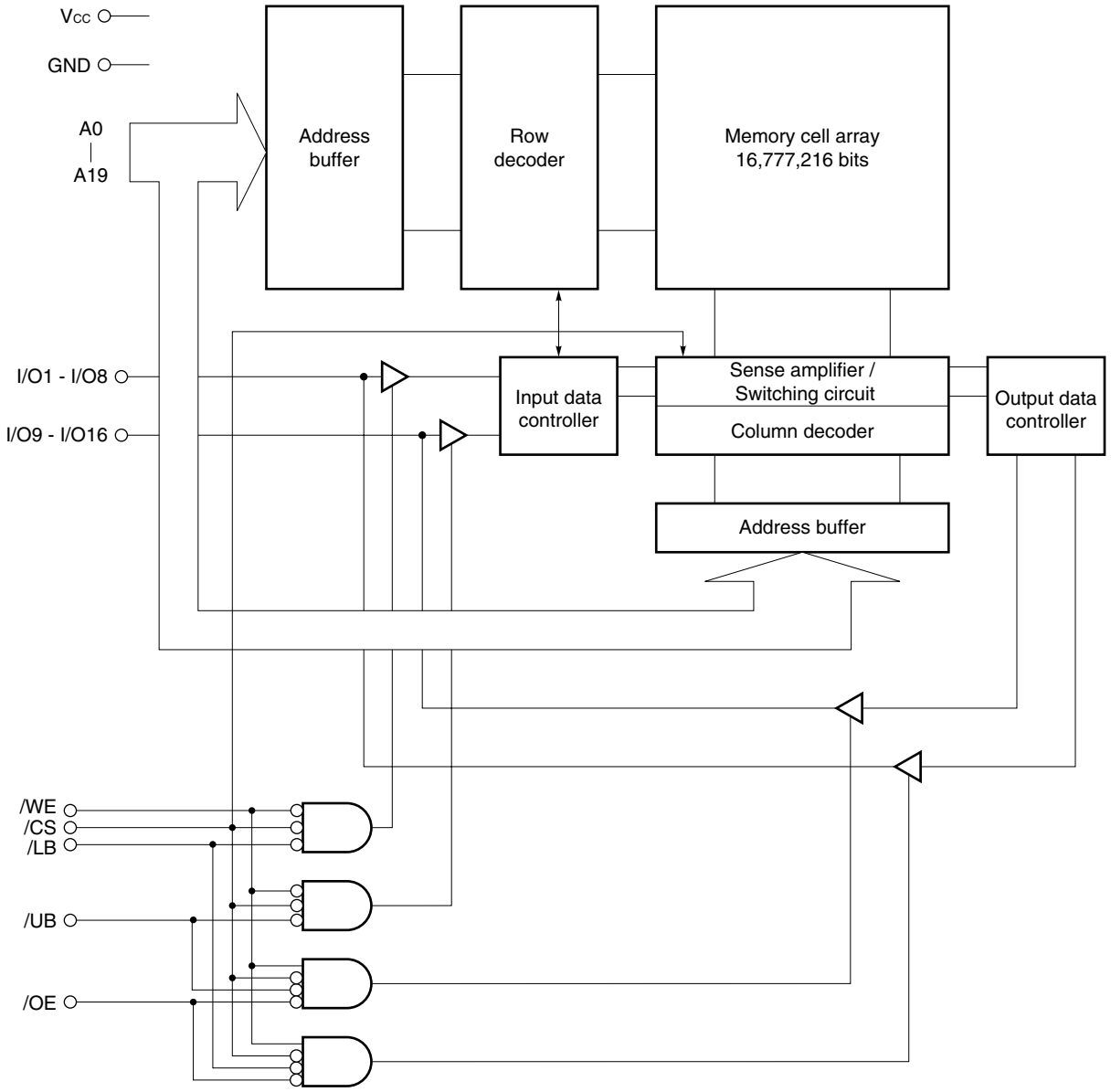



| | | |
|---|---|---|
| A0 - A19 | : | Address Inputs |
| I/O1 - I/O16 | : | Data Inputs / Outputs |
| /CS | : | Chip Select |
| /WE | : | Write Enable |
| /OE | : | Output Enable |
| /LB, /UB | : | Byte data select |
| VCC | : | Power supply |
| GND | : | Ground |
| NC | : | No connection |
| IC | : | Internal connection [Note] |

**Note** Leave this pin connect to GND.

**Remark** Refer to **Package Drawing** for 1-pin index mark.

## Block Diagram




## Truth Table

| /CS | /OE | /WE | /LB | /UB | Mode | I/O | | Supply current |
|---|---|---|---|---|---|---|---|---|
| | | | | | | I/O 1 - I/O 8 | I/O 9 - I/O16 | |
| H | × | × | × | × | Not selected | High impedance | High impedance | $I_{SB}$ |
| L | L | H | L | L | Read | $D_{OUT}$ | $D_{OUT}$ | $I_{CC}$ |
| | | | L | H | | $D_{OUT}$ | High impedance | |
| | | | H | L | | High impedance | $D_{OUT}$ | |
| L | × | L | L | L | Write | $D_{IN}$ | $D_{IN}$ | |
| | | | L | H | | $D_{IN}$ | High impedance | |
| | | | H | L | | High impedance | $D_{IN}$ | |
| L | H | H | × | × | Output disable | High impedance | High impedance | |
| L | × | × | H | H | | High impedance | High impedance | |

**Remark** × : Don't care

## Electrical Specifications

### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | –0.5 Note to +4.0 | V |
| Input / Output voltage | $V_T$ | | –0.5 Note to +4.0 | V |
| Operating ambient temperature | $T_A$ | | 0 to 70 | °C |
| Storage temperature | $T_{stg}$ | | –55 to +125 | °C |

**Note** –2.0 V (MIN.) (pulse width : 2 ns)

**Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Recommended Operating Conditions

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 3.0 | 3.3 | 3.6 | V |
| High level input voltage | $V_{IH}$ | | 2.0 | | $V_{CC}$ + 0.3 | V |
| Low level input voltage | $V_{IL}$ | | –0.3 Note | | +0.8 | V |
| Operating ambient temperature | $T_A$ | | 0 | | 70 | °C |

**Note** –2.0 V (MIN.) (pulse width : 2 ns)

### DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$ = 0 V to $V_{CC}$ | –2 | | +2 | μA |
| Output leakage current | $I_{LO}$ | $V_{I/O}$ = 0 V to $V_{CC}$, /CS = $V_{IH}$ or /OE = $V_{IH}$ or /WE = $V_{IL}$ or /LB = $V_{IH}$ or /UB = $V_{IH}$ | –2 | | +2 | μA |
| Operating supply current | $I_{CC}$ | /CS = $V_{IL}$, $I_{I/O}$ = 0 mA, Minimum cycle time | | | 250 | mA |
| Standby supply current | $I_{SB}$ | /CS = $V_{IH}$, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, Minimum cycle time | | | 80 | mA |
| | $I_{SB1}$ | /CS ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≤ 0.2 V or $V_{IN}$ ≥ $V_{CC}$ – 0.2 V | | | 10 | |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | 2.4 | | | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = +8.0 mA | | | 0.4 | V |

**Remark** $V_{IN}$ : Input voltage, $V_{I/O}$ : Input / Output voltage

### Capacitance ($T_A$ = 25 °C, f = 1 MHz)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | | | 6 | pF |
| Input / Output capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V | | | 8 | pF |

**Remarks 1.** $V_{IN}$ : Input voltage, $V_{I/O}$ : Input / Output voltage

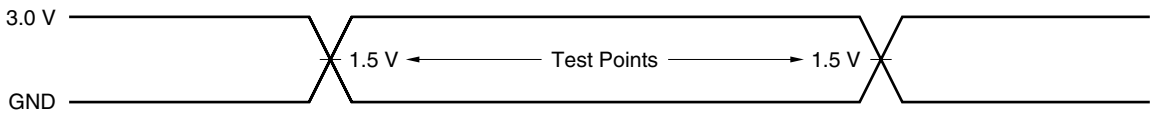
**2.** These parameters are periodically sampled and not 100% tested.

**AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

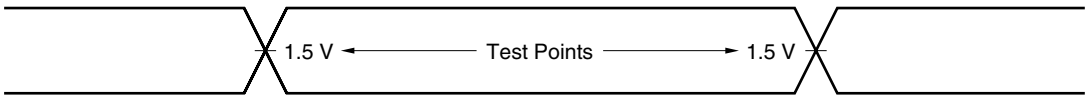
**AC Test Conditions**

**LVTTL Interface**

**Input Waveform (Rise and Fall Time ≤ 3 ns)**




**Output Waveform**




**Output Load**

AC characteristics directed with the note should be measured with the output load shown in Figure 1 or Figure 2.

**Figure 1**

(for $t_{AA}$, $t_{ACS}$, $t_{OE}$, $t_{ABD}$, $t_{OH}$)

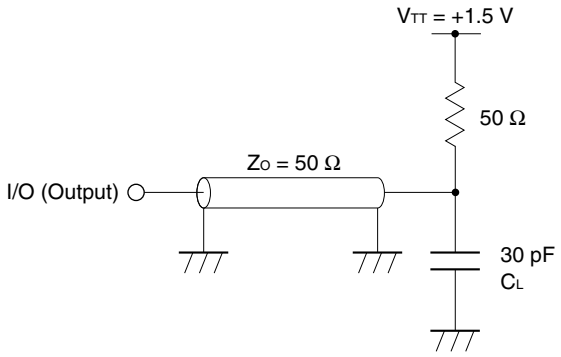
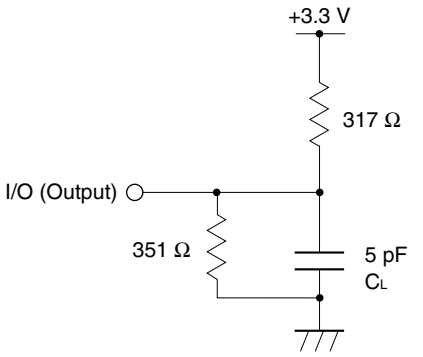



**Figure 2**

(for $t_{CLZ}$, $t_{OLZ}$, $t_{BLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{BHZ}$, $t_{WHZ}$, $t_{OW}$)




**Remark** $C_L$ includes capacitances of the probe and jig, and stray capacitances.

**Read Cycle**

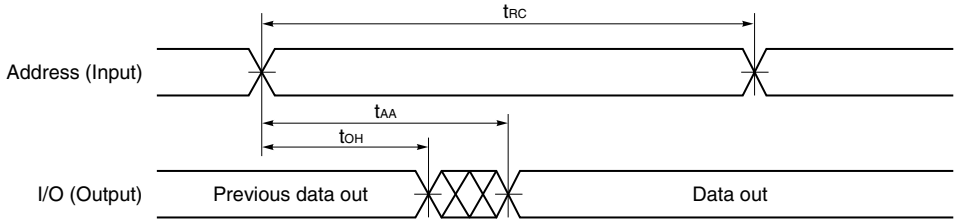
| Parameter | Symbol | MIN. | MAX. | Unit | Notes |
|---|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 15 | | ns | |
| Address access time | $t_{AA}$ | | 15 | ns | 1 |
| /CS access time | $t_{ACS}$ | | 15 | ns | |
| /OE access time | $t_{OE}$ | | 7 | ns | |
| /LB, /UB access time | $t_{ABD}$ | | 7 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | | ns | |
| /CS to output in low impedance | $t_{CLZ}$ | 3 | | ns | 2, 3 |
| /OE to output in low impedance | $t_{OLZ}$ | 0 | | ns | |
| /LB, /UB to output in low impedance | $t_{BLZ}$ | 0 | | ns | |
| /CS to output in high impedance | $t_{CHZ}$ | | 7 | ns | |
| /OE to output hold in high impedance | $t_{OHZ}$ | | 7 | ns | |
| /LB, /UB to output hold in high impedance | $t_{BHZ}$ | | 7 | ns | |

**Notes 1.** See the output load shown in **Figure 1**.

**2.** Transition is measured at ±200 mV from steady-state voltage with the output load shown in **Figure 2**.

**3.** These parameters are periodically sampled and not 100% tested.

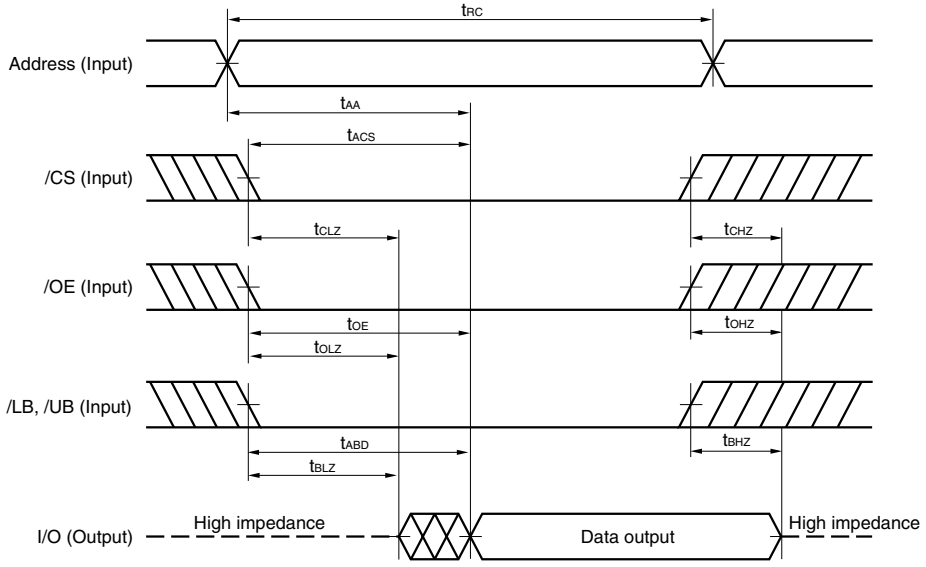
**Read Cycle Timing Chart 1 (Address Access)**




**Remarks 1.** In read cycle, /WE should be fixed to high level.

**2.** /CS = /OE= /LB (or /UB) = $V_{IL}$

**Read Cycle Timing Chart 2 (/CS Access)**




**Caution Address valid prior to or coincident with /CS low level input.**

**Remark** In read cycle, /WE should be fixed to high level.

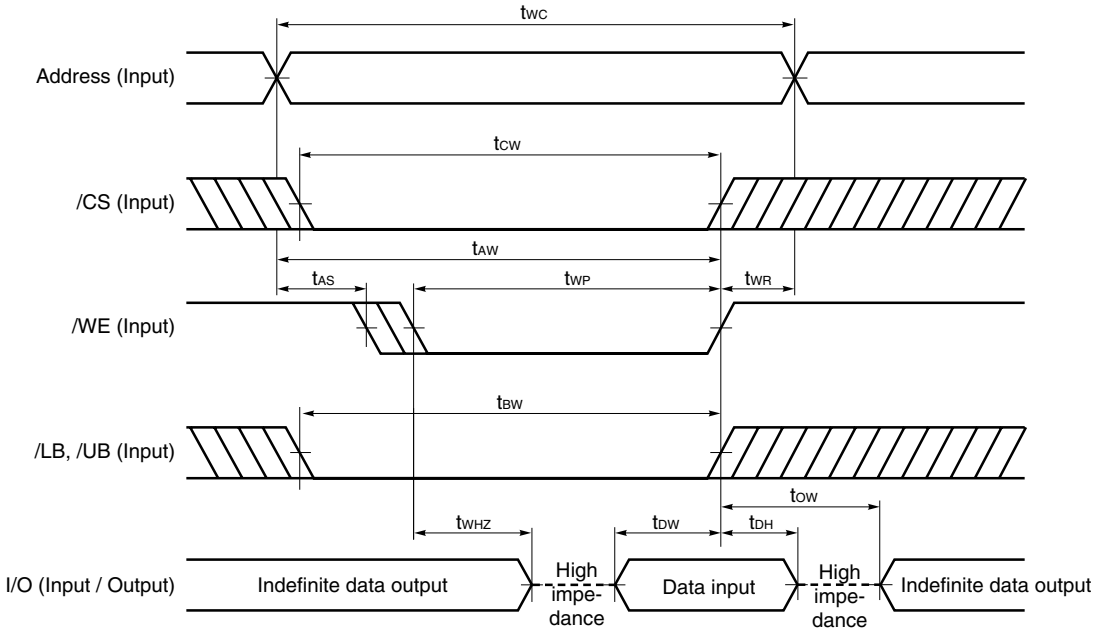
**Write Cycle**

| Parameter | Symbol | MIN. | MAX. | Unit | Notes |
|---|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 15 | | ns | |
| /CS to end of write | $t_{CW}$ | 10 | | ns | |
| Address valid to end of write | $t_{AW}$ | 10 | | ns | |
| Write pulse width | $t_{WP}$ | 10 | | ns | |
| /LB, /UB to end of write | $t_{BW}$ | 10 | | ns | |
| Data valid to end of write | $t_{DW}$ | 7 | | ns | |
| Data hold time | $t_{DH}$ | 0 | | ns | |
| Address setup time | $t_{AS}$ | 0 | | ns | |
| Write recovery time | $t_{WR}$ | 1 | | ns | |
| /WE to output in high impedance | $t_{WHZ}$ | | 7 | ns | 1, 2 |
| Output active from end of write | $t_{OW}$ | 3 | | ns | |

**Notes 1.** Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

**2.** These parameters are periodically sampled and not 100% tested.

**Write Cycle Timing Chart 1 (/WE Controlled)**




**Cautions 1. /CS or /WE should be fixed to high level during address transition.**

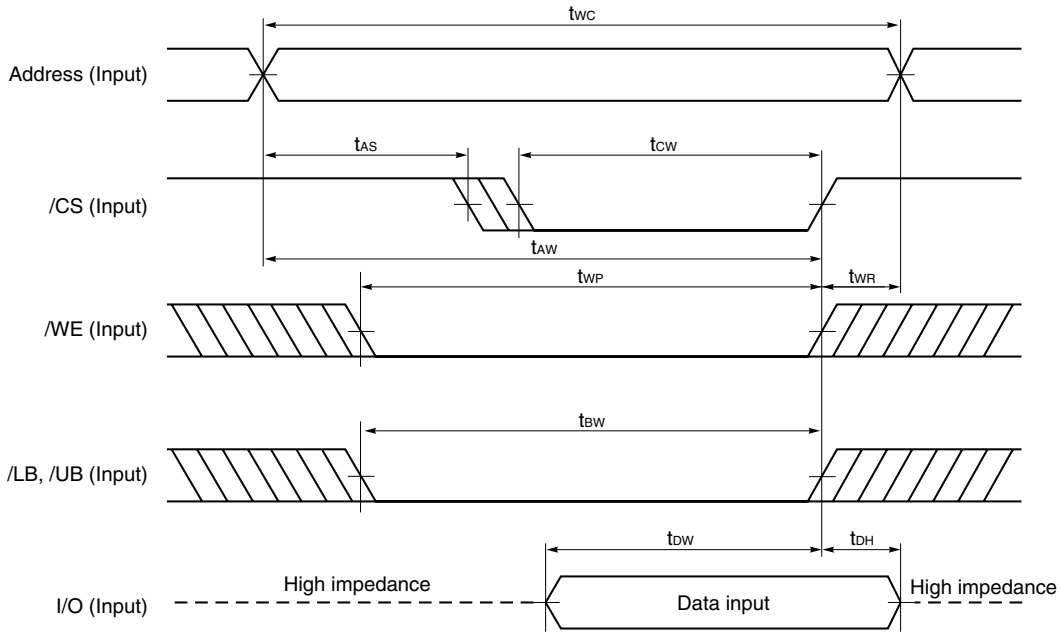
**2. Do not input data to the I/O pins while they are in the output state.**

**Remarks 1.** Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

**2.** During $t_{WHZ}$, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

**3.** When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

**Write Cycle Timing Chart 2 (/CS Controlled)**

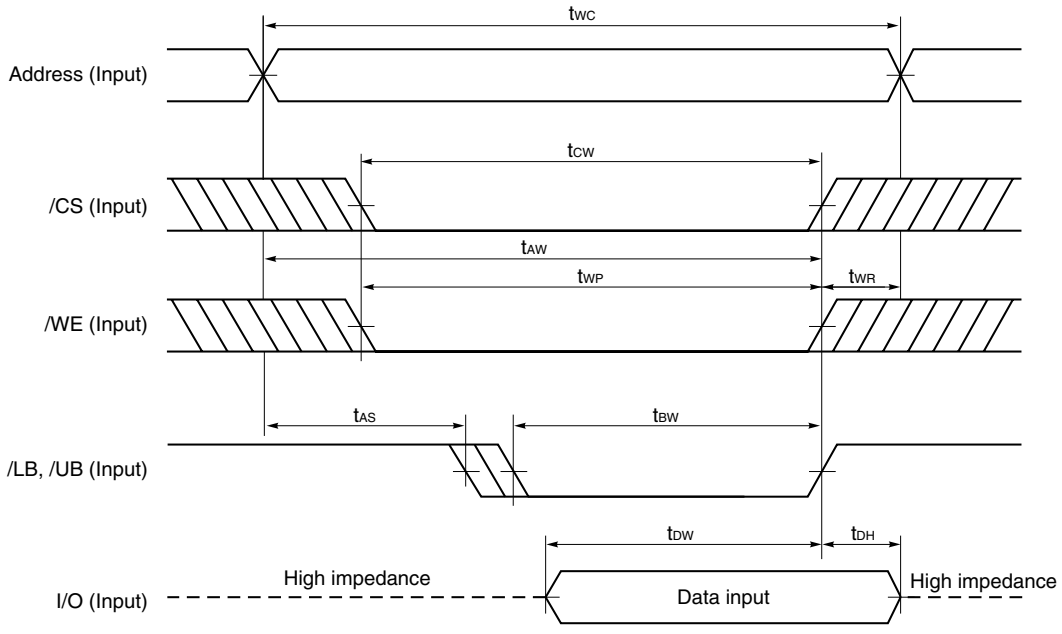



**Cautions 1. /CS or /WE should be fixed to high level during address transition.**

**2. Do not input data to the I/O pins while they are in the output state.**

**Remark** Write operation is done during the overlap time of a low level /CS and a low level /WE and a low level /LB (or low level /UB).

**Write Cycle Timing Chart 3 (/LB, /UB Controlled)**



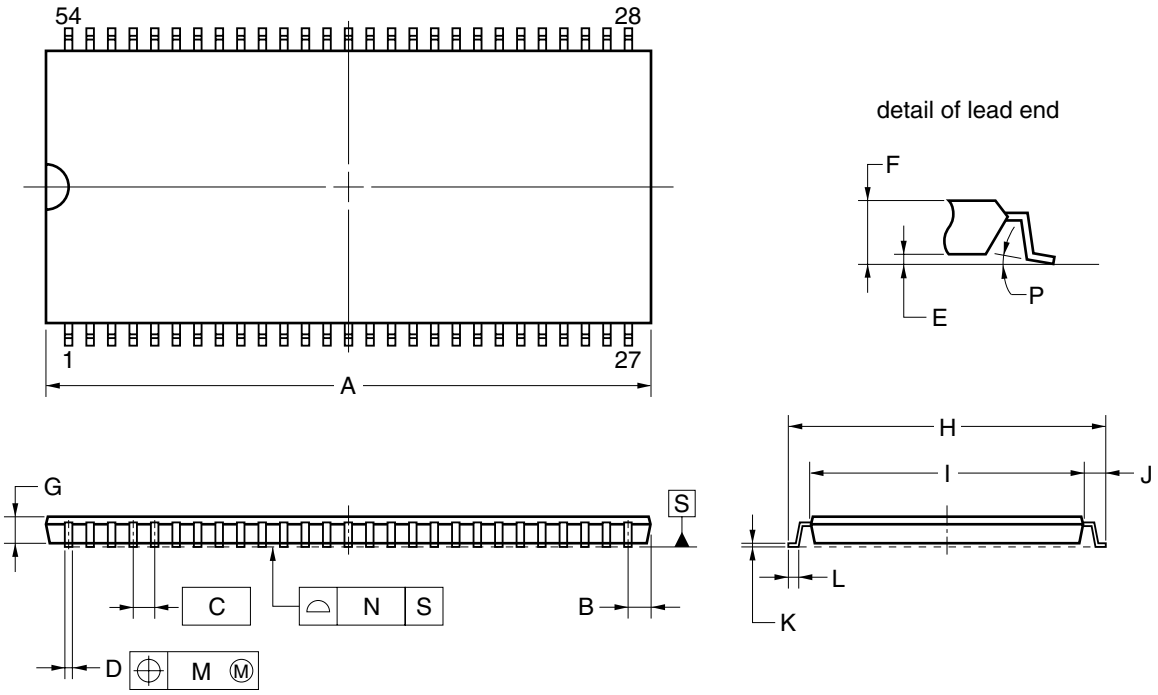

**Cautions 1. /CS or /WE should be fixed to high level during address transition.**

**2. Do not input data to the I/O pins while they are in the output state.**

**Remark** Write operation is done during the overlap time of a low level /CS and a low level /WE and a low level /LB (or low level /UB).

**Package Drawing**

## 54-PIN PLASTIC TSOP (II) (10.16 mm (400))




**NOTES**

1. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

2. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

| ITEM | MILLIMETERS |
|---|---|
| A | 22.22±0.05 |
| B | 0.91 MAX. |
| C | 0.80 (T.P.) |
| D | $0.32^{+0.08}_{-0.07}$ |
| E | 0.10±0.05 |
| F | 1.1±0.1 |
| G | 1.00 |
| H | 11.76±0.20 |
| I | 10.16±0.10 |
| J | 0.80±0.20 |
| K | $0.145^{+0.025}_{-0.015}$ |
| L | 0.50±0.10 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |

**S54G5-80-9JF-3**

### Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD4416016.

**Type of Surface Mount Device**

μPD4416016G5-9JF : 54-PIN PLASTIC TSOP (II) (10.16 mm (400))

μPD4416016G5-9JF-A : 54-PIN PLASTIC TSOP (II) (10.16 mm (400))

<R> ### Quality Grade

- A quality grade of the products is “Standard”.
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

**Revision History**

| Edition/ Date | Page | | Type of revision | Location | Description (Previous edition → This edition) |
|---|---|---|---|---|---|
| | This edition | Previous edition | | | |
| 7th edition/ Sep. 2006 | p.1 | p.1 | Deletion | Ordering Information | μPD4416016G5-A17-9JF<br>μPD4416016G5-A17-9JF-A |
| | p.10 | p.10 | Addition | Quality Grade | Section of Quality Grade has been added. |

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## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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