240pin Unbuffered DDR2 SDRAM MODULE

Based on 32Mx16 DDR2 SDRAM

Features

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 32Mx64 DDR2 Unbuffered DIMM based on 32Mx16 DDR2 SDRAM
- Performance:

		PC2-3200	PC2-4200	PC2-5300	Unit
Speed Sort		5A	37B	3C	
DIMM $\overline{CAS}$ Latency*		3	4	5	
f_{CK}	Clock Frequency	200	266	333	MHz
t_{CK}	Clock Cycle	5	3.7	3	ns
f_{DQ}	DQ Burst Frequency	400	533	667	MHz

- Intended for 200 MHz, 266MHz, and 333MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ}$ = 1.8Volt ± 0.1
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 3, 4, 5
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 13/10/1 Addressing (row/column/bank)
- 7.8µs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 84-ball FBGA Package

Description

M1U25664TUH4A0F & M1Y25664TUH4A0F are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a one-rank 64Mx64 high-speed memory array. Modules use four 32Mx16 DDR2 SDRAMs in FBGA packages. These DIMMs manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 200 MHz (266MHz and 333MHz) clock speeds and achieves high-speed data transfer rates of up to 400 MHz (533MHz and 667MHz). Prior to any access operation, the device $\overline{CAS}$ latency and burst type/ length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M1U25664TUH4A0F-5A	200MHz (5ns @ CL = 3)	DDR2-400	PC2-3200	32Mx64	Gold	1.8V	
M1Y25664TUH4A0F-5A							Green
M1U25664TUH4A0F-37B	266MHz (3.7ns @ CL = 4)	DDR2-533	PC2-4200				
M1Y25664TUH4A0F-37B							Green
M1U25664TUH4A0F-3C	333MHz (3ns @ CL = 5)	DDR2-667	PC2-5300				
M1Y25664TUH4A0F-3C							Green

Pin Description

CK0, $\overline{CK0}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	CB0-CB7	ECC Check Bit Data Input/Output
$\overline{RAS}$	Row Address Strobe	DQS0-DQS8	Bidirectional data strobes
$\overline{CAS}$	Column Address Strobe	DM0-DM8/DQS9-17	Input Data Mask/High Data Strobes
$\overline{WE}$	Write Enable	$\overline{DQS0}$-$\overline{DQS17}$	Differential data strobes
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	V_{DD}	Power (1.8V)
A0-A9, A11-A13	Address Inputs	V_{REF}	Ref. Voltage for SSTL_18 inputs
A10/AP	Column Address Input/Auto-precharge	V_{DDSPD}	Serial EEPROM positive power supply
BA0, BA1	SDRAM Bank Address Inputs	V_{SS}	Ground
$\overline{RESET}$	Reset pin	SCL	Serial Presence Detect Clock Input
ODT0, ODT1	Active termination control lines	SDA	Serial Presence Detect Data input/output
NC	No Connect	SA0-2	Serial Presence Detect Address Inputs

Pinout

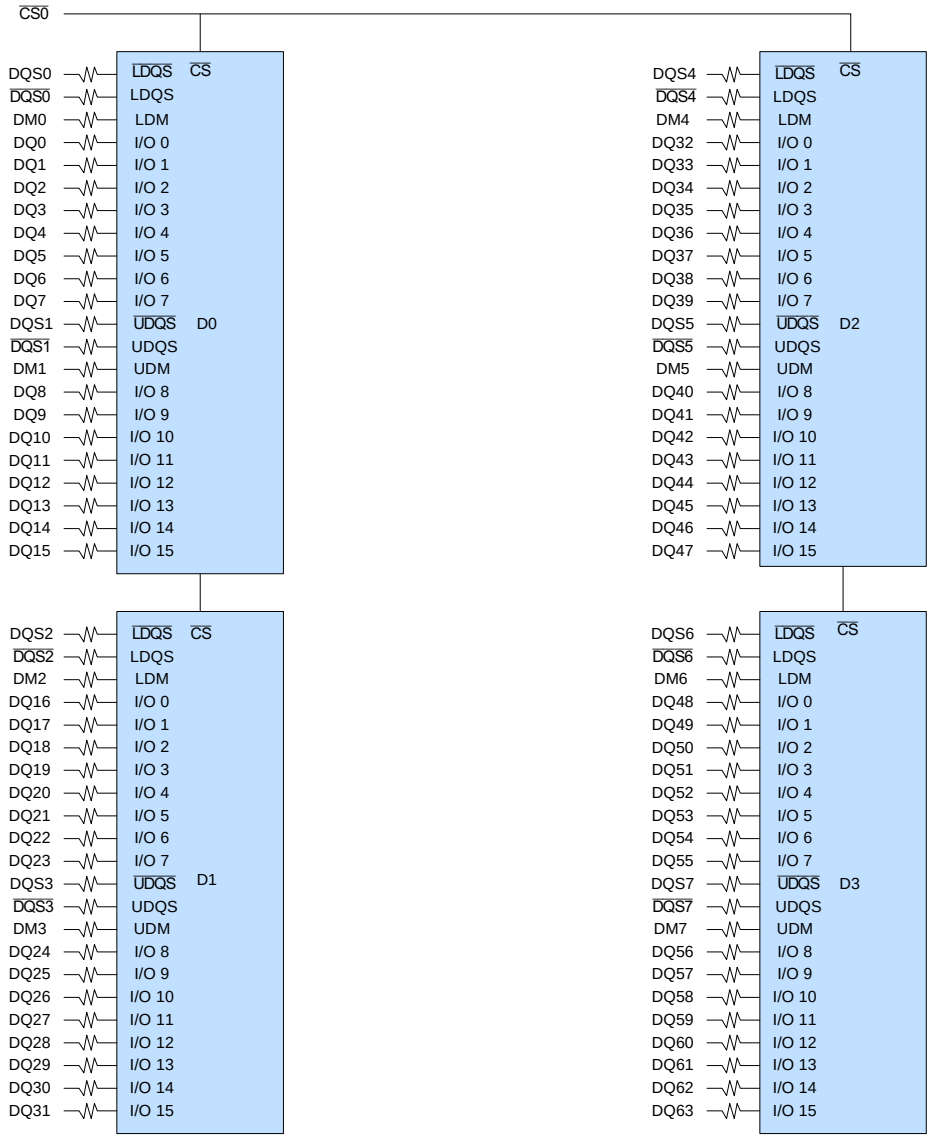
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{REF}	42	NC	82	V_{SS}	123	DQ5	164	NC	204	V_{SS}
2	V_{SS}	43	NC	83	$\overline{DQS4}$	124	V_{SS}	165	NC	205	DQ38
3	DQ0	44	V_{SS}	84	DQS4	125	DM0, DQS9	166	V_{SS}	206	DQ39
4	DQ1	45	NC	85	V_{SS}	126	$\overline{DQS9}$	167	NC	207	V_{SS}
5	V_{SS}	46	NC	86	DQ34	127	V_{SS}	168	NC	208	DQ44
6	$\overline{DQS0}$	47	V_{SS}	87	DQ35	128	DQ6	169	V_{SS}	209	DQ45
7	DQS0	48	NC	88	V_{SS}	129	DQ7	170	V_{DDQ}	210	V_{SS}
8	V_{SS}	49	NC	89	DQ40	130	V_{SS}	171	CKE1	211	DM5
9	DQ2	50	V_{SS}	90	DQ41	131	DQ12	172	V_{DD}	212	NC
10	DQ3	51	V_{DDQ}	91	V_{SS}	132	DQ13	173	NC	213	V_{SS}
11	V_{SS}	52	CKE0	92	$\overline{DQS5}$	133	V_{SS}	174	NC	214	DQ46
12	DQ8	53	V_{DD}	93	DQS5	134	DM1, DQS10	175	V_{DDQ}	215	DQ47
13	DQ9	54	NC	94	V_{SS}	135	$\overline{DQS10}$	176	A12	216	V_{SS}
14	V_{SS}	55	NC	95	DQ42	136	V_{SS}	177	A9	217	DQ52
15	$\overline{DQS1}$	56	V_{DDQ}	96	DQ43	137	CK1	178	V_{DD}	218	DQ53
16	DQS1	57	A11	97	V_{SS}	138	$\overline{CK1}$	179	A8	219	V_{SS}
17	V_{SS}	58	A7	98	DQ48	139	V_{SS}	180	A6	220	CK2
18	NC	59	V_{DD}	99	DQ49	140	DQ14	181	V_{DDQ}	221	$\overline{CK2}$
19	NC	60	A5	100	V_{SS}	141	DQ15	182	A3	222	V_{SS}
20	V_{SS}	61	A4	101	SA2	142	V_{SS}	183	A1	223	DM6
21	DQ10	62	V_{DDQ}	102	NC	143	DQ20	184	V_{DD}	224	NC
22	DQ11	63	A2	103	V_{SS}	144	DQ21	KEY		225	V_{SS}
23	V_{SS}	64	V_{DD}	104	$\overline{DQS6}$	145	V_{SS}	185	$\overline{CK0}$	226	DQ54
24	DQ16	KEY		105	DQS6	146	DM2	186	$\overline{CK0}$	227	DQ55
25	DQ17	65	V_{SS}	106	V_{SS}	147	NC	187	V_{DD}	228	V_{SS}
26	V_{SS}	66	V_{SS}	107	DQ50	148	V_{SS}	188	A0	229	DQ60
27	$\overline{DQS2}$	67	V_{DD}	108	DQ51	149	DQ22	189	V_{DD}	230	DQ61
28	DQS2	68	NC	109	V_{SS}	150	DQ23	190	BA1	231	V_{SS}
29	V_{SS}	69	V_{DD}	110	DQ56	151	V_{SS}	191	V_{DDQ}	232	DM7
30	DQ18	70	A10/AP	111	DQ57	152	DQ28	192	$\overline{RAS}$	233	NC
31	DQ19	71	BA0	112	V_{SS}	153	DQ29	193	$\overline{CS0}$	234	V_{SS}
32	V_{SS}	72	V_{DDQ}	113	$\overline{DQS7}$	154	V_{SS}	194	V_{DDQ}	235	DQ62
33	DQ24	73	$\overline{WE}$	114	DQS7	155	DM3	195	ODT0	236	DQ63
34	DQ25	74	$\overline{CAS}$	115	V_{SS}	156	NC	196	A13	237	V_{SS}
35	V_{SS}	75	V_{DDQ}	116	DQ58	157	V_{SS}	197	V_{DD}	238	V_{DDSPD}
36	$\overline{DQS3}$	76	$\overline{CS1}$	117	DQ59	158	DQ30	198	V_{SS}	239	SA0
37	DQS3	77	ODT1	118	V_{SS}	159	DQ31	199	DQ36	240	SA1
38	V_{SS}	78	V_{DDQ}	119	SDA	160	V_{SS}	200	DQ37		
39	DQ26	79	V_{SS}	120	SCL	161	NC	201	V_{SS}		
40	DQ27	80	DQ32	121	V_{SS}	162	NC	202	DM4		
41	V_{SS}	81	DQ33	122	DQ4	163	V_{SS}	203	NC		

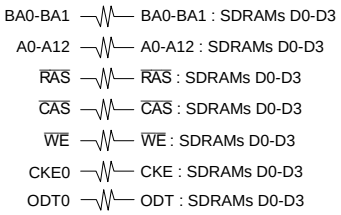
Input/Output Functional Description

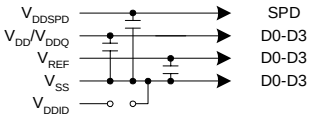
Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63 CB0 – CB7	(SSTL)	Active High	Data and Check Bit Input/Output pins. Check bits are only applicable on the x72 DIMM configurations.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0 – DQS8 $\overline{DQS0}$ – $\overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V DD to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

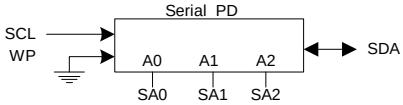
(256MB, 1 Rank, 32Mx16 DDR2 SDRAMs)







Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
4. BAx, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
5. Address and control resistors are 22 Ohms +/- 5%



Serial Presence Detect -- Part 1 of 2

32Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 32Mx16, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	13			0D			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Bank, Package, and Height	1 rank, Height=30mm			60			
6	Data Width of this Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at CL=5	5ns	3.75ns	3ns	50	3D	30	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	0.6ns	0.5ns	0.45ns	60	50	45	
11	DIMM Configuration Type	Non - ECC			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDR2 SDRAM Width	X16			10			
14	Error Checking DDR2 SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	3/4/5			38			
19	Reserved	Undefined			00			
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133/35mm)			02			
21	DDR2 SDRAM Module Attributes:	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver			01	01	13	
23	Minimum Clock Cycle at CL=4	5ns	3.75ns	3.75ns	50	3D	3D	
24	Maximum Data Access Time (t_{ac}) from Clock at CL=4	0.6ns	0.5ns	0.5ns	60	50	50	
25	Minimum Clock Cycle Time at CL=3	5ns			50			
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3	0.6ns			60			
27	Minimum Row Precharge Time (t_{RP})	15ns			3C			
28	Minimum Row Active to Row Active delay (t_{RRD})	10ns			28			
29	Minimum RAS to CAS delay (t_{RCD})	15ns			3C			
30	Minimum RAS Pulse Width (t_{RAS})	45ns			2D			
31	Module Bank Density	256MB			40			
32	Address and Command Setup Time Before Clock (t_{IS})	0.35ns	0.25ns	0.2ns	35	25	20	
33	Address and Command Hold Time After Clock (t_{IH})	0.475ns	0.375ns	0.325ns	47	37	32	
34	Data Input Setup Time Before Clock (t_{DS})	0.15ns	0.1ns	0.05ns	15	10	05	
35	Data Input Hold Time After Clock (t_{DH})	0.275ns	0.225ns	0.175ns	27	22	17	
36	Write Recovery Time (t_{WR})	15ns			3C			
37	Internal Write to Read Command delay (t_{WTR})	10ns	7.5ns	7.5ns	28	1E	1E	
38	Internal Read to Precharge delay (t_{RTP})	7.5ns			1E			
39	Memory Analysis Probe Characteristics	Undefined			00			
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns			00			
41	Minimum Core Cycle Time (t_{RC})	60ns			3C			

Serial Presence Detect -- Part 2 of 2

32Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 32Mx16, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	105ns			69			
43	Maximum Clock Cycle Time (t_{CK})	8ns			80			
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.35ns	0.3ns	0.25ns	23	1E	19	
45	Read Data Hold Skew Factor (t_{QHS})	0.45ns	0.4ns	0.35ns	2D	28	23	
46	PLL Relock Time	N/A			00			
47-xx	IDD in SPD	Undefined			00			
xx-61	Reserved	Undefined			00			
62	SPD Reversion	1.0			10			
63	Checksum for byte 0-62	Checksum data			05	81	51	
64-71	Manufacture's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	N/A			00			
73-255	Reserved	Undefined			00			

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.5 to V_{DDQ}+0.5	V
V_{IN}	Voltage on Input relative to V_{SS}	-0.5 to +2.3	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	-0.5 to +2.3	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	-0.5 to +2.3	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	-55 to +100	°C

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics and Operating Conditions

(TA = 0 °C ~ 70 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDQ}	I/O Supply Voltage	1.7	1.9	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{IH} (DC)	Input High (Logic1) Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V	1
V_{IL} (DC)	Input Low (Logic0) Voltage	-0.3	V_{REF} - 0.125	V	1

Note:
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value

Operating, Standby, and Refresh Currents

T_A = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (256MB, 1 Rank, 32Mx16 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-3200 (-5A)	PC2-4200 (-37B)	PC2-5300 (-3C)	Unit	Notes
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	290	330	TBD	mA	1, 2
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	310	360	TBD	mA	1, 2
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	20	20	TBD	mA	1, 2
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	140	170	TBD	mA	1, 2
I_{DD3P}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	55	70	TBD	mA	1, 2
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	145	170	TBD	mA	1, 2
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	350	400	TBD	mA	1, 2
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = t_{CK} (MIN)	370	450	TBD	mA	1, 2
I_{DD5}	Auto-Refresh Current: t_{RC} = t_{RFC} (MIN)	490	520	TBD	mA	1, 2, 4
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	18	18	TBD	mA	1, 2
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	850	900	TBD	mA	1, 2

Note:
1. I_{DD} specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ns.
3. Enables on-chip refresh and address counters.
4. Current at 7.8µs is time-averaged value of I_{DD5} at t_{RFC} (MIN) and I_{DD2P} over 7.8µs.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter		-5A		-37B		-3C		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	DQ output access time from CK/$\overline{CK}$		-0.6	+0.6	-0.5	+0.5	-0.45	+0.45	ns
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		-0.5	+0.5	-0.45	+0.45	-0.4	+0.4	ns
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time		t_{CH} or t_{CL}		t_{CH} or t_{CL}		t_{CH} or t_{CL}		t_{CK}
t_{CK}	Clock cycle time	CL=3	5	8	3.75	8	3	8	ns
t_{CK}		CL=4, 5	5	8	3.75	8	3	8	ns
t_{DH}	DQ and DM input hold time		0.275		0.225		0.175		ns
t_{DS}	DQ and DM input setup time		0.15		0.1		0.1		ns
t_{IPW}	Input pulse width		0.6		0.6		0.6		ns
t_{DIPW}	DQ and DM input pulse width (each input)		0.35		0.35		0.35		ns
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$			t_{AC} (max)		t_{AC} (max)	t_{AC}		ns
t_{LZ}	Data-out low-impedance time from CK/$\overline{CK}$		2tAC (min)	t_{AC} (max)	2 t_{AC} (min)	t_{AC} (max)	t_{AC}		ns
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)			0.35		0.3		0.24	ns
t_{QHS}	Data hold Skew Factor			0.45		0.4		0.34	ns
t_{QH}	Data output hold time from DQS		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{CK}
t_{DQSS}	Write command to 1st DQS latching transition		-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	t_{CK}
$t_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)		0.35		0.35		0.35		t_{CK}
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		0.2		t_{CK}
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		0.2		t_{CK}
t_{MRD}	Mode register set command cycle time		2		2		2		t_{CK}
t_{WPST}	Write postamble		0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{WPRE}	Write preamble		0.35		0.35		0.35		t_{CK}
t_{IH}	Address and control input hold time		0.475		0.375		0.275		ns
t_{IS}	Address and control input setup time		0.35		0.25		0.2		ns
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
t_{RPST}	Read postamble		0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{RAS}	Active to Precharge command		45	120,000	40	120,000	45	120,000	ns
t_{RRD}	Active bank A to Active bank B command		7.5		7.5		7.5		ns
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$		2		2		2		t_{CK}

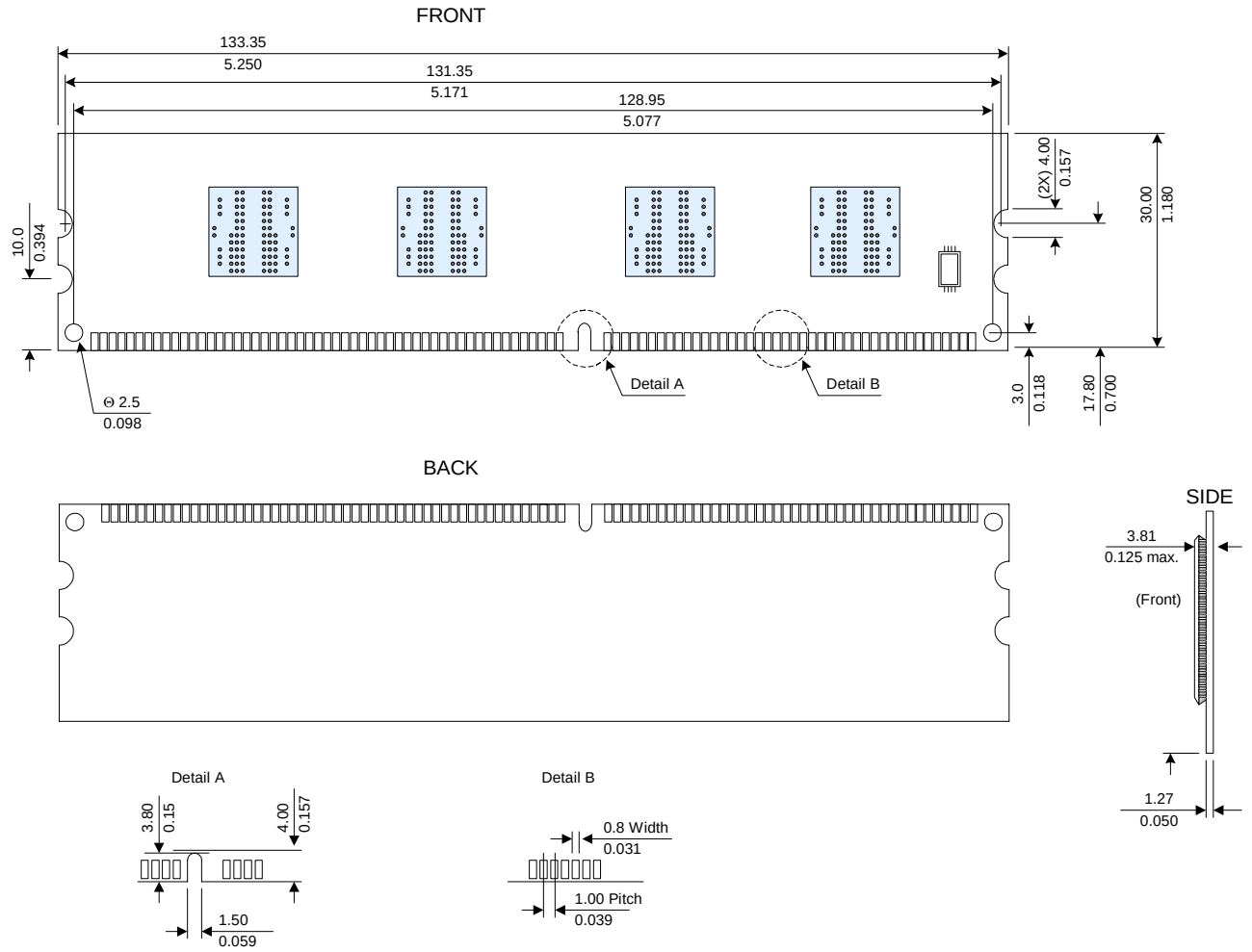
AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_A = 0 °C ~ 70 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-5A		-37B		-3C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WR}	Write recovery time	15		15		15		ns
t_{DAL}	Auto precharge write recovery + precharge time	$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		t_{CK}
t_{WTR}	Internal write to read command delay	10		7.5		7.5		t_{CK}
t_{RTP}	Internal read to precharge command delay	7.5		7.5		7.5		ns
t_{XSNR}	Exit self refresh to a Non-read command	t_{RFC}+10		t_{RFC} +10		t_{RFC} +10		ns
t_{XSRD}	Exit self refresh to a Read command	200		200		200		t_{CK}
t_{XP}	Exit precharge power down to any Non- read command	2		2		2		t_{CK}
t_{XARD}	Exit active power down to read command	2		2		2		t_{CK}
t_{XARDS}	Exit active power down to read command	6-AL		6-AL		7-AL		t_{CK}
t_{CKE}	CKE minimum pulse width	3		3		3		t_{CK}
t_{AOND}	ODT turn-on delay	2		2		2		t_{CK}
t_{AON}	ODT turn-on	t_{AC} (min)	t_{AC} (max) +1	t_{AC} (min)	t_{AC} (max) +1	t_{AC} (min)	t_{AC} (max) +0.7	t_{CK}
t_{AONPD}	ODT turn-on (Power down mode)	t_{AC} (min) +2	$2t_{CK}$ + t_{AC} (max) +1	t_{AC} (min) +2	$2t_{CK}$ + t_{AC} (max) +1	t_{AC} (min) +2	$2t_{CK}$ + t_{AC} (max) +1	t_{CK}
t_{AOFD}	ODT turn-off delay	2.5		2.5		2.5		t_{CK}
t_{AOF}	ODT turn-off	t_{AC} (min)	t_{AC} (max) +0.6	t_{AC} (min)	t_{AC} (max) +0.6	t_{AC} (min)	t_{AC} (max) +0.6	ns
t_{AOFPD}	ODT turn-off (Power down mode)	t_{AC} (min)+2	$2.5t_{CK}$ + t_{AC} (max) +1	t_{AC} (min)+2	$2.5t_{CK}$ + t_{AC} (max) +1	t_{AC} (min)+2	$2.5t_{CK}$ + t_{AC} (max) +1	ns
t_{ANPD}	ODT to power down entry latency	3		3		3		t_{CK}
t_{AXPD}	ODT power down exit latency	8		8		8		t_{CK}
t_{OIT}	OCD drive mode output delay	0	12	0	12	0	12	ns
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	t_{IS} + t_{CK} + t_{IH}		t_{IS} + t_{CK} + t_{IH}		t_{IS} + t_{CK} + t_{IH}		ns
t_{RCD}	Active to Read or Write delay	15		15		12		ns
t_{RP}	Precharge command period	15		15		12		ns
t_{REFI}	Average Periodic Refresh Interval		7.8		7.8		7.8	µs

Package Dimensions

(256MB, 1 Rank, 32Mx16 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Revision Log

Rev	Date	Modification
0.1	08/2004	Preliminary Release
1.0	01/2005	Added I_{dd} values
1.1	03/2005	Added DDR2-667 spec.