ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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EVALUATION KIT AVAILABLE

MAXIM

500ksps, 12-Bit Sampling ADCs with Track/Hold and Reference

General Description

The MAX120 and MAX122, BiCMOS, sampling 12-bit analog-to-digital converters (ADCs) combine an on-chip track/hold (T/H) and a low-drift voltage reference with fast conversion speeds and low power consumption. The T/H's 350ns acquisition time combined with the MAX120's 1.6µs conversion time results in throughputs as high as 500k samples per second (ksps). Throughput rates of 333ksps are possible with the 2.6µs conversion time of the MAX122.

The MAX120/MAX122 accept analog input voltages from -5V to +5V. The only external components needed are decoupling capacitors for the power-supply and reference voltages. The MAX120 operates with TTL-compatible clocks in the 0.1MHz to 8MHz frequency range. The MAX122 accepts 0.1MHz to 5MHz clock frequencies.

The MAX120/MAX122 employ a standard microprocessor (µP) interface. 3-state data outputs are configured to operate with 12-bit data buses. Data-access and bus-release timing specifications are compatible with most popular µPs without resorting to wait states. All logic inputs and outputs are TTL/CMOS compatible.

Applications

Digital-Signal Processing

Audio and Telecom Processing

Speech Recognition and Synthesis

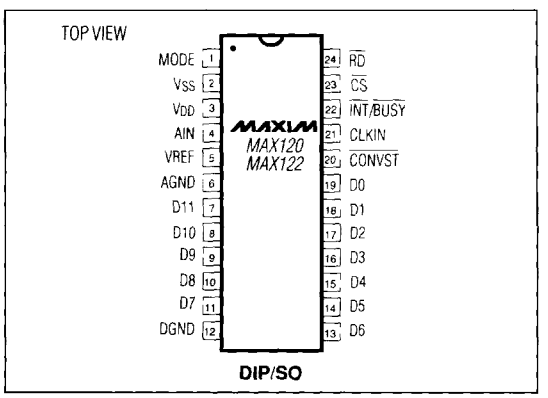
High-Speed Data Acquisition

Spectrum Analysis

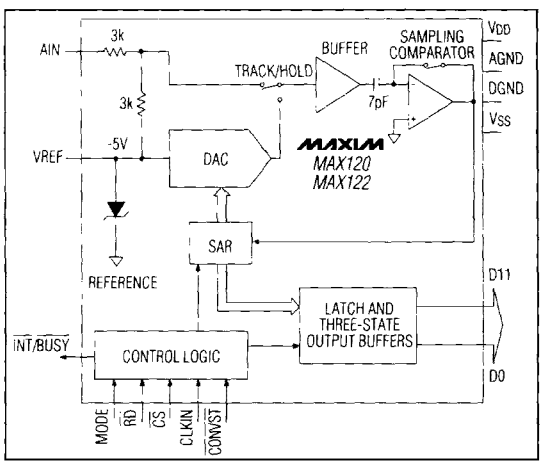
Features

- **12-Bit Resolution**
- **No Missing Codes Over Temperature**
- **20ppm°/C, -5V Internal Reference**
- **1.6µs Conversion Time/500ksps Throughput (MAX120)**
- **2.6µs Conversion Time/333ksps Throughput (MAX122)**
- **Low Noise and Distortion:**
  70 dB Min SINAD;
  -77 dB Max THD (MAX122)
- **Low Power Dissipation: 210mW**
- **Separate Track/Hold Control Input**
- **Continuous-Conversion Mode Available**
- **±5V Input Range, Overvoltage Tolerant to ±15V**
- **24-Pin Narrow DIP and Wide SO Packages**

Pin Configuration



Functional Diagram



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500ksps 12-Bit ADCs with Track/Hold and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +6V
V_{SS} to DGND ..... +0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs/Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.70mW/°C above +70°C) 727mW
SO (derate 11.76mW/°C above +70°C) 941mW
CERDIP (derate 12.50W/°C above +70°C) 1000mW

Operating Temperature Ranges:
MAX12_C__ ..... 0°C to +70°C
MAX12_E__ ..... -40°C to +85°C
MAX12_MRG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Differential Nonlinearity (Note 1)	DNL	No missing codes over temp range	MAX122A			±3/4	LSB
			MAX120, MAX122B			±1	
Integral Non-linearity (Note 1)	INL		MAX122A			±3/4	LSB
			MAX120, MAX122B			±1	
Bipolar Zero Error (Note 1)		Code 00..00 to 00..01 transition, near AIN = 0V				±3	LSB
		Temperature drift			±0.005		LSB/°C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error: T_A = +25°C				±8	LSB
Full-Scale Temperature Drift		Excluding reference			±1		ppm/°C
Power-Supply Rejection Ratio (Change in FS, Note 3)	PSRR	V_{DD} only, 5V to ±5%			±1/4	±3/4	LSB
		V_{SS} only, -12V to ±10%			±1/4	±1	
		V_{SS} only, -15V to ±5%			±1/4	±1	
ANALOG INPUT							
Input Range				-5		+5	V
Input Current		AIN = +5V (approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 4)						10	pF
Full-Power Input Bandwidth					1.5		MHz
REFERENCE							
Output Voltage		No external load, AIN = 5V, T_A = +25°C		-5.02		-4.98	V
External Load Regulation		0mA < I_{SINK} < 5mA, AIN = 0V				5	mV
Temperature Drift (Note 5)		MAX12_C/E				±20	ppm/°C
		MAX12_M				±25	
Supply Rejection		V_{DD} only, +5V to ±5%			0.6		mV
		V_{SS} only, -12V to ±10%			0.6		
		V_{SS} only, -15V to ±5%			0.6		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX120: f_S = 500kHz, AIN = ±5Vp-p, 100kHz, Note 4) (MAX122: f_S = 333kHz, AIN = ±5Vp-p, 50kHz, Note 4)							
Signal-to-Noise Plus Distortion	S/(N+D)	MAX120		69	70		dB
		MAX122		70	71.5		
Total Harmonic Distortion (First Five Harmonics)	THD	MAX120			-80	-75	dB
		MAX122			-82	-77	
Spurious-Free Dynamic Range	SFDR	MAX120		75	80		dB
		MAX122		77	82		
Intermodulation Distribution (2nd-Order Terms)	IMD	MAX120 f_A = 98kHz, f_B = 102kHz			-75		dB
		MAX122 f_A = 49kHz, f_B = 51kHz			-75		
CONVERSION TIME							
Synchronous	t_{CONV}	13t_{CLK}	MAX120			1.63	µs
			MAX122			2.60	
Clock Frequency	f_{CLK}		MAX120	0.1		8	MHz
			MAX122	0.1		5	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 4)						10	pF
Input Current		V_{IN} = 0V or V_{DD}				±5	µA
DIGITAL OUTPUTS ($\overline{INT}$/$\overline{BUSY}$, D11-D0)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA		V_{DD} - 0.5			V
Leakage Current	I_{LKG}	V_{IN} = 0V or V_{DD}, D11-D0				±5	µA
Output Capacitance (Note 4)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	Guaranteed by supply rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	Guaranteed by supply rejection test		-10.80		-15.75	V
Positive Supply Current	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V			9	15	mA
Negative Supply Current	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V			14	20	mA
Power Dissipation		V_{DD} = 5V, V_{SS} = -12V, AIN = 0V, $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V			210	315	mW

Note 1: These tests are performed at V_{DD} = 5V, V_{SS} = -15V. Operation over supply is guaranteed by supply rejection tests.
Note 2: Ideal full-scale transition is at +5V -3/2LSB = +4.9963V, adjusted for offset error.
Note 3: Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage = (FS at nominal supply) - (FS at nominal supply ± tolerance), expressed in LSBs.
Note 4: For design guidance only, not tested.
Note 5: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as TC = (ΔVREF)/VREF) /(ΔT)

500ksps 12-Bit ADCs with Track/Hold and Reference

TIMING CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = -12V or -15V, 100% tested, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX12_C/E			MAX12_M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}		0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0			0			ns
$\overline{CONVST}$ Pulse Width	t_{CW}		30			30			30			ns
$\overline{RD}$ Pulse Width	t_{RW}		t_{DA}			t_{DA}			t_{DA}			ns
Data-Access Time	t_{DA}	C_L = 100pF		40	75			100			120	ns
Bus-Relinquish Time	t_{DH}			30	50			65			80	ns
$\overline{RD}$ or $\overline{CONVST}$ to $\overline{BUSY}$	t_{B0}	C_L = 50pF		30	75			100			120	ns
CLKIN to $\overline{BUSY}$ or $\overline{INT}$	t_{B1}	C_L = 50pF		70	110			150			180	ns
CLKIN to $\overline{BUSY}$ Low	t_{B2}	In Mode 5		45	90			120			150	ns
$\overline{RD}$ to $\overline{INT}$ High	t_{IH}	C_L = 50pF		30	50			75			90	ns
$\overline{BUSY}$ or $\overline{INT}$ to Data Valid	t_{BD}	C_L (Data) = 100pF, C_L ($\overline{INT}$, $\overline{BUSY}$) = 50pF			20			30			35	ns
Acquisition Time (Note 7)	t_{AQ}		350			350			400			ns
Aperture Delay (Note 7)	t_{AP}			10								ns
Aperture Jitter (Note 7)				30								ps
Clock Setup/Hold Time (Note 7)	t_{CK}		10		50	10		50	10		50	ns

Note 6: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Output delays are measured to +0.8V if going low, or +2.4V if going high. For bus-relinquish time, a change of 0.5V is measured. See Figures 1 and 2 for load circuits.

Note 7: For design guidance only, not tested.