SGS-THOMSON MICROELECTRONICS

SGSP574
SGSP575

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

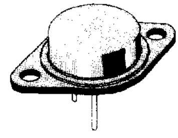
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP574	450 V	0.7 Ω	9 A
SGSP575	400 V	0.55 Ω	10 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR SMPS UPTO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT >100kHz
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

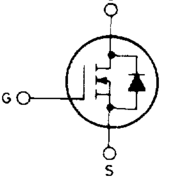
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Fast switching and easy drive make these POWER MOS transistors ideal for high voltage switching applications. These applications include electronic welders, switched mode power supplies and sonar equipment.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP574	SGSP575	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	450	400	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	450	400	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	9	10	A
I_D	Drain current (cont.) at $T_c=100°C$	5.6	6.3	A
I_{DM} (•)	Drain current (pulsed)	40	40	A
I_{DLM} (•)	Drain inductive current, clamped	40	40	A
P_{tot}	Total dissipation at $T_c<25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit

OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP574** for **SGSP575**	 450 400			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA

ON (*)

$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4.5 A for **SGSP574** I_D = 5 A for **SGSP575** V_{GS} = 10 V T_c = 100°C I_D = 4.5 A for **SGSP574** I_D = 5 A for **SGSP575**			 0.7 0.55 1.4 1.1	 Ω Ω Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 5 A	6			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	2100 390 260	pF pF pF

SWITCHING

$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 225 V I_D = 5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 45 125 30	40 60 165 40	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

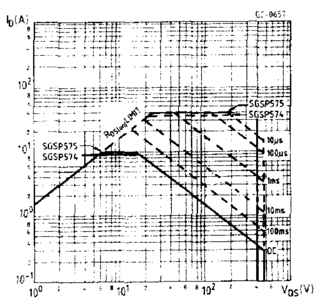
Parameters		Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

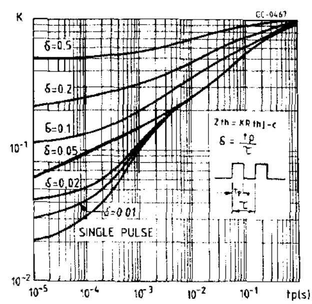
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	for **SGSP574** for **SGSP575**			9 10	A A
I_{SDM} (•)	Source-drain current (pulsed)				40	A
V_{SD}	Forward on voltage	V_{GS} = 0 I_{SD} = 9 A for **SGSP574** I_{SD} = 10 A for **SGSP575**			 1.2 1.2	 V V
t_{rr}	Reverse recovery time	I_{SD} = 10 A V_{GS} = 0 di/dt = 100 A/μs		420		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

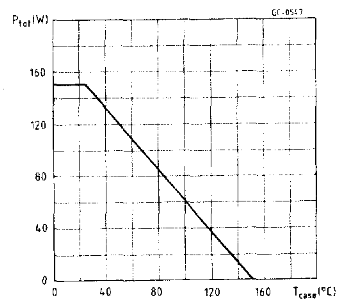
Safe operating areas



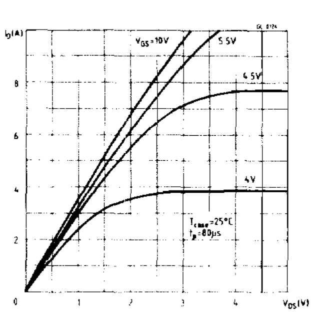
Thermal impedance



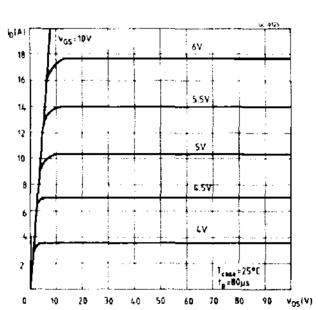
Derating curve



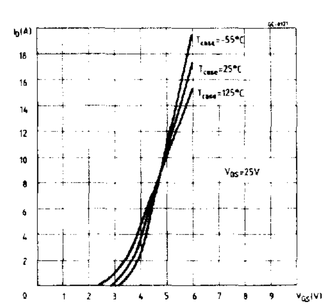
Output characteristics



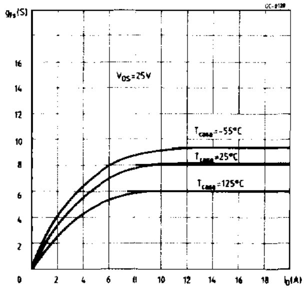
Output characteristics



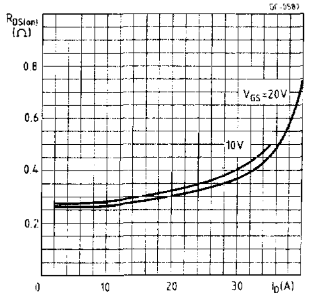
Transfer characteristics



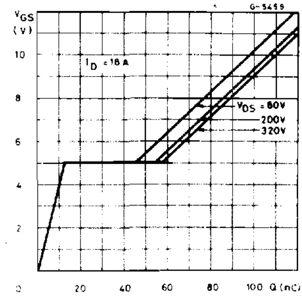
Transconductance



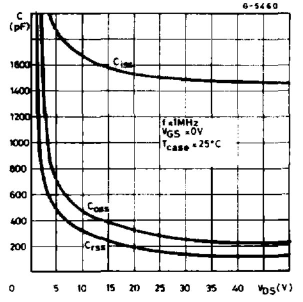
Static drain-source on resistance



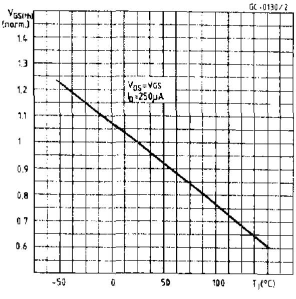
Gate charge vs gate-source voltage



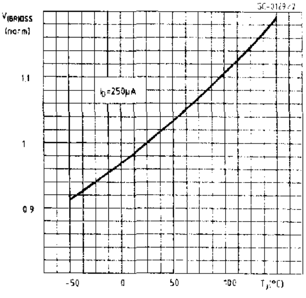
Capacitance variation



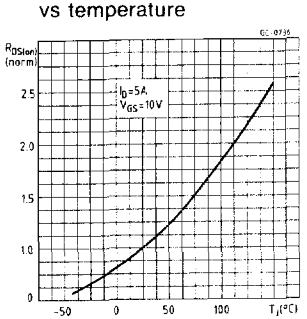
Normalized gate threshold voltage vs temperature



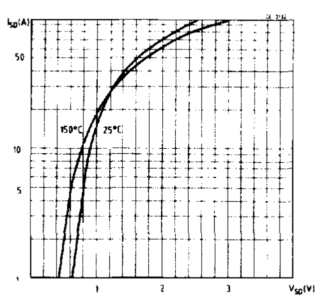
Normalized breakdown voltage vs temperature



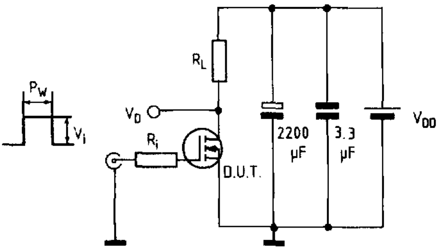
Normalized on resistance vs temperature



Source-drain diode forward characteristics

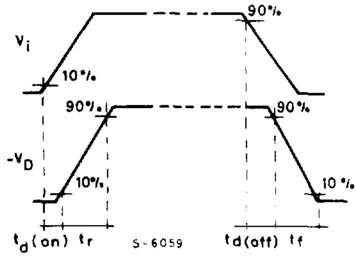


Switching times test circuit for resistive load

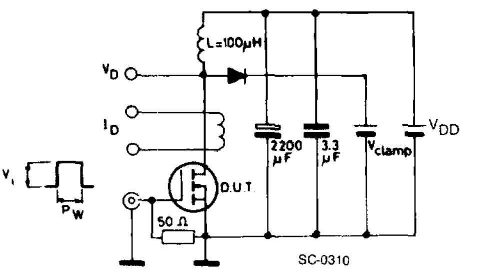


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

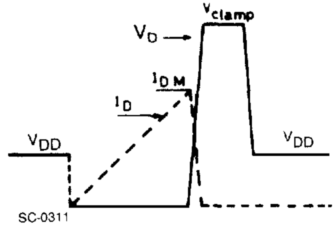


Clamped inductive load test circuit

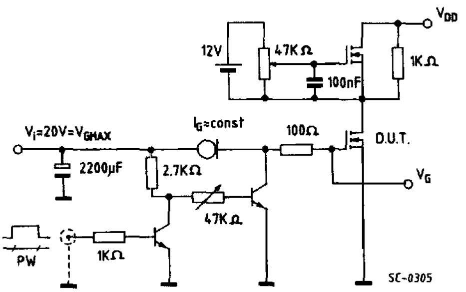


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit