

# LC898111AXA

# LC898111AXB



ON Semiconductor®

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CMOS LSI

## OIS Controller & Driver

### Overview

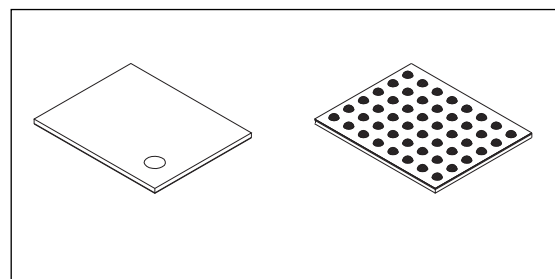
The LC898111AXA and the LC898111AXB are image stabilization system control LSIs for smartphone camera modules.

The LSIs have built-in digital signal processing circuits, such as a 2ch saturation H-Bridge Driver and a Flexible Filter circuit, and control VCM type actuators.

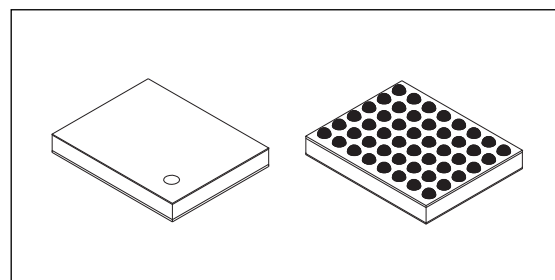
The LC898111AXA and the LC898111AXB are identical LSIs except for the dimensions, i.e. XA has WLP thickness, max. 0.33 mm without back coat (B/C) and XB has WLP thickness, max. 0.69 mm with B/C.

### Function

- Digital signal processing LSI (Logic LSI)
  - Built-in digital servo circuit
  - Built-in Gyro filter
  - AD converter
    - 12-bit
    - input 5ch
    - Equipped with a sample-hold circuit
  - DA converter
    - 8-bit
    - Output 2ch (Constant current Bias : max 7mA)
  - Built-in Serial I/F circuit (2-wire I<sup>2</sup>C-Bus or 4-wire SPI Bus interface)
  - Built-in Hall Bias circuit
  - Built-in Hall Amp (Gain of Opamp : x25, x50, x75, x100, x150, x200)
  - Built-in OSC (Oscillator)
    - 48MHz ± 5% (Frequency adjustment function)
  - External Clock input is possible from TSTCLK (48MHz ± 5%)
  - Built-in LDO (Low Drop-Out regulator)
  - Digital Gyro I/F for the companies (SPI Bus)  
(Please refer for the details)
  - Support Hall sensor and Photo Reflector as means to detect a position
- Motor Driver
  - Saturation-drive H bridge x2ch
  - I<sub>Q</sub> max : 220mA
- Package
  - LC898111AXA : WLP48J  
(2.57mm x 3.22mm, thickness max 0.33mm, without B/C)
  - LC898111AXB : WLP48  
(2.57mm x 3.22mm, thickness max 0.69mm, with B/C)
  - Pb-free
  - Halogen Free
- Power supply voltage
  - Logic : DVDD30 = 2.6 to 3.6 V
  - Driver : VM = 2.6 to 3.6 V



WLP48J



WLP48

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

\* I<sup>2</sup>C Bus is a trademark of Philips Corporation.

# LC898111AXA, LC898111AXB

## Block Diagram

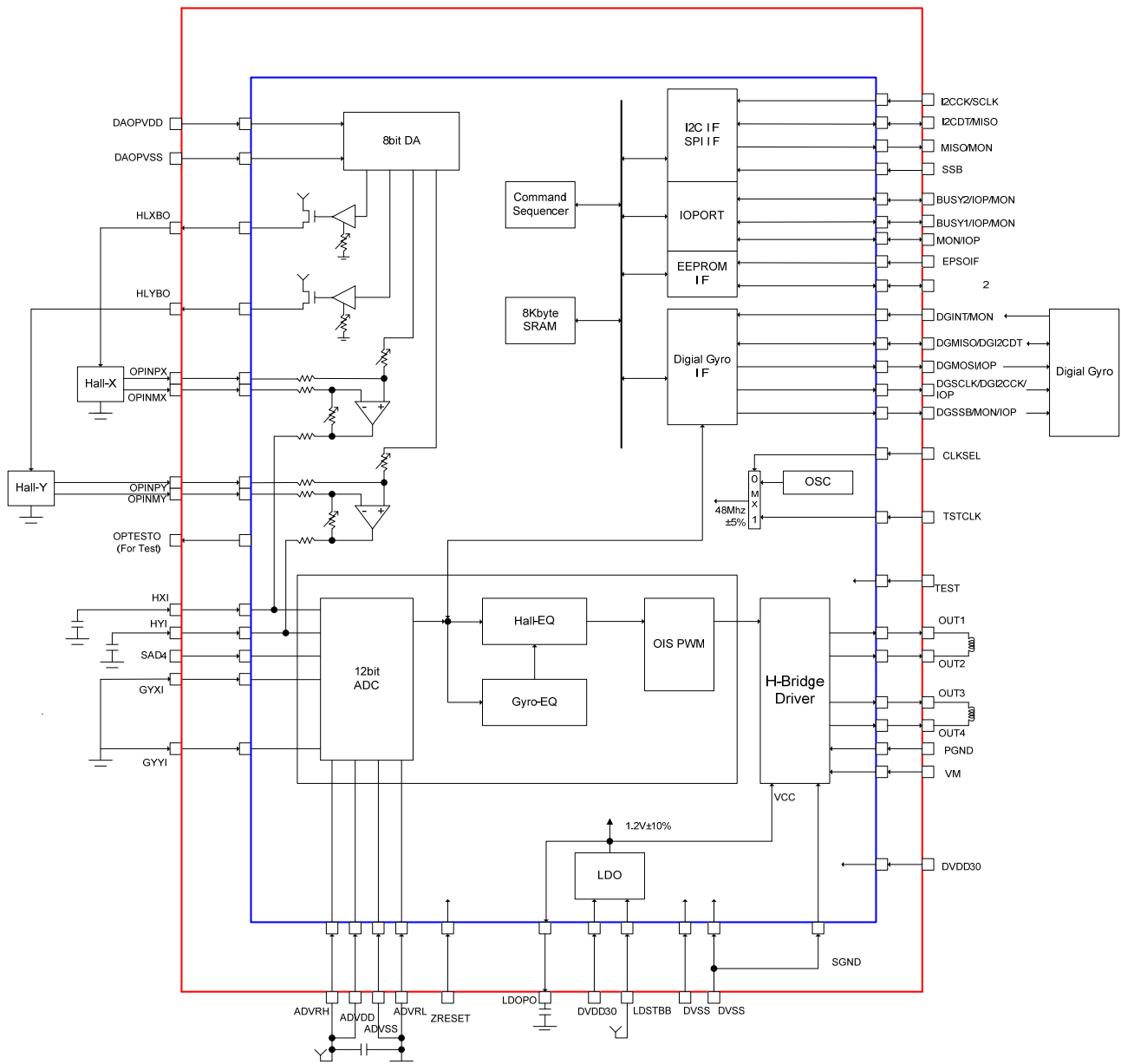
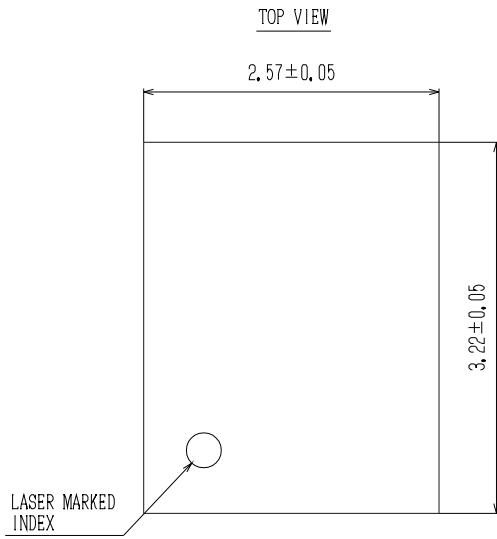


Figure 3.1 Example of wiring diagram (Hall) in LC898111AXA/XB

# LC898111AXA, LC898111AXB

LC898111AXA

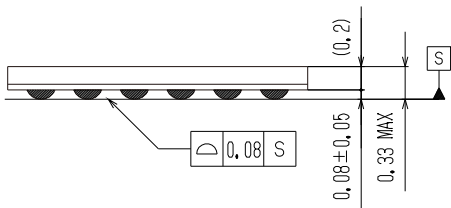
PACKAGE DIMENSIONS  
WLP48J(3.22X2.57)



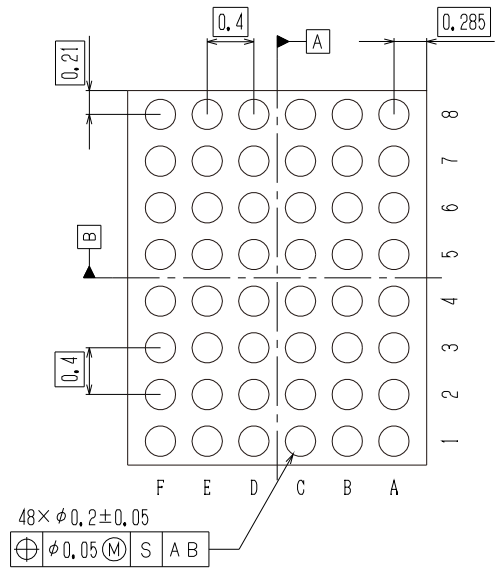
SIDE VIEW



SIDE VIEW



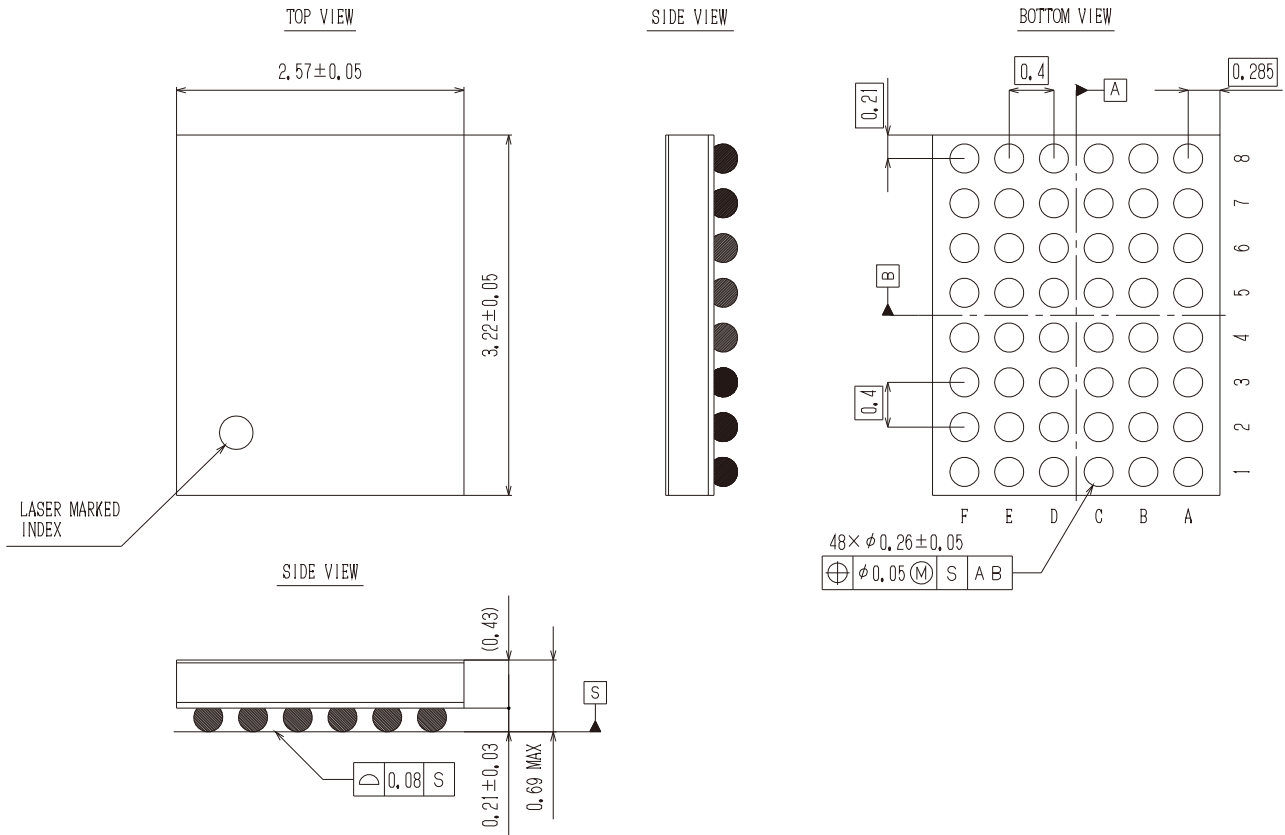
BOTTOM VIEW



# LC898111AXA, LC898111AXB

LC898111AXB

PACKAGE DIMENSIONS  
WLP48(3.22X2.57)



# LC898111AXA, LC898111AXB

## Pin Assign (WLP48J/WLP48)

Top View

1	OPTESTO	OPINPY	ADVDD	ADVSS	GYI	HXI
2	HLXBO	OPINMY	ADVRH	GYXI	DVSS	I2CDT
3	EPSOIF	DAOPVDD	ADVRL	HYI	EPCSBIF2	I2CCK
4	DVDD30	DAOPVSS	OPINPX	SAD4	SSB	MISO
5	BUSY2	HLYBO	OPINMX	ZRESET	LDOPO	DVDD30
6	BUSY1	TEST	DVSS	TSTCLK	LDSTBB	DGSCCLK
7	VM	MON	CLKSEL	DGMOSI	DGMISO	DGINT
8	OUT4	OUT3	OUT2	OUT1	PGND	DGSSB
	F	E	D	C	B	A

	Driver
	DAC
	OpAmp
	ADC

	EEPROM i/f
	Logic GND
	IO VDD (2.6V to 3.6V)
	Logic Core VDD (1.14 to 1.26V)

## LC898111AXA, LC898111AXB

<typ> I : INPUT, O : OUTPUT, B : BIDIRECTION, P : Power, GND

Ball No	Pin Name	type	Description
F8	OUT4	O	Driver Output
F7	VM	P	Driver VDD (2.6V to 3.6V)
F6	BUSY1	B	EEPROM I/F (at I <sup>2</sup> C type EEPROM ) / BUSY1(O) / General-purpose IOPORT(B) / inner signal Monitor(O)
F5	BUSY2	B	BUSY2(O) / General-purpose IOPORT(B) / inner signal Monitor(O)
F4	DVDD30	P	Logic IO VDD (2.6V to 3.6V)
F3	EPSOIF	I	EEPROM I/F
F2	HLXBO	O	Hall-X Bias (Current Drive)
F1	OPTESTO	O	OpAmp Test out
E8	OUT3	O	Driver output
E7	MON	B	inner signal monitor / General-purpose IOPORT
E6	TEST	I	SPI & External clock case sets "1" other cases set "0"
E5	HLYBO	O	Hall-Y Bias (Current Drive)
E4	DAOPVSS	P	DA&Opamp VSS
E3	DAOPVDD	P	DA&Opamp VDD (2.6V to 3.6V)
E2	OPINMY	I	Hall-Y OpAmp input-
E1	OPINPY	I	Hall-Y OpAmp input+
D8	OUT2	O	Driver Output
D7	CLKSEL	I	change pin of OSC(0) and External clock(1)
D6	DVSS	P	Logic GND
D5	OPINMX	I	Hall-X OpAmp input-
D4	OPINPX	I	Hall-X OpAmp input+
D3	ADVRL	I	ADC Reference Voltage Low input
D2	ADVRLH	I	ADC Reference Voltage High input
D1	ADVDD	P	AD VDD (2.6V to 3.6V)
C8	OUT1	O	Driver Output
C7	DGMOSI	B	Digital Gyro (4-wire)IF data(O) / HPS Control(O) / General-purpose IOPORT(B)
C6	TSTCLK	I	CLKSEL=1 : External Clock, CLKSEL=0 : change pin of I <sup>2</sup> C(0) and SPI(1)
C5	ZRESET	I	Hard Wafer Reset
C4	SAD4	I	General-purpose AD input
C3	HYI	I	Hall-Y AD input
C2	GYXI	I	Gyro-X AD input
C1	ADVSS	P	AD GND
B8	PGND	P	Driver GND
B7	DGMISO	B	Digital Gyro SPI IF Data( I ) / Digital Gyro I <sup>2</sup> C IF Data(B)
B6	LDSTBB	I	LDO Standby (0 : Standby On, 1 : Standby Off)
B5	LDOPO	P	LDO Power supply out (Logic Core VDD (1.14V to 1.26V))
B4	SSB	I	SPI I/F Chip Select / VDD fix at I <sup>2</sup> C i/f
B3	EPCSBIF2	B	EEPROM I/F
B2	DVSS	P	Logic GND
B1	GYI	I	Gyro-Y AD input
A8	DGSSB	B	Digital Gyro SPI IF Chip Select(O) / inner signal monitor(O) / General-purpose IOPORT(B)
A7	DGINT	B	Digital Gyro SPI IF Data Busy( I ) / inner signal monitor(O) / General-purpose IOPORT(B)
A6	DGSCLK	B	Digital Gyro SPI IF clock (O) / Digital Gyro I <sup>2</sup> C IF clock(O) / HPS Control 1(O) / General-purpose IOPORT (B)
A5	DVDD30	P	Logic IO VDD (2.6V to 3.6V) and power supply to LDO
A4	MISO	O	SPI I/F Data / General-purpose IOPORT / inner signal monitor
A3	I2CCK	I	I <sup>2</sup> C_IF clock / SPI IF clock
A2	I2CDT	B	I <sup>2</sup> C_IF Data(B) / SPI IF Data
A1	HXI	I	Hall-X AD input

## LC898111AXA, LC898111AXB

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### ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898111AXA-MH	WLP48J(3.22X2.57) (Pb-Free / Halogen Free)	5000 / Tape & Reel
LC898111AXB-MH	WLP48(3.22X2.57) (Pb-Free / Halogen Free)	5000 / Tape & Reel

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