PAC107 SINGLE-CHIP CMOS QQVGA IMAGE SENSOR with EMBEDDED TWIN-TURBO 8032 MICRO-PROCESSOR

General Description

The PAC107 is a QQVGA CMOS imager sensor with an embedded 40Mhz Twin-Turbo 8032 Micro Control Unit (MCU). To have excellent application flexibility, the PAC107 controls the embedded CMOS imager through 8032's SFR. A one-cycle execution multiplier is available for instruction "MUL". It's suitable for recognition applications.

The PAC107 had on-chip 16KB program ROM and 1KB on-chip SRAM. There are two 8-bit PWM ports with pre-scale function. Hence melody play and simple board level control function can be implemented. A dedicate image data write to External SRAM sequence is provided to have a fast and efficient image data caption through Port0 of 8032. The exposure-time control of imager can be done by on-chip real time hardware control, and extend the operation luminance range through firmware.

Features

- **164x124 pixels, 1/11" Lens**
- **Auto/Manual exposure-gain control.**
- **Automatic de-flicker**
- **Firmware controlled imager power down**
- **On-chip 10-bit ADC**
- **Continuous variable exposure time**
- **Continuous variable frame time(1/2s~1/30s)**
- **Crystal mode: 4~40 MHz**
- **Operating voltage: 2.6V ~ 3.6V**
- **RISC-like Twin-turbo 8032**
- **2 UART with programmable baud-rate**
- **2 PWM**
- **1 cycle execution MUL instruction**
- **Software controllable Sensor shut down**
- **MOVX direct dump image data to SRAM**
- **1KB on-chip SRAM**
- **16KB on-chip program ROM**
- **External program ROM bus supported**

Power Supply	2.6V ~ 3.6V	**FPN**	< 0.2% saturation
Array Elements	164 x 124	**PGA Gain**	16X (24dB)
Optical Format	1/11 "	**Digital Gain**	4X(12dB)
Pixel Size	7.25 μm x 7.25μm	**Frame Rate**	60fps
Master Clock	Up to 40MHz	**Scan Mode**	Progressive
Max. Pixel Rate	1.5MHz	**Package**	80-pin LCC and 48-pin LCC

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1. Pin Description

1.1 80-pin LCC

Pin No.	Name	Type	Definition
1	VRT	Bypass	Top-voltage reference for analog circuit
2	GNDA	G	Analog ground
3	/EA	I	Enable bar of external ROM, “1” for internal ROM
4	ROM_AR13	O	Address for external ROM, bit 13
5	ROM_AR12	O	Address for external ROM, bit 12
6	ROM_AR11	O	Address for external ROM, bit 11
7	PWM1	O	8032, Programmable Pulse-width-modulation output
8	ROM_AR10	O	Address for external ROM, bit 10
9	ROM_AR9	O	Address for external ROM, bit 9
10	ALE	O	Address latch pulse for SRAM-address
11	RST	I	Chip reset
12	ROM_AR8	O	Address for external ROM, bit 8
13	ROM_AR7	O	Address for external ROM, bit 7
14	ROM_AR6	O	Address for external ROM, bit 6
15	ROM_AR5	O	Address for external ROM, bit 5
16	VDDD	P	Digital power
17	ROM_AR4	O	Address for external ROM, bit 4
18	ROM_AR3	O	Address for external ROM, bit 3
19	ROM_AR2	O	Address for external ROM, bit 2
20	ROM_AR1	O	Address for external ROM, bit 1
21	ROM_AR0	O	Address for external ROM, bit 0
22	ROM_D0	I	Data from external ROM, bit 0
23	ROM_D1	I	Data from external ROM, bit 1
24	GNDD	G	Digital ground
25	ROM_D2	I	Data from external ROM, bit 2
26	ROM_D3	I	Data from external ROM, bit 3
27	ROM_D4	I	Data from external ROM, bit 4
28	ROM_D5	I	Data from external ROM, bit 5
29	ROM_D6	I	Data from external ROM, bit 6
30	P3_6(/WR)	O	8032, P3_6 (/WR) – Write pulse of SRAM
31	P3_7(/RD)	O	8032, P3_7 (/RD) – Read pulse of SRAM
32	NC	NC	Not connected
33	ROM_D7	I	Data from external ROM, bit 7
34	P2_0	IO	8032, P2_0
35	P2_1	IO	8032, P2_1
36	PWM2	O	8032, Programmable Pulse-width-modulation output
37	P2_2	IO	8032, P2_2
38	P2_3	IO	8032, P2_3
39	VDDD	P	Digital power

40	GNDD	G	Digital ground
41	P2_4	IO	8032, P2_4
42	P2_5	IO	8032, P2_5
43	P2_6	IO	8032, P2_6
44	P2_7	IO	8032, P2_7
45	P3_3(/INT1)	IO	8032, P3_3
46	P3_4(T0)	IO	8032, P3_4
47	P1_2(/RXD1)	IO	8032, P1_2(/RXD1) – UART1 Rxd
48	P1_1(T2EX)	IO	8032, P1_1
49	P1_0(T2)	IO	8032, P1_0
50	P3_5(T1)	IO	8032, P3_5
51	NC	NC	Not connected
52	LCD_4B0	O	Specific data pin connect to color LCM
53	LCD_4B1	O	Specific data pin connect to color LCM
54	XTAL1	Clock	Differential input of Crystal Oscillator
55	XTAL2	Clock	Differential output of Crystal Oscillator
56	LCD_4B2	O	Specific data pin connect to color LCM
57	LCD_4B3	O	Specific data pin connect to color LCM
58	VDDD	P	Digital power
59	GNDD	G	Digital ground
60	LCD_WRB	O	Specific write pulse pin connect to color LCM
61	P1_6	IO	8032, P1_6
62	P0_0	IO	8032, P0_0
63	P0_1	IO	8032, P0_1
64	P0_2	IO	8032, P0_2
65	P0_3	IO	8032, P0_3
66	P1_5	IO	8032, P1_5
67	P0_4	IO	8032, P0_4
68	P0_5	IO	8032, P0_5
69	P0_6	IO	8032, P0_6
70	P0_7	IO	8032, P0_7
71	NC	NC	Not connected
72	P1_4	IO	8032, P1_4
73	P1_3(/TXD1)	IO	8032, P1_3(/TXD1) – UART1 Txd
74	P3_1(/TXD0)	IO	8032, P3_1(/TXD0) – UART0 Txd
75	P3_0(/RXD0)	IO	8032, P3_0(/RXD0) – UART0 Rxd
76	P3_2(/INT0)	I	P3_2(/INT0) – INT0 to ASIC
77	VDDA	P	Analog power
78	VDDAY1	Bypass	Sensor power
79	VRB	Bypass	Bottom-voltage reference for analog circuit
80	VCM	Bypass	Common-mode-voltage reference for analog circuit

1.2 48-pin LCC

Pin No.	Name	Type	Definition
1	VDDA	P	Analog power
2	VDDAY1	Bypass	Sensor power
3	VRB	Bypass	Bottom-voltage reference for analog circuit
4	VCM	Bypass	Common-mode-voltage reference for analog circuit
5	VRT	Bypass	Top-voltage reference for analog circuit
6	GNDA	G	Analog ground
7	/EA	I	Enable bar of external ROM, “1” for internal ROM
8	NC	NC	Not connected
9	NC	NC	Not connected
10	ALE	O	Address latch pulse for SRAM-address
11	RST	I	Chip reset
12	VDDD	P	Digital power
13	NC	NC	Not connected
14	NC	NC	Not connected
15	GNDD	G	Digital ground
16	P3_6 (/WR)	O	8032, P3_6 (/WR) – Write pulse of SRAM
17	P3_7 (/RD)	O	8032, P3_7 (/RD) – Read pulse of SRAM
18	P2_0	IO	8032, P2_0
19	P2_1	IO	8032, P2_1
20	PWM2	O	8032, Programmable Pulse-width-modulation output
21	P2_2	IO	8032, P2_2
22	P2_3	IO	8032, P2_3
23	P2_4	IO	8032, P2_4
24	P2_5	IO	8032, P2_5
25	P2_6	IO	8032, P2_6
26	P2_7	IO	8032, P2_7
27	P1_2	IO	8032, P1_2
28	P1_1	IO	8032, P1_1
29	P1_0	IO	8032, P1_0
30	P3_5	IO	8032, P3_5
31	XTAL1	Clock	Differential input of Crystal Oscillator
32	XTAL2	Clock	Differential input of Crystal Oscillator
33	VDDD	P	Digital power
34	P1_6	IO	8032, P1_6
35	P0_0	IO	8032, P0_0
36	P0_1	IO	8032, P0_1
37	P0_2	IO	8032, P0_2
38	P0_3	IO	8032, P0_3
39	P0_4	IO	8032, P0_4
40	P0_5	IO	8032, P0_5

41	P0_6	IO	8032, P0_6
42	P0_7	IO	8032, P0_7
43	GNDD	G	Digital ground
44	P1_4	IO	8032, P1_4
45	P1_3	IO	8032, P1_3
46	P3_1(/TXD)	IO	8032, P3_1(/TXD) – UART Txd
47	P3_0(/RXD)	IO	8032, P3_0(/RXD) – UART Rxd
48	P3_2(/INT0)	I	P3_2(/INT0) – INT0 to ASIC

2. Block Diagram

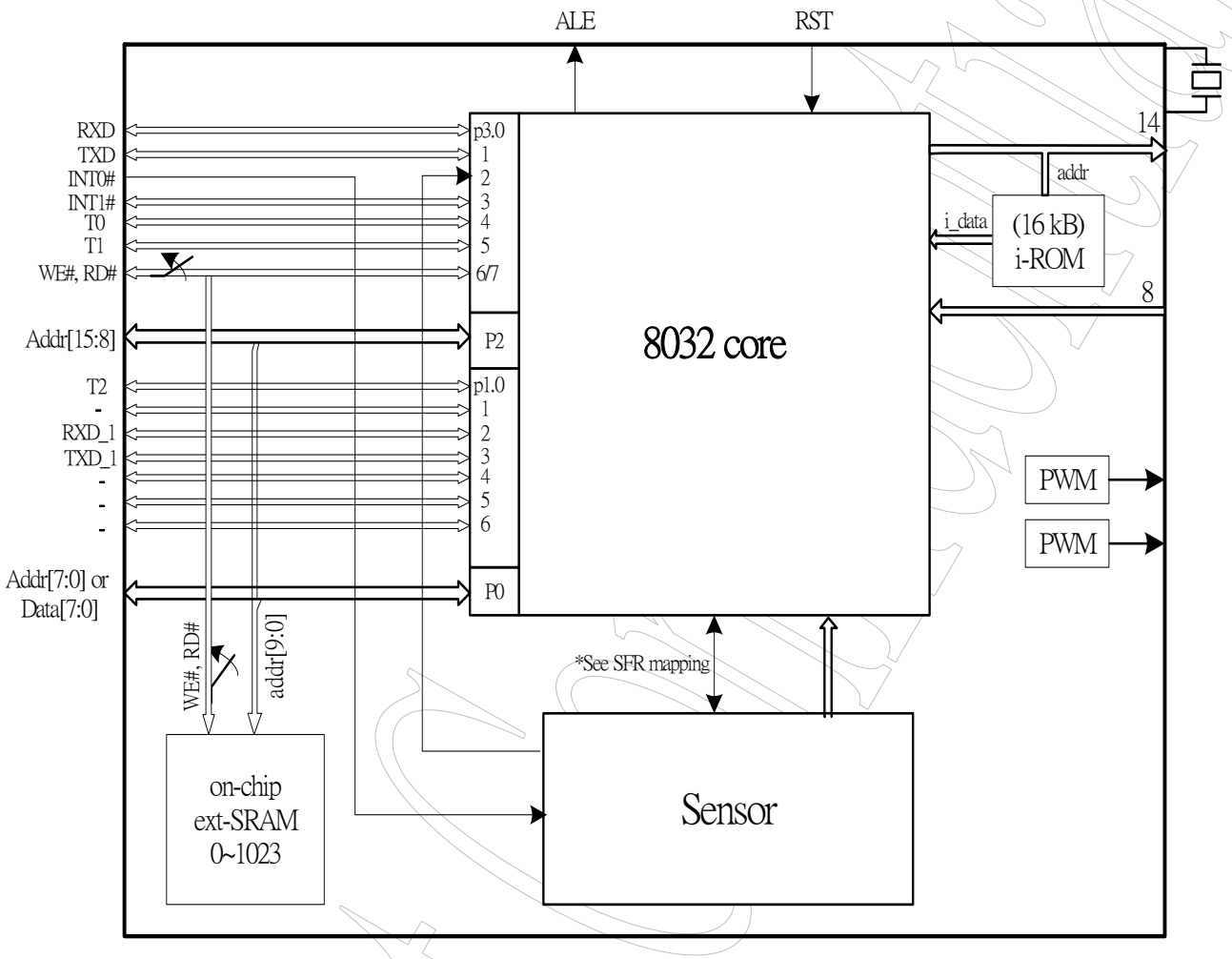


Fig 2.1 – Block diagram of PAC107

As the block diagram of PAC107 is shown in Figure 2.1. By pulling the CSB register in SFR(Special function register) to low, the 164x124 sensor starts to produce a signal according to the amount of the light integrated in pixels. The integrated analog signal will be readout and amplifier with ADC output in 8-bit. The output 8 bit digital sensor data then be received by 8051 core by software.

16KB program ROM and 1kB SRAM is provided in PAC107 and two PWM ports are supported.

3. Register table of CMOS Image Sensor

Address	Name	R/W	Default	Recommended setting	Description
Reg_0[7:0]	Pdct_id[11:4]	R	0000_0001	-	Product ID
Reg_1[7:4]	pdct_id[3:0]	R	1001	-	Product ID
Reg_1[3:0]	ver_id[3:0]	R	0000	-	Version ID
Reg_2[7:1]	Ysum_report[6:0]	R	-	-	Ysum report in AE/AG calculation
Reg_2[0]	s_valid	R	-	-	Ysum valid flag
Reg_3[7]	RSV	-	-	-	Reserved
Reg_3[6:0]	AE_wait[6:0]	R/W	000_0001	0	Frame wait for AE/AG calculation
Reg_4[7:4]	Ysum_hi[3:0]	R/W	1010	-	Ysum high threshold
Reg_4[3:0]	Ysum_lo[3:0]	R/W	1000	-	Ysum low threshold
Reg_5[7:6]	AE_max[1:0]	R/W	11	-	Maximum AE index in Auto mode
Reg_5[5:1]	AG_max[4:0]	R/W	1_1111	-	Maximum Gain index in Auto mode
Reg_5[0]	dac[8]	R/W	0	-	Sign bit of DAC
Reg_6[7:0]	dac[7:0]	R/W	0000_0000	-	Magnitude of DAC
Reg_7[7]	RSV	-	-	-	Reserved
Reg_7[6:0]	ny3[6:0]	R/W	000_1011	0	Raw exposure set #4 for AE
Reg_8[7:0]	ne3[7:0]	R/W	0101_1000	0	Fine exposure set #4 for AE
Reg_9[7]	RSV	-	-	-	Reserved
Reg_9[6:0]	ny2[6:0]	R/W	010_1000	0	Raw exposure set #3 for AE
Reg_10[7:0]	ne2[7:0]	R/W	0000_1000	0	Fine exposure set #3 for AE
Reg_11[7]	RSV	-	-	-	Reserved
Reg_11[6:0]	ny1[6:0]	R/W	100_0100	010_1011	Raw exposure set #2 for AE
Reg_12[7:0]	ne1[7:0]	R/W	1000_1101	0	Fine exposure set #2 for AE
Reg_13[7:6]	RSV	-	-	-	Reserved
Reg_13[5:0]	np[5:0]	R/W	00_0110	01_0000	pxclk = sysclk / np
Reg_14[7:0]	lpf[7:0]	R/W	0111_1101	0111_1111	Line per frame
Reg_15[7]	adc8b	R/W	0	1	1: ADC 8_bit valid 0: ADC 10_bit valid
Reg_15[6:4]	comp[2:0]	R/W	011	-	Companding curve selection
Reg_15[3:2]	cgn_B[1:0]	R/W	10	11	Color gain for Blue
Reg_15[1:0]	cgn_R[1:0]	R/W	10	01	Color gain for Red
Reg_16[7:5]	RSV	-	-	-	Reserved
Reg_16[4:0]	pga[4:0]	R/W	0_0100	-	PGA global gain
Reg_17[7]	RSV	-	-	-	Reserved
Reg_17[6:0]	ny0[6:0]	R/W	110_0001	101_0110	Raw exposure set #1 for AE
Reg_18[7:0]	ne0[7:0]	R/W	0100_0111	0	Fine exposure set #1 for AE
Reg_19[7:1]	RSV	-	-	-	Reserved
Reg_19[0]	flag	R/W	0	-	Synchronization flag for I2C update
Reg_20[7:0]	RSV	-	1000_0000	-	Reserved
Reg_21[7]	Col_reverse	R/W	0	-	Line readout reverse
Reg_21[6:5]	Pack[1:0]	R/W	00	-	8, 4, 2, 1 bit packing selection

Reg_21[4]	Toyt	R/W	0	-	Toy timing enable
Reg_21[3]	aegenh	R/W	1	-	AE/AG enable
Reg_21[2:1]	Edge-gn[1:0]	R/W	00	-	Edge gain
Reg_21[0]	Vlrst_outh	R/W	0	0	External vlrst enable
Reg_22[7]	Shr_we2	R/W	1	0	CDS extension
Reg_22[6]	Intvddy	R/W	1	-	Internal array vdd
Reg_22[5]	Intvref	R/W	1	-	Internal voltage reference
Reg_22[4]	Cdsenh	R/W	1	-	CDS enable
Reg_22[3]	Dacenh	R/W	1	0	DAC enable
Reg_22[2]	Pgaenh	R/W	1	-	PGA enable
Reg_22[1]	Adcenh	R/W	1	-	ADC enable
Reg_22[0]	Dqioenl	R/W	0	-	DQIO enable / tri-stage
Reg_23[7]	vlrst_enh	R/W	0	0	vlrst enable
Reg_23[6]	Vr	R/W	0	1	Vref option
Reg_23[5]	Vy	R/W	0	1	Array vdd option
Reg_23[4:3]	Regfast[1:0]	R/W	00	-	Fast mode for Regulator
Reg_23[2]	Cdsfast	R/W	0	-	Fast mode for CDS
Reg_23[1]	Pgafast	R/W	0	-	Fast mode for PGA
Reg_23[0]	Adcfast	R/W	0	-	Fast mode for ADC
Reg_24[7:3]	RSV	R/W	-	-	Reserved
Reg_24[2]	Dacscan	R/W	0	-	DAC test mode
Reg_24[1]	Pgascan	R/W	0	-	PGA test mode
Reg_24[0]	Frstenl	R/W	1	-	Frame reset enable
Reg_25[7:1]	RSV	-	-	-	Reserved
Reg_25[0]	fast_i2c	R/W	0	-	Fast update for Reg_13 ~ Reg_18
Reg_26[7:5]	RSV	R/W-	-	-	Reserved
Reg_26[4:0]	Pga_report[4:0]	R	-	-	PGA code report (AE enable)
Reg_27[7:0]	Ne_report[7:0]	R	-	-	NE report (AE enable)
Reg_28[7]	RSV	-	-	-	Reserved
Reg)28[6:0]	Ny_report[6:0]	R	-	-	NY report (AE enable)

3.1. MEMORY ORGANIZATION

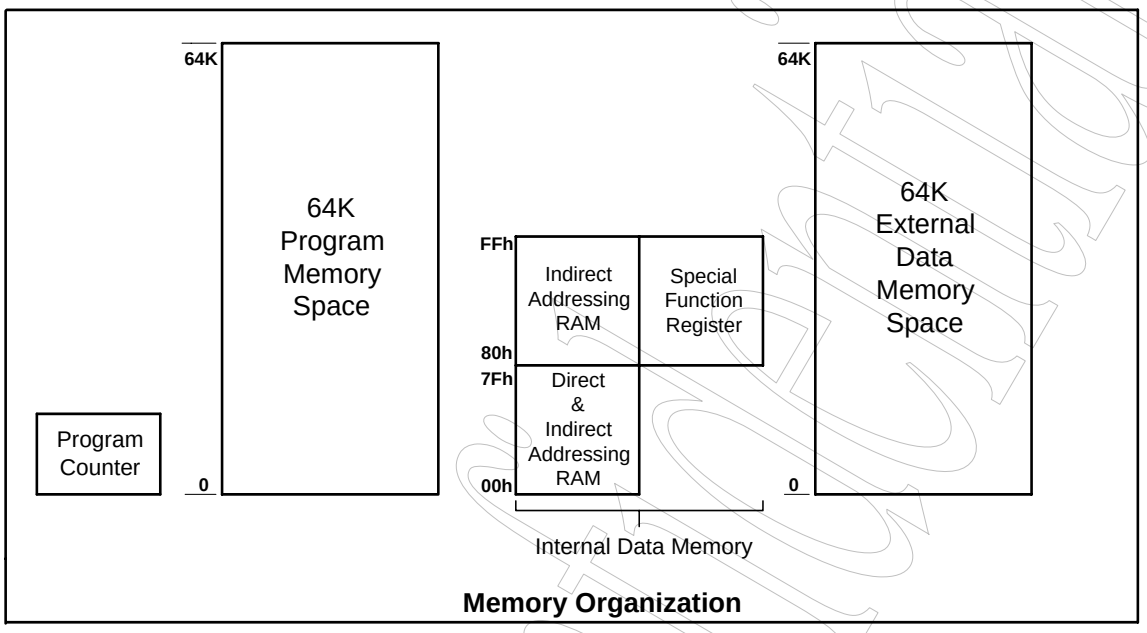
In the RISC 52 the memory is organized as three address spaces and the program counter. The memory spaces shown in memory map.

- 16-bit Program Counter
- 16kB Program Memory address space
- 64kB External Data Memory address space
- 256-byte Internal Data Memory address

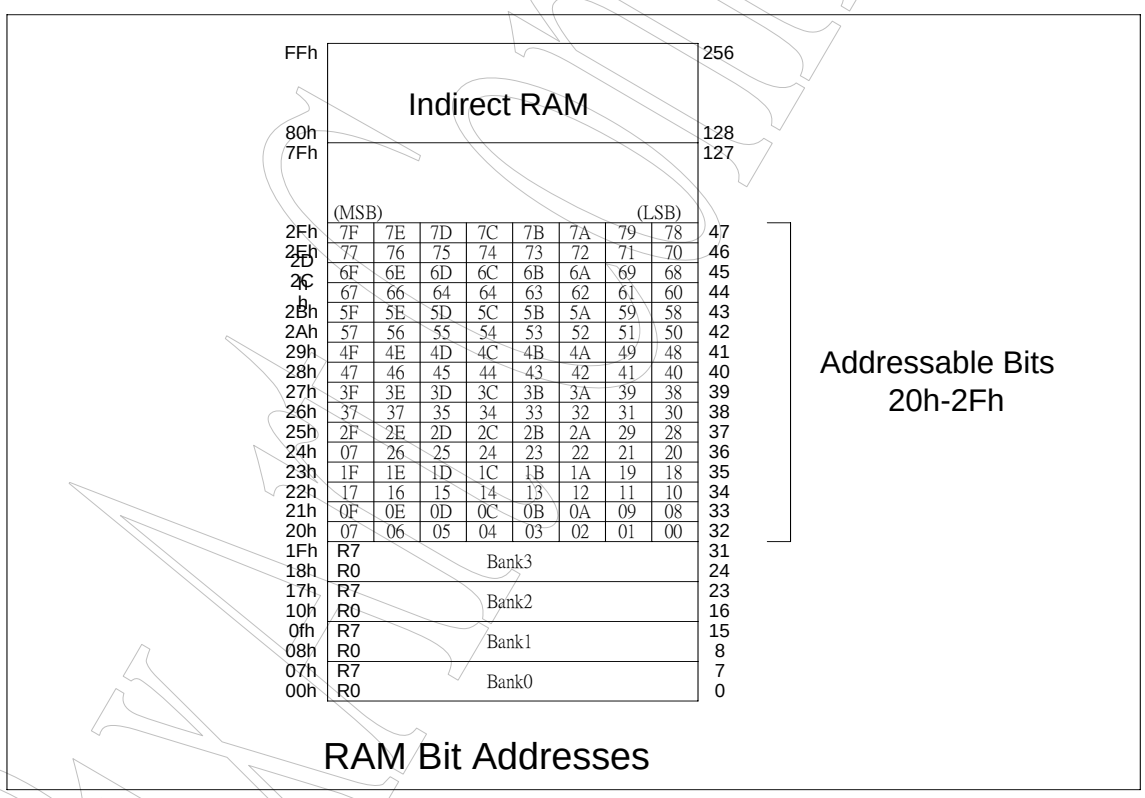
The 14-bit Program Counter register provides the RISC 52 with its 16kB addressing capabilities. The program Counter allows the user to execute calls and branches to any location within the Program Memory space. There are no instructions that permit program execution to move from the Program Memory space to any of the data memory spaces.

The 64k-byte External Data Memory address space is automatically accessed when the MOVX instruction is executed. Note that user can extend the addressable data RAM space by MUX the general I/O pins in port 1 and 3.

The Internal SRAM address space is 0 to 255 CPU internal usage. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit locations of the on-chip RAM are accessible through Direct Addressing.



Memory Organization



RAM Bit Addresses

3.2. Special Function Register Table

The Special Function Register address space is from 80h to FFh. All registers except the Program Counter and the four 8-Register Banks reside here. The SFRs are accessed by using direct addressing only. All of the SFRs are the compatible with standard 8032 with Image Sensor control registers. The SFR in red color are those different with standard 8032.

F8H								
F0H	B						PWM21conf	PWM11conf
E8H			CdInsWtSt			I2C	PixSt	Cap
E0H	ACC	PDCON			Vstart	Vend	Hstart	Hend
D8H	WDTCON				PWM2conf	PWM1conf	PWMData1	PWMData2
D0H	PSW							
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0H	SCON1	SBUF1			PMR	STATUS		
B8H	IP							
B0H	P3							
A8H	IE							
A0H	P2							
98H	SCON	SBUF						
90H	P1							
88H	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80H	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

B

Address:F0h

bit 7							bit 0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

The B Register is used for both a source and destination in MUL and DIV instructions.

ACC

Address:E0h

bit 7							bit 0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Accumulator.

PSW

Address: D0h

bit 7							bit 0
CY	AC	F0	RS1	RS0	OV	F1	PARITY

Program Status Word.

CY: Carry Flag

AC: Auxiliary-Carry Flag

F0: Flag 0 available to the user for general-purpose.

RS1, RS0: 2-Bit Register Bank Address selector.

RS1	RS0	Register Bank	Address
0	0	0	00h-07h
0	1	1	08h-0Fh
1	0	2	10h-17h
1	1	3	18h-1Fh

OV: Overflow Flag

UD: User-definable Flag, General-purpose flag, available for user.

P: Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of “1” bit in the Acc.

T2CON

Address:C8h

bit 7							bit 0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Timer 2 Control Register.

TF2: Timer2 Overflow flag. Cleared by software. TF2 can not be set when RCLK=1or TCLK=1.

EXF2: Timer 2 external flag. Set when either a capture or reload is caused by a negative transition on T2EX, EXEN2=1. When Timer2 interrupt is enabled, EXF2=1 will cause the CPU to vector of Timer2 ISR. EXF2 must be cleared by software.

RCLK: Receive Clock flag. Selects timer 2 overflow pulses (RCLK=1) or timer 1overfiow pulses (RCLK=0) as the baud rate generator for UART modes 1 & 3.

TCLK: Transmit Clock flag. Select Timer2 overflow pulses (TCLK=1) or timer 1 overflow pulses (TCLK=0) as the baud rate generator for serial port modes 1 & 3.

EXEN2:Timer 2 External Enable flag. EXEN2=1: Capture or reload when a negative transition on T2EX unless timer 2 is being used as the baud rate generator for the serial port. Clearing EXEN2 causes timer 2 to ignore events at T2EX.

TR2: Timer 2 Run Control flag. Setting this bit starts the timer.

C/$\overline{T2}$: Timer 2 Counter/Timer Select

C/$\overline{T2}$ = 0 Timer 2 counts the divided-down system clock.

C/$\overline{T2}$ = 1 Timer 2 counts when external pin T2 goes low.

CP/$\overline{RL2}$: Capture/Reload Bit

CP/$\overline{RL2}$ =1: (if EXEN2=1), captures occurred at negative edge of T2EX.

CP/$\overline{RL2}$ =0: (if EXEN2=1), auto-reloads occurred at negative edge of T2EX or when Timer 2 overflowed.

(if RCLK =1 or TCLK = 1).CP/$\overline{RL2}$ is ignored and timer 2 is auto-reloaded when timer 2 overflow,

T2MOD Address:C9h

bit 7							bit 0
–	–	–	–	–	–	T2OE	DCEN

Timer 2 Mode Control Register.

Bit7-Bit2: Reserved

T2OE: Timer 2 Output Enable flag. In the timer 2 clock-out mode, connects the programmable clock output to external pin T2.

DCEN: Down Count Enable flag. Configures timer 2 as an up/down counter.

RCAP2L

Address:CAh

bit 7							bit 0
RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Low byte of Timer2 Capture

RCAP2L stores data to be loaded into or captured from the timer register TL2 for Timer2

RCAP2H

Address:CBh

bit 7							bit 0
RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

High byte of Timer2 Capture

RCAP2H stores data to be loaded into or captured from the TH2 for Timer2

IP

Address:B8h

bit 7							bit 0
—	PS1	PT2	PS	PT1	PX1	PT0	PX0

Interrupt Priority Control Register

IP.7: Reserved bits

PS1: Serial port 1 priority control bit. 1: high priority interrupt

PT2: Timer 2 interrupt priority control bit. 1:

PS0: Serial port0 priority control bit. 1: high priority interrupt

PT1: Timer 1 interrupt priority control bit.

PX1: External interrupt 1 priority control bit. 1: high priority interrupt

PT0: Timer 0 interrupt priority control bit.

PX0: External interrupt 0 priority control bit.1

IE

Address:A8h

bit 7							bit 0
EA	ES1	ET2	ES	ET1	EX1	ET0	EX0

Interrupt Enable Register.

EA: Global Interrupt Enable/Mask. (EA=1/EA=0)
ES1: Serial port 1 Interrupt Enable
ET2: Timer 2 Overflow Interrupt Enable
ES0: Serial port0 Interrupt Enable
ET1: Timer 1 Overflow Interrupt Enable
EX1: External Interrupt 1 Enable
ET0: Timer 0 Overflow Interrupt Enable
EX0: External Interrupt 0 Enable

SBUF Address:99h

bit 7							bit 0
SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Serial Data Buffer. Writing to SBUF loads the transmit buffer to the serial I/O port. Reading SBUF reads the receive buffer of the serial port.

TCON Address:88h

bit 7							bit 0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Timer/Counter Control Register.

TF1: Timer 1 Overflow Flag.

Set by hardware when the Timer 1 overflowed. Cleared by hardware when the interrupt service routine (ISR) is executed.

TR1: Timer 1 Run Control Bit.

Timer 1 is on/off, when TR1 is set/cleared by software.

TF0: Timer 0 Overflow Flag.

Set when Timer 0 overflows. Cleared by hardware when ISR is executed.

TR0: Timer 0 Run Control Bit.

Timer 0 is on/off, when TR0 is set/cleared by software.

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IE1: Interrupt 1 Edge Detect. Set by hardware when interrupted at pin- $\overline{INT1}$. Cleared when ISR is processed for edge-triggered.

IT1: Interrupt 1 Trigger Type Selection Bit.

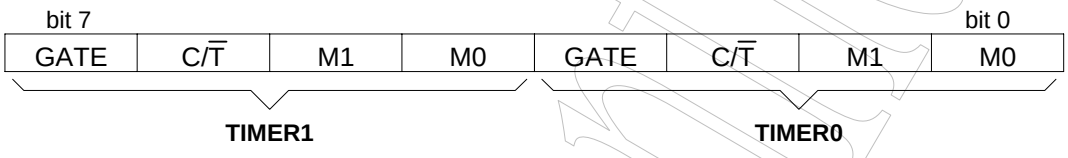
IT1=1: Edge-triggered (hi-to-lo). IT1=0: Level-triggered (active low).

IE0: Interrupt 0 Edge Detect. Set by hardware when interrupted at pin- $\overline{INT0}$. Cleared when ISR is processed for edge-triggered.

IT0: Interrupt 0 Trigger Type Selection Bit.

IT0=1: Edge-triggered (hi-to-lo). IT0=0: Level-triggered (active low).

TMOD Address:89h



Timer/Counter Mode Control Register.

GATE (TMOD.7 or TMOD.3): Timer1/Timer0 toggling gate control

When TRx(in TCON) is set and GATE=1, TIMER/COUNTERx will run only while INTx pin is high(hardware control). When GATE=0, Timer/Counterx will run only while TRx=1(software control).

C/$\overline{T}$: Timer or Counter Selector

C/$\overline{T}$ = 0: Timer operation: TIMERx(input from internal system clock).

C/$\overline{T}$ = 1: Counter operation: COUNTERx counts at falling-edge of Pin-Tx.

M1 (TMOD.5), M0 (TMOD.4) :Mode select of Timer 1

M1	M0	MODE	Operation
0	0	0	1 bit Timer. 8-bit Timer/Counter (THx) with 5-bit pre-scalar (TLx)
0	1	1	16-bit Timer/Counter
1	0	2	8-bit auto-reload Timer/Counter. Reload from THx when overflow.
1	1	3	(Timer 0) TL0 is an 8-bit Timer and is controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 is stopped.

P3: Port 3 of I/O port, P3.2 is modified as an input Address:0B0H

P2: Port 2 of I/O port. Address:0A0H

P1: Port 1 of I/O port, P1.7 is modified for dumping sensor data. Address:090H

P0: Port 0 of I/O port. Address:080H

TH0: High byte of Timer 0. Address:08CH

TL0: Low byte of Timer 0. Address:08AH

TH1: High byte of Timer 1. Address:08DH

TL1: Low byte of Timer 1. Address:08BH

TH2: High byte of Timer 2. Address:0CDH

TL2: Low byte of Timer 2. Address:0CCH

DPH1: High byte of DPTR1. Address:085H

DPL1: Low byte of DPTR1. Address:084H

DPH: High byte of DPTR. Address:083H

DPL: Low byte of DPTR. Address:082H

DPS Address:86H

bit 7							bit 0
—	—	—	—	—	—	—	Dps

Data Point Selection bit. DPS=1: DPTR will be selected. DPS=0: DPTR1 will be selected

SP

Address:81h

bit 7							bit 0
SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Stack Pointer. 8-bit SP memo the address of last address pushed to the stacker. SP is advanced before PUSH exactly executed and can be read or written through software.

PCON

Address:87h

bit 7							bit 0
SMOD1	SMOD0	–	–	GF1	GF0	PD	IDL

Power Control Register.

SMOD1: Double Baud Rate Bit.

1 for Timer 1 in mode 1, 2, or 3 is selected in SCON.

SMOD0: Framing Error Detection Enable.

This bit selects function of the SCON0.7 and SCON1 bits.

0: SCON1.7 control the SM0 function defined for the SCON0 and SCON1

1: SCON1.7 are converted to the FE flag for respective serial port

GF1, GF0: General Purpose Flag

It will be (1, 1) when it came form Idle mode

PD: Set=1 to activates power-down mode. Clear by hardware when interrupted or reset.

IDL: Set=1 to activates Idle mode. Clear by hardware when interrupted or reset.

PDCON

Address: E1H

bit 7							bit 0
PWM2On	PWM1On	WC3	WC2	WC1	WC0	JWP	PDC

Power Down Controller register

PDC: Power down control

0: original (pull-high), 1: SFR value (default)

JWP: Just Wake up

0: Execute Interrupt after wake up (default)

1: Don't execute Interrupt after wake up

WC3, WC2, WC1, WC0: power wake up counter

0, 0, 0, 0: 1-bit counter;	0, 0, 0, 1: 2-bits counter;
0, 0, 1, 0: 3-bits counter;	0, 0, 1, 1: 4-bits counter;
0, 1, 0, 0: 5-bits counter;	0, 1, 0, 1: 6-bits counter;
0, 1, 1, 0: 7-bits counter;	0, 1, 1, 1: 8-bits counter;
1, 0, 0, 0: 9-bits counter;	1, 0, 0, 1: 10-bits counter;
1, 0, 1, 0: 11-bits counter;	1, 0, 1, 1: 12-bits counter;
1, 1, 0, 0: 13-bits counter;	1, 1, 0, 1: 14-bits counter;
1, 1, 1, 0: 15-bits counter;	1, 1, 1, 1: 16-bits counter (default)

PWM2On: Channel 2 ON / OFF (default = 0 / OFF)

PWM1On: Channel 1 ON / OFF (default = 0 / OFF)

WDTCON Address: D8H

bit 7							bit 0
SMOD_1	—	—	—		—	WDTEN	WDTRST

Watch Dog Timer Controller register

SMOD_1: Serial Modification. Doubling the baud-rate of UART1 in modes 1, 2, 3

WDTEN: Watchdog Timer enable, set to “1” to enable watchdog timer

WDTRST: Watchdog Timer reset, set to “1” to reset timer, and be clear when counter reset to 0.

PMR Address: C4H

bit 7							bit 0
UARTOFF	—	—	—	—	ALEOFF	CD1	CD0

Power Manager Register

ALEOFF: 0: ALE toggling is enabled.
1: ALE toggling is disabled

UARTOFF: 0: enable the clock input of UART.
1: disable the clock input of UART

{CD1, CD0}: Output to system clock of Sensor.

(0, 0) => Default

(0, 1) => PAC107's system clk/2

(1, 0) => PAC107's system clk/4

(1, 1) => PAC107's system clk/8

CKCON Address: 8Eh

bit 7							bit 0
WDT1	WDT0	T2M	T1M	T0M	MD2	MD1	MD0

Clock Control register

WDT1, WDT0: WDT time-out counter select

0, 0 - 17 bit counter

0, 1 - 20 bit counter

1, 0 - 23 bit counter

1, 1 - 26 bit counter

T2M: Timer2 clock = sysclk/4(T2M=1) or sysclk/12(T2M=0)

T1M: Timer1 clock = sysclk/4(T2M=1) or sysclk/12(T2M=0)

T0M: Timer0 clock = sysclk/4(T2M=1) or sysclk/12(T2M=0)

MD2, MD1, MD0: Insert Wait-state of MOVX

(0, 0, 0): No Wait-State (0, 0, 1): Original + 4T

(0, 1, 0): Original + 8T (0, 1, 1): Original + 12T

(1, 0, 0): Original + 16T (1, 0, 1): Original + 20T

(1, 1, 0): Original + 24T (1, 1, 1): Original + 28T

SCON1 Address: C0H

bit 7							bit 0
SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1

SCON_1 register

FE_1: Framing Error Bit.

Set by receiver when an invalid stop bit is detected. The FE is not cleared by valid frames but should be clear by software. The "SMOD0" must be set to enable access to the FE bit.

SM0_1: Serial port mode control Set/cleared by software

SM2_1: Set by software to disable reception of frames for which bit8 zero

REN_1: Receiver enable bit. Set/cleared by software.

TB8_1: Set/Cleared by hardware. The state of 9th bit transmitted in 9-bit mode

RB8_1: Set/cleared by hardware to indicate state of ninth data bit received

TI_1: Transmit Interrupt flag.

Set by hardware when byte transmitted. Cleared by software after serving.

RI_1: Received Interrupt flag.

Set by hardware when byte received. Cleared by software after serving.

SM1_1: SM2_1 SELECT

00: Shift reg. I/O expansion

01: 8 bit UART, variable data rate

10: 9 bit UART, fixed data rate

11: 9 bit UART, variable data rate

SCON Address: 98H

bit 7							bit 0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

FE: Framing Error Bit.

Set by receiver when an invalid stop bit is detected.

The FE bit is not cleared by valid frames but should be cleared by software.

The "SMOD0" bit must be set to enable access to the FE.

SM0, SM1: Serial port operation mode specifier.

SM0	SM1	Mode	Description	Baud rate
0	0	0	Shift register.	Fosc/12
0	1	1	8 bit UART,	Variable data rate
1	0	2	9 bit UART,	Fosc/32 or Fosc/64
1	1	3	9 bit UART,	Variable data rate

SM2: Enable the multiprocessor communication feature in mode 2 & 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In mode0, SM2 should be 0.

Mode	SCON	SM2 VARIATION
0 1 2 3	10H 50H 90H D0H	Single Processor Equivalent (SM2=0)
0 1 2 3	10H 50H 90H D0H	Multi Processor Equivalent (SM2=1)

REN: Set/cleared by software to enable/disable reception.

TB8: The 9th bit that will be transmitted in mode 2 & 3. Set/clear by software.

RB8: The 9th bit in mode 2 & 3. In mode 1, if SM2=0, RB8 is the stop bit that was received. In mode0, RB8 is not used.

TI: Transmit Interrupt flag. Set by hardware at the end of 8th bit time in mode0, or at the beginning of the stop bit in other modes. Must be cleared by software.

RI: Receive Interrupt flag. Set by hardware at the end of 8th bit time in mode0, or halfway through the stop bit time in other modes (except see SM2). Must be cleared by software.

Status Address: C5h

bit 7							bit 0
(R1)	HIP	LIP	(R2)	SPTA1	SPRA1	SPTA0	SPRA0

(R1) : Power Fail Priority Interrupt Status

HIP : High Priority Interrupt Status

LIP : Low Priority Interrupt Status

(R2) : Crystal OSC Warm-up Status

SPTA1: Serial Port1 Transmit Activity Monitor

SPRA1: Serial Port1 Receive Activity Monitor

SPTA0: Serial Port0 Transmit Activity Monitor

SPRA0: Serial Port0 Receive Activity Monitor

CdInsWtSt Address: EAh

bit 7							bit 0
—	—			CDW3	CDW2	CDW1	CDW0

Insert Wait-State of Program Code.

{CDW3, CDW2, CDW1, CDW0} = ROM Wait-State

Default ROM Wait-State = 7

3.3 Miscellaneous SFR(Pixart defined)

Hardware windowing registers

Vstart[6:0] – 0E4'H (default : 7'b0000100)

Vend[6:0] – 0E5'H (default : 7'b1111100)

Hstart[7:0] – 0E6'H (default : 8'b00000100)

Hend[7:0] – 0E7'H (default : 8'b10100100)

PWM registers (PWM1 and PWM2)

PWM1conf	- 0DD'H,	Pre-scaling of PWM1 clock, m1
PWM1conf1	- 0F7'H,	Pos-scaling of PWM1 clock, n1
PWM1 Data	- 0DE'H,	High duty width of PWM1, D1
=> Frequency = sysclk / (m1 +1)(n1 +1) => Duty ratio = D1 / n1, (note: D1 must < n1)		

PWM2conf	- 0DC'H,	Pre-scaling of PWM2 clock, m2
PWM2conf1	- 0F6'H,	Pos-scaling of PWM2 clock, n2
PWM2 Data	- 0DF'H,	High duty width of PWM2, D2
=> Frequency = sysclk / (m2 +1)(n2 +1) => Duty ratio = D2 / n2, (note: D2 must < n2)		

PixSt (default:8'b01000011) Address:EEH

bit 7							bit 0
iRAM_EnH	dis_exint	clr_exint	clr_inint	Mode1	Mode0	skip1	skip0

iRAM_EnH: When 1, MOVX will access internal 1KB SRAM

dis_exint: When 1, disable external interrupt

clr_exint: When 1, clear external interrupts, then have to clear to 0

clr_inint: When 1, clear internal interrupts, then have to clear to 0

{Mode1, Mode0}:

{0, 0} = Normal capture mode.

{0, 1} = Compressed capture mode (DPCM).

{1, 0} = Full window display on LCM mode (through P0).

{1, 1} = Hardware windowing display on LCM mode (through P0).

{skip1, skip0}:

{0, 0} = No skip pixel when display on LCM

{0, 1} = Skip 1 pixel when display on LCM

{1, 0} = Skip 2 pixel when display on LCM

{1, 1} = Skip 4 pixel when display on LCM

Cap (default: 8'b00000000) Address: EFH

bit 7							bit 0
-	-	-	Capture	Cap_no3	Cap_no2	Cap_no1	Cap_no0

Capture: when 1, capture {Cap_no3 : Cap_no0} image through ASIC.

I2C: Sensor command register Address: EDH

bit 7							bit 0
intp_pd	lcdwrb	SDAo	int4lcd	int4cap	CSB	SCL	SDAi

intp_pd: When 1, disable interrupt block, 0 enable interrupt block.

lcdwrb: Control output pin LCD_WRB.

SDAo: I2C data output of sensor.

int4lcd: During LCD mode, each frame will generate interrupt called int4lcd.

int4cap: When set Capture at Cap register and ASIC finish its capture job. ASIC will generate interrupt called int4cap.

CSB: When 1, disable sensor, 0 enable sensor

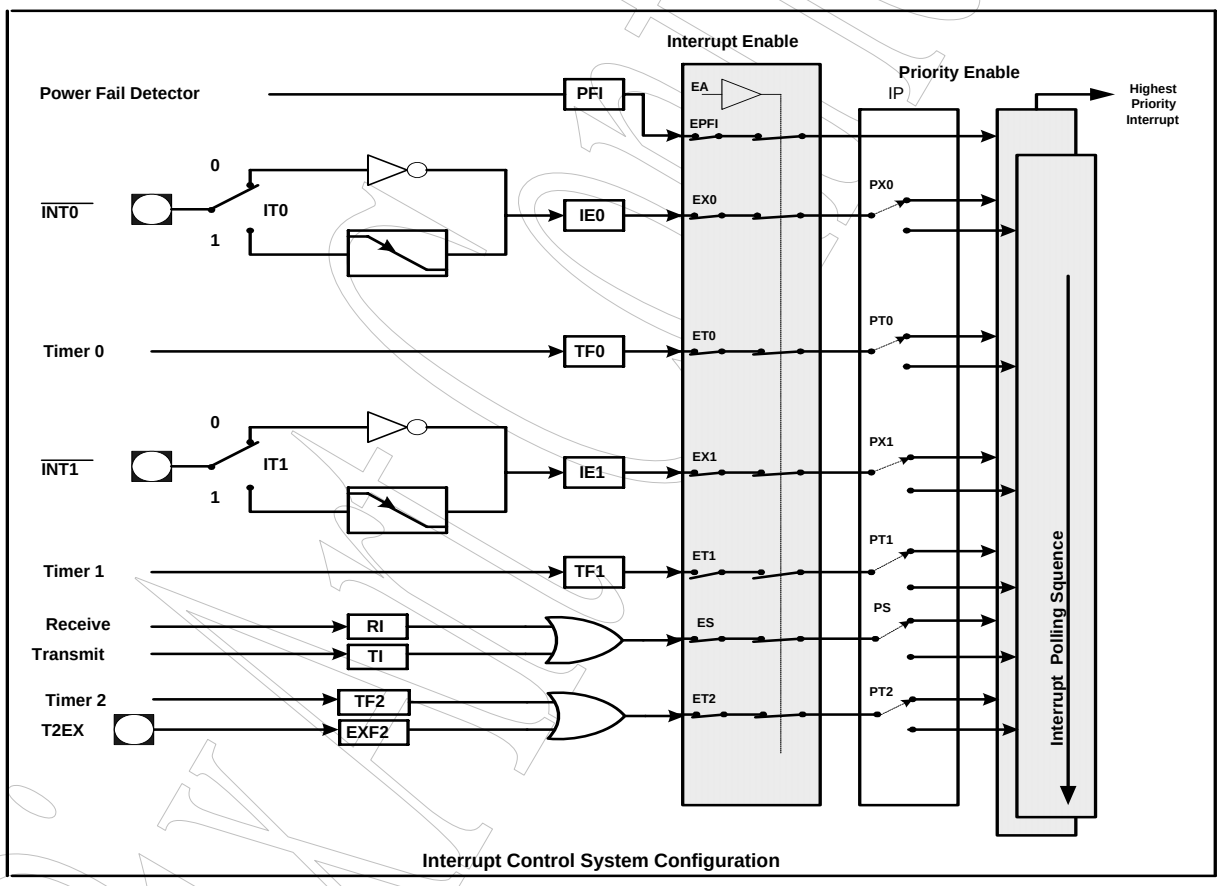
SCL: I2C clock of sensor.

SDAi: I2C data in of sensor.

4. ON-CHIP PERIPHERALS

4.1 Interrupts

Interrupt Source	Request Flag		Priority Flag	Enable Flag	Vector Address	Priority-Within-Level	Flog Cleared by Hardware?
External Request	IE0/TCON.1		PX0/IP.0	EX0/IE.0	0003h	1	Edge-Yes Level-No
Internal Timer0/Counter0	TF0/TCON.5		PT0/IP.1	ET0/IE.1	000Bh	2	Yes
External Request	IE1/TCON.3		PX1/IP.2	EX1/IE.2	0013h	3	Edge-Yes Level-No
Internal Timer1/Counter1	TF1/TCON.7		PT1/IP.3	ET1/IE.3	001Bh	4	Yes
Internal Serial Port	Xmit	Ti/SCON.1	PS/IP.4	ES/IE.4	0023h	5	No
	Rcvr	RI/SCON.0					
Internal Timer2/Counter2	TF2/T2CON.7		PT2/IP.5	ET2/IE.5	002Bh	6	No
	EXF2/TSCON.6						



Interrupt Control System Configuration

Interrupt System Table

External Interrupt

External Interrupt $\overline{\text{INT0}}$ is modified as a Sensor control pin. The $\overline{\text{INT1}}$ pins can be

programmed to be level-triggered or edge triggered. IT1 = 0, $\overline{INT1}$ is triggered by detected low at the pin. If IT1 = 1, $\overline{INT1}$ is negative-edge triggered. External interrupts are enabled with bits EX1in the IE register. Evens on the external interrupt pins set the interrupt flags IE1 in TCON. These request bits are cleared by hardware vectors to service routines only if the interrupt is negative-edge triggered. If the interrupt is level-triggered, the interrupt service routine must clear the request bit. External hardware must release $\overline{INT1}$ before the service routine completes, or an additional interrupt is requested.

External interrupt pins are sampled once when rising edge of oscillator clock. The interrupt pin should hold for at least 3 clocks for level-detection. And hold one clock for edge-triggered interrupt. EX1 is set if external interrupt is detected. And the EX1 is automatically cleared during service routine fetch cycles for edge-triggered interrupts.

Timer Interrupts

Three interrupt request TF0, TF1 and TF2 are set by timer 0 ,timer 1 and timer 2 overflow. TF0 and TF1 are cleared by hardware vectors and jump to interrupt service routine when timer 0 and timer 1 interrupts are generated. TF2 is different to TF0/TF1. TF2 is clear by software when timer 2 interrupt is generated.

The relative enable bit of Timre0, Timer1, Timer2 are ET0, ET1, and ET2 in register IE.

Timer 2 interrupts are generated by a logical OR of bits TF2 and EXF2 in register T2CON. Neither flag is cleared by a hardware vector to a service routine. In fact, the interrupt service routine must determine if TF2 or EXEF2 generated the interrupt, and then clear the bit. Timer 2 interrupt is enabled by ET2 in register IE.

Serial Port Interrupt

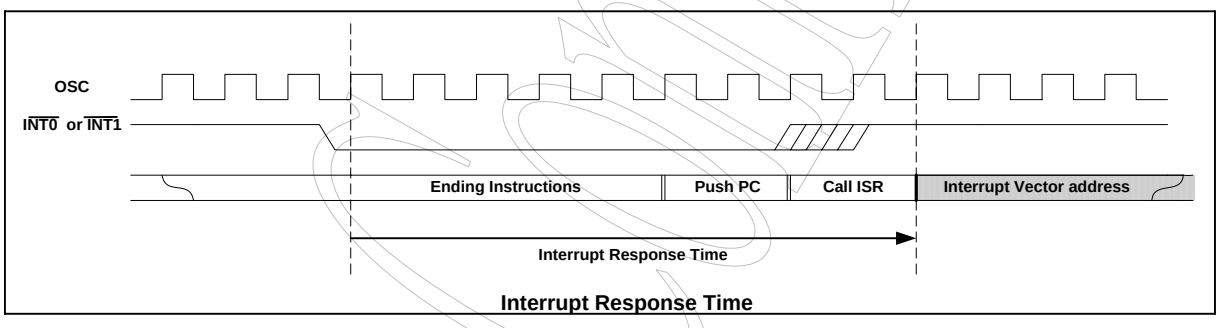
Serial port interrupts are generated by the logical OR of bits RI and TI in the SCON register. Neither flag is cleared by a hardware vector to the service routine. The service routine resolves RI and TI interrupt generation and clears the serial port request flag. The serial port interrupt is enabled by bit ES in the IE register. In the same way by using serial port 1. Serial port 1 control register is SCON1, and the buffer is SBUF1. Here is one thing to be noticed that serial port 1 only uses timer 1 to generate baud rate.

Interrupt Priority

PAC107 has 2 level priorities. Setting / clearing a bit in the Interrupt Priority register (IP) or Extent Interrupt Priority register (EIP) established its associated interrupt request as a high / low priority. If a low-priority level interrupt is being serviced, a high-priority level interrupt will interrupt it. However, an interrupt source cannot interrupt a service program of the same or higher level. The interrupt priority is shown on Interrupt Control System Configuration.

Interrupt Response Time

The minimum interrupt response time is eight clocks that when an interrupt request asserts as last instruction executed. The maximum interrupt response time is 24 clocks. DJNZ direct, rel or others instruction sets which operation period is 16 clocks, is decoded ok. When a high priority interrupt asserts during a low priority interrupt service program, the minimum and maximum interrupt response times are 8 clocks and 24 clocks.



Interrupt Response Time

4.2 TIMER/COUNTERS

Timer 0

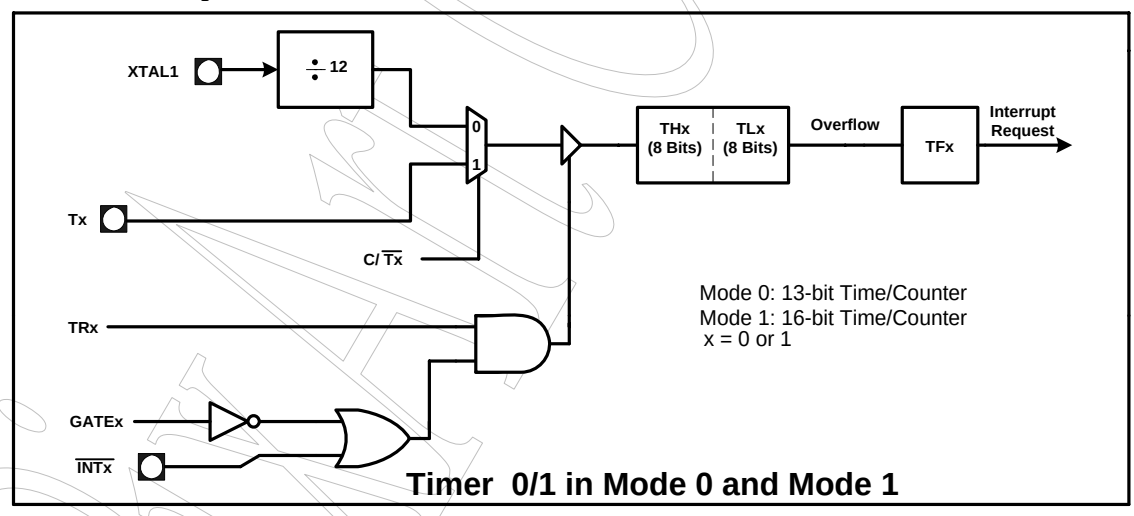
Timer 0 can be a timer or event counter in four modes of operation. It's controlled by the high-nibble of the TMOD register and bits 5, 4, 1, and 0 of the TCON register. The TMOD register selects the method of timer gating (GATE), timer or counter operation (C/$\overline{T}$), and mode of operation (M1, M0). The TCON register provides timer 0 control functions: overflag (TF0), run control (TR0), interrupt flag (IE0), and interrupt type control (IT0). For normal timer operation (GATE = 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE and TR0 allows $\overline{INT0}$ to control timer operation.

Timer0/Mode 0 (13-bit Timer)

Mode 0 configures timer 0 as a 13-bit timer which is set up as an 8-bit timer (TH0 register) with a modulo 32 pre-scalar implemented with the lower five bits of the TL0 register. The upper three bits of TL0 register are indeterminate and should be ignored. Pre-scalar overflow increments the TH0 register.

Timer 0/ Mode 1 (16-bit Timer)

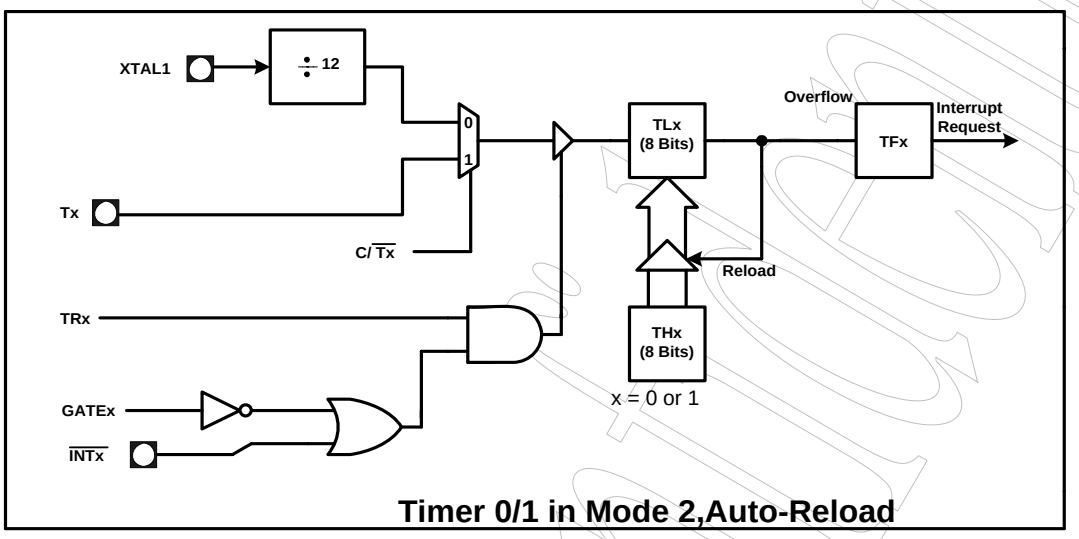
Mode 1 configures timer 0 as a 16-bit timer with TH0 and TL0 connected in cascade. The selected input increments TL0.



Timer 0/1 in Mode 0 and Mode 1

Timer 0/ Mode 2 (8-bit Timer With Auto-reload)

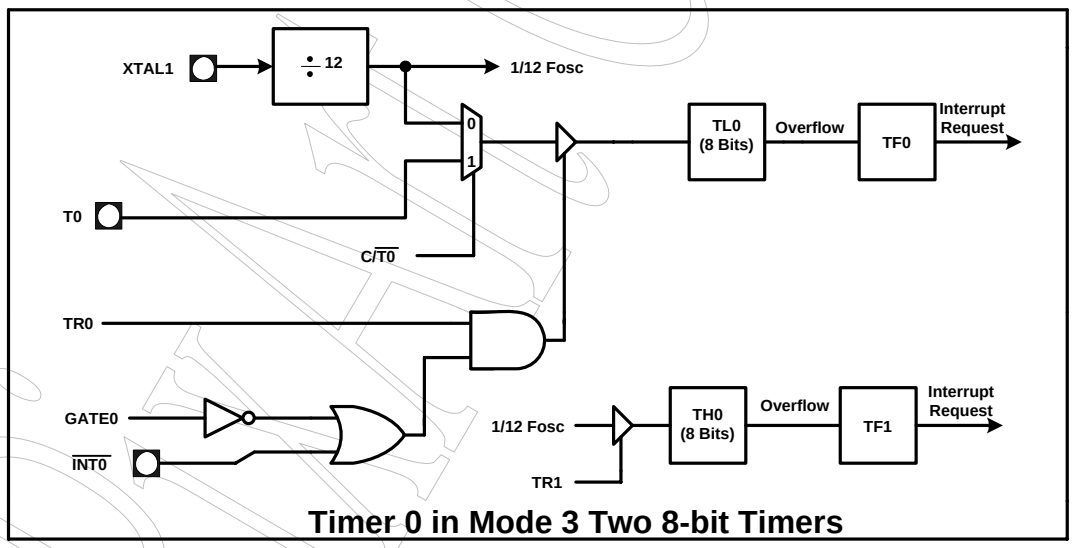
Mode 2 configures timer 0 as an 8-bit timer (TL0 register) that automatically reloads from the TH0 register. TL0 overflow sets the timer overflow flag (TF0) in the TCON register and reloads TL0 with the contents of TH0, which is preset by software. When the interrupt request is serviced, hardware clears TF0. The reload leaves TH0 unchanged.



Timer 0/1 in Mode 2,Auto-Reload

Timer 0/ Mode 3(Two 8-bit Timers)

Mode 3: TL0 and TH0 operate as 8-bit timers independently. Counter TL0 is configured by uses Timer's C/$\overline{T}$ and GATE in TMOD, and TR0 in TCON. TH0 worked as a timer (free running at frequency= Fosc/12) and takes over by timer 1 interrupt (TF1) and run control bits(TR1). Thus, operation of timer 1 is restricted when timer 0 is in mode 3.



Timer 0 in Mode 3 Two 8-bit Timers

Timer 1

Timer 1 can be a timer or event counter in three modes of operation. The configuration for

modes 0,1 and 2 are same as Timer 0. Timer 1's mode 3 is a hold-count mode.

Timer 1 is controlled by high-nibble of the TMOD register and bits 7,6,3,and 2 of the TCON register. TMOD selects the method of timer gating (GATE), timer or counter operation ($C/\overline{T}$), and mode of operation (M1 and M0). TCON set timer 1 control functions: overflow flag (TF1),run control (TR1),interrupt flag(IE1), and interrupt type control (IT1). For normal timer operation (GATE = 0), setting TR1 allows timer register TL1 to be incremented by the selected input. Setting GATE and TR1 allows external pin $\overline{INT1}$ to control timer operation. This setup can be used to make pulse width measurements.

Timer 1/ Mode 0 (13-bit Timer)

Mode 0 configures timer 0 as a 13-bit timer, which is set up as an 8-bit timer (TH1 register) with a modulo-32 prescalar implemented with the lower 5 bits of the TL1 register. The upper 3 bits of the TL1 register are ignored. Prescalar overflow increment the TH1 register.

Timer1/ Mode 1 (16-bit Timer)

Mode 1 configures timer 1 as a16-bit timer with TH1 and TL1 connected in cascade. The selected input increments TL1.

Timer 1/ Mode 2 (8-bit Timer)

Mode 2 configures timer 1 as an 8-bit timer (TL1 register) with automatic reload from the TH1 register on overflow. Overflow from TL1 sets overflow flag TF1 in the TCON register and reloads TL1 with the contents of TH1, which is preset by software. The reload leaves TH1 unchanged.

Timer 1/ Mode3 (Halt)

Placing timer in mode 3 causes it to halt and its count. This can be used to halt timer 1 when the TR1 run control bit is not available, i.e., when timer 0 is in mode 3.

Timer 2

Timer 2 is a 16-bit timer/count constructed by {TH2, TL2}. The mode control T2MOD and the configure T2CON control the operation of timer 2.

Operating modes:

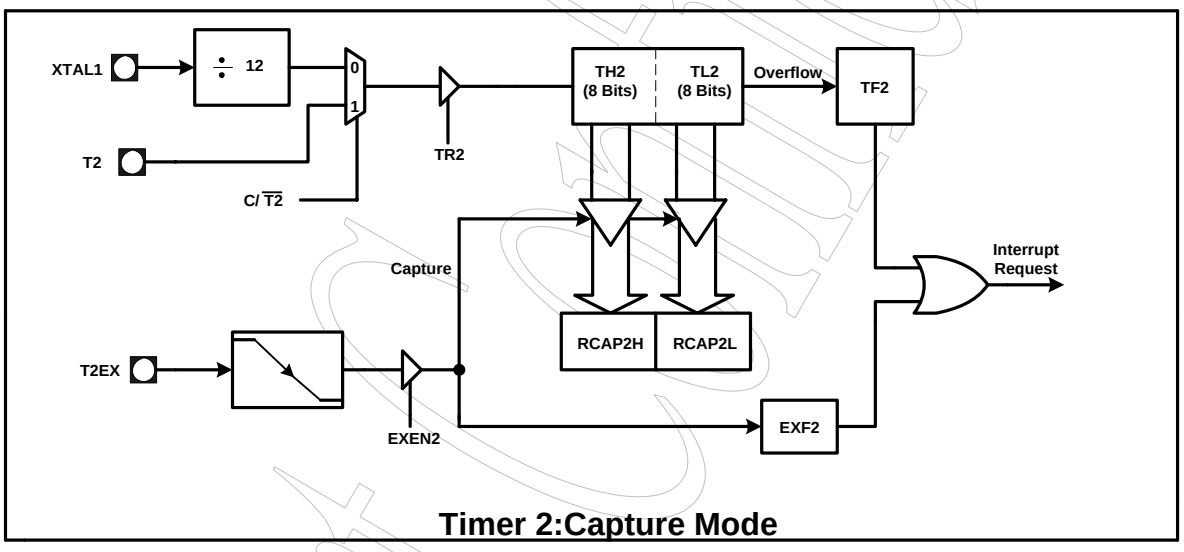
capture mode,
auto-reload mode, (default)
baud rate generator mode,
programmable clock-out mode.

RCLK and/or TCLK selects the baud rate generator mode.

Timer 2 is similar to timer 0 and timer 1. C/$\overline{T2}$ selects Fosc/12 (timer operation) or external pin T2 (counter operation) as the timer register input. Setting TF2 to be advanced by the selected input.

Timer 2/ Capture Mode

Timer 2 function as a 16-bit timer or counter. An overflow condition sets bit TF2 to execute ISR. Set the external enable bit EXEN2 allows the RCAP2Hand RCAP2L registers to report the current value in timer registers TH2 and TL2 in response to a hi-to-lo transition at external input T2EX. The transition at T2EX also sets bit EXF2 on T2CON. The EXF2 bit, like TF2, can generate an interrupt. TR2 must be enabled in this mode.



Timer 2:Capture Mode

Timer 2/ Auto-reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. The timer operates an as an up counter or as an up/down counter, as determined by the down counter enable bit (DCEN). At device reset, DCEN is cleared, so in the auto-reload mode, timer 2 defaults to operation as an up counter. TR2 must be enabled when running this mode.

Up Counter Operation

When DCEN = 0, timer 2 operates as an up counter. If EXEN = 0, timer 2 counts up to FFFFH and sets the TF2 overflow flag. The overflow condition loads the 16-bit value in the

reload/capture registers (RCAP2H, RCAP2L) into the timer registers (TH2, TL2). The values in RCAP2H and RCAP2L are preset by software.

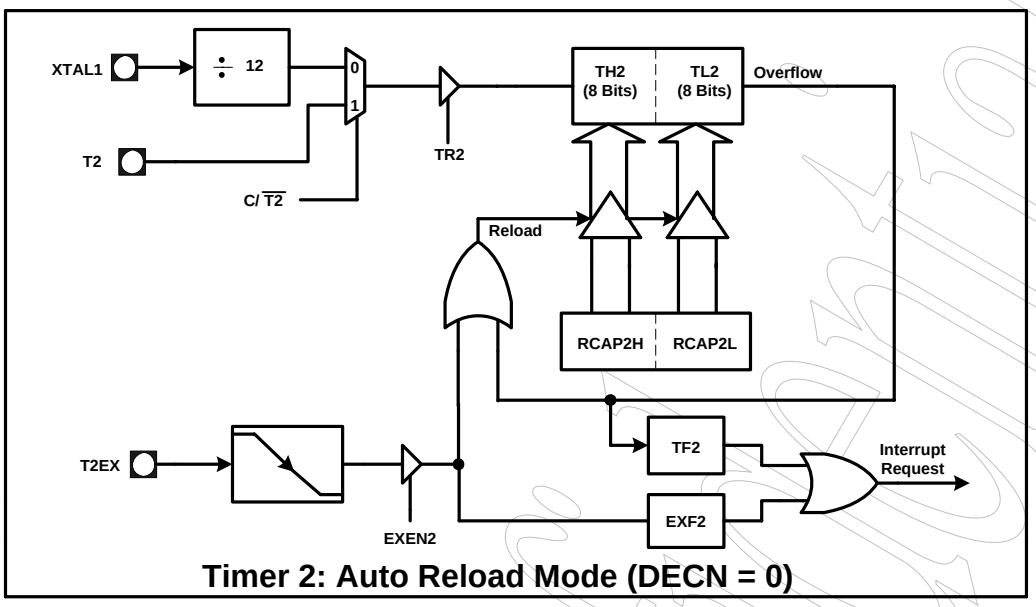
If EXEN2 = 1, the timer registers are reloaded by either a timer overflow or a high-to-low transition at external input T2EX. This transition also sets the EXF2 bit in the T2CON register. Either TF2 or EXF2 bit can generate a timer 2 interrupt request. TR2 must be enabled when running this mode.

Up/Down Counter Operation

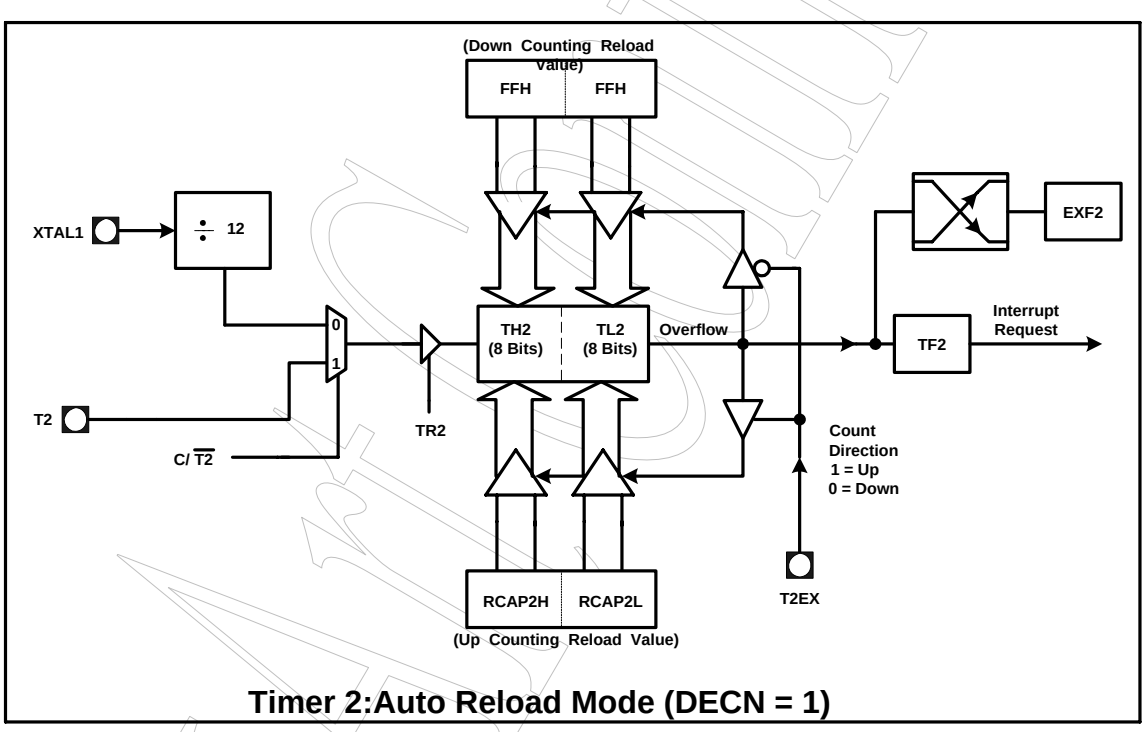
When DCEN = 1, timer 2 operates as an up/down counter. External pin T2EX controls the direction of the count. When T2EX is high, timer 2 counts up. The timer overflow occurs at FFFFH which sets the timer 2 overflow flag (TF2) and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers (TH2, TL2) equals the value stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and reloads FFFFH into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows changing the direction of the count. When timer 2 operates as an up/down counter, EXF2 does not generate an interrupt. This bit can be used to provide 17-bit resolution. TR2 must be enabled when running this mode.



Timer 2: Auto Reload Mode (DECN = 0)



Timer 2:Auto Reload Mode (DECN = 1)

Timer 2/ Baud Rate Generator Mode

This mode configures timer 2 as a baud rate generator for use with the serial port. Select this mode by setting the RCLK and/ or TCLK bits in T2CON.

Timer 2/ Clock-out Mode

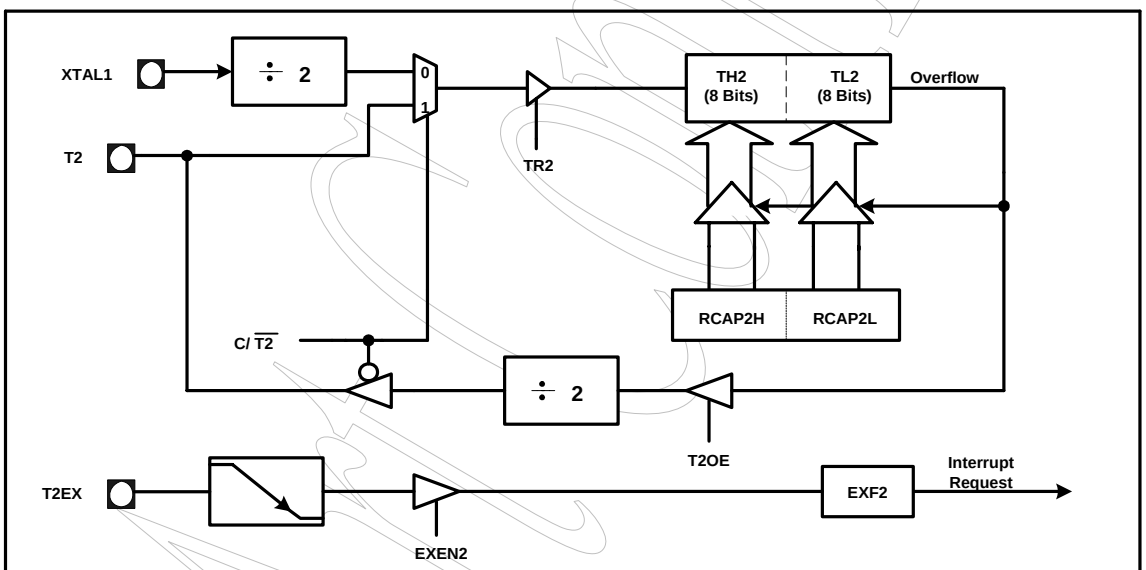
In the clock-out mode, timer 2 functions as a 50%-duty-cycle, variable-frequency clock.

The input clock advances TL0 at frequency of Fosc/2. The timer repeatedly counts to overflow from a preloaded value. At overflow, the contents of the RCAP2H and RCAP2L registers are loaded into TH2/TL2. In this mode, timer 2 overflows do not generates interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

$$\text{Clock-out Frequency} = \frac{\text{Fosc}}{4\text{X}(65536 - \text{RCAP2H, RCAP2L})}$$

Timer 2 Modes of Operation

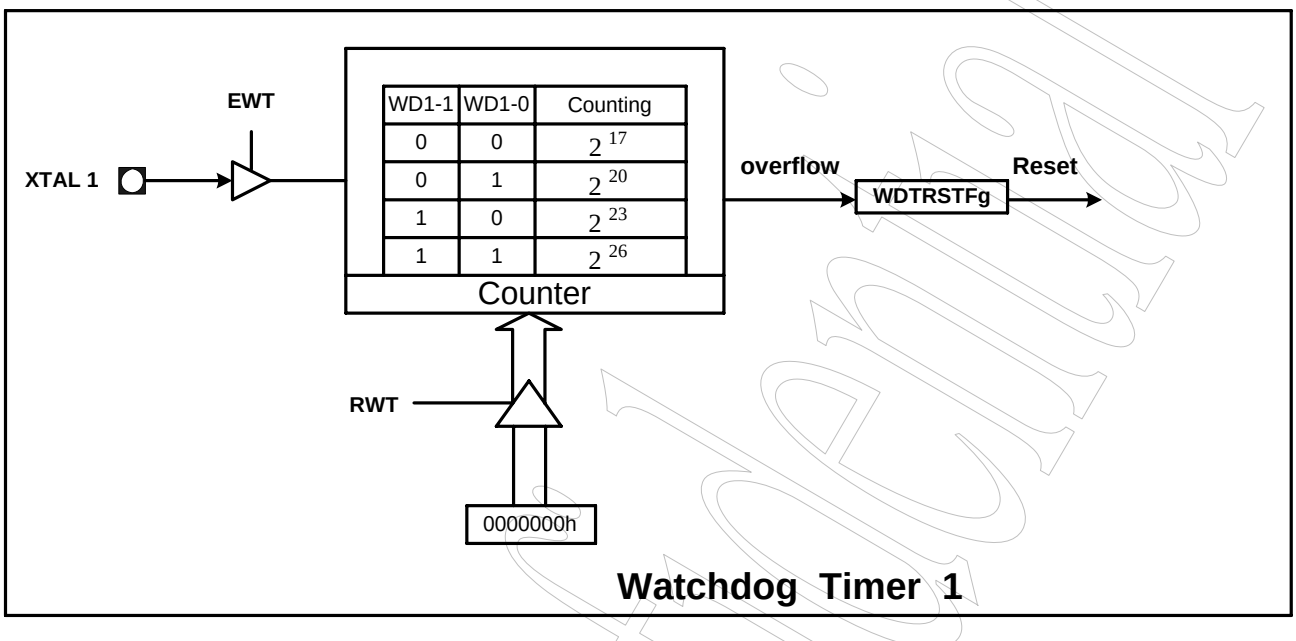
Mode	RCLK OR TCLK (in T2COON)	CP/RL2# (in T2MOD)	T2OE (in T2MOD)
Auto-reload Mode	0	0	0
Capture Mode	0	1	0
Baud Rate Generator Mode	1	X	X
Programmable Clock-Out	X	0	1



Timer 2: Clock Out Mode

Watchdog Timer

The watchdog timer has system reset functions. By setting WD1-1, WD1-0 (CKCON, 8Eh) to choose 2^{17}, 2^{20}, 2^{23} or 2^{26} counter for Watchdog Timer. As the Watchdog Timer overflow, sets WDTRSTFg (in register WDCON, D8h) and finally resets the MCU. If MCU is reset by watchdog Timer , WDTRSTFg remains one and POR (in register WDCON, D8h) is zero. On the other hand, if RISC 52 has been power-on reset, WDTRSTFg is zero and POR one.

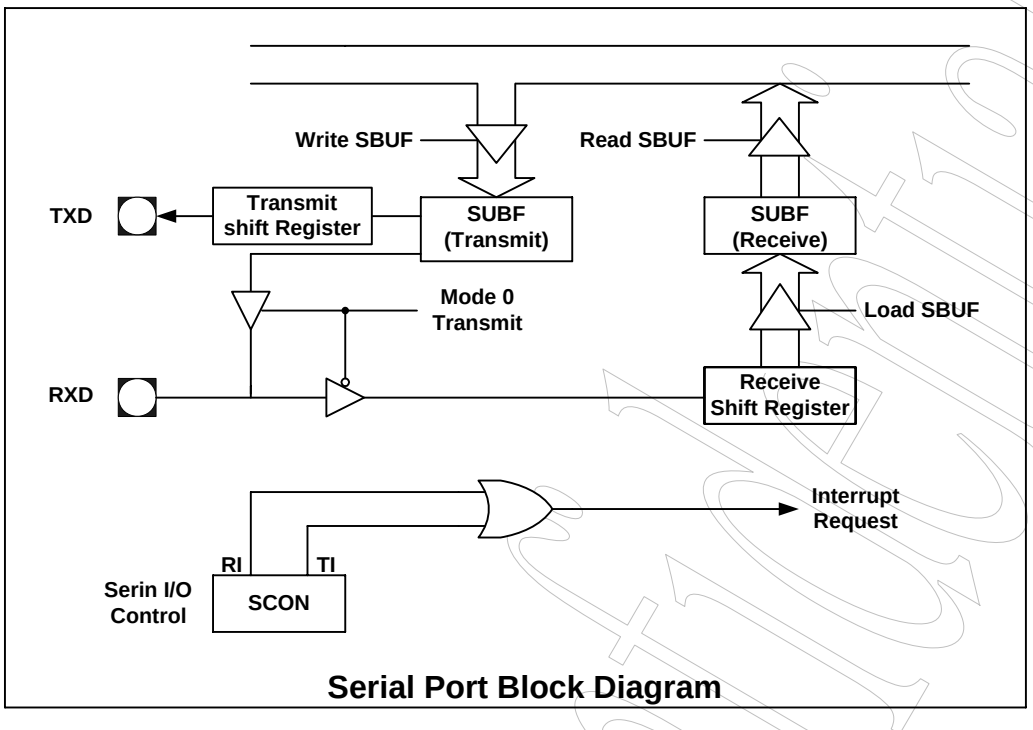


4.3 SERIAL I/O PORT

Both synchronous and asynchronous communication modes are provided in the serial I/O port. It operates as UART in three full-duplex modes (modes 1, 2, and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates. The serial port also operates in a single synchronous mode (mode 0).

Mode 0 – Synchronous mode: operates at a single baud rate.
Mode 1 - operate over a wide range of baud rate generated by timer 1 and timer 2.
Mode 2 - operates at two baud rates.
Mode 3 - operate over a wide range of baud rates generated by timer 1 and timer 2.

Asynchronous modes, Pin-TXD: transmits. Pin-RXD: receives.
Synchronous mode (mode 0), Pin-TXD: clock output. Pin-RXD: sends and receives data.
SBUF holds received data byte and data to be transmitted, actually consists of two buffers. The receive shift register allows reception of a second byte before the byte be read from SBUF. And the 1st byte will be override by 2nd byte if software doesn't read it. the UART sets interrupt bits TI and RI for transmission and reception, respectively. Both of these two bits share a same interrupt vector.



Serial Port Block Diagram

Serial Port Signals

Function Name	Type	Description	Multiplexed With
TXD	O	**Transmit Data.** In mode 0, TXD transmits the clock signal. In modes 1, 2,and 3,TXD transmits serial data.	P3.1
RXD	I/O	**Receive Data.** In mode 0, RXD transmits and receives serial data. In mode 1, 2,and 3, RXD receives serial data.	P3.0

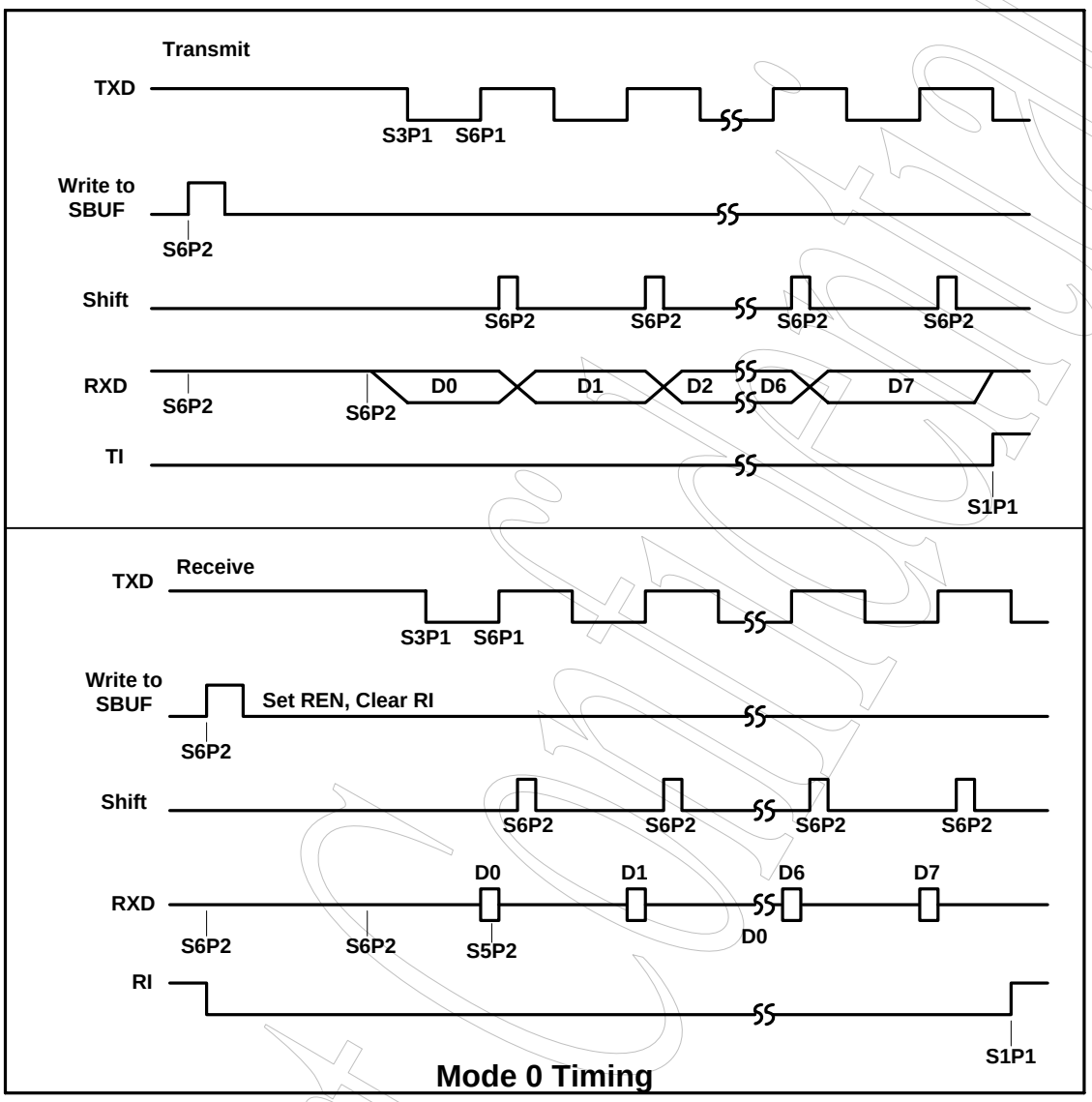
Synchronous Mode (Mode 0)

Mode 0 is a half-duplex, synchronous mode, which is commonly used to expand I/O capabilities of device with shift registers. The transmit data (TXD) pin outputs a set of eight clock pulses which the receive data (RXD) pin transmits or receives a byte of data. The transmission and reception are all least-significant bit (LSB) first. Shifts occurred in the last phase (S6P2) of every peripheral cycle. Baud rate = Fosc/12.

Transmission (Mode 0)

Follow these steps to begin a transmission:

1. Write to the SCON register, clearing bits SM0,SM1, and REN.
2. Write 8-bit data to be transmitted to SBUF.



Mode 0 Timing

At S6P2 of the following cycle, hardware shifts the LSB (D0) onto the RXD pin. At S3P1 of the next cycle, the TXD pin goes low for the first clock-signal pulse. Shifts continue every peripheral cycle. In the 9th cycle after the write to SBUF, the MSB (D7) is on the RXD pin. At the beginning of the tenth cycle, hardware drives the RXD pin high and assert TI (S1P1) to indicate an end of transmission.

Reception (Mode 0)

To start a reception in mode 0, write to the SCON register. Clear SM0, SM1, and RI and set REN. Hardware executes the write to SCON in the last phase (S6P2) of a peripheral cycle. Write to SCON in the second peripheral cycle, TXD goes low at S3P1 for the first clock, and the LSB (D0) is sampled on RXD pin at S5P2. D0 bit is then shifted into the shift

register. As eight shifts at S6P2 of every peripheral cycle, the LSB (D7) is done, then hardware asserts RI (S1P1) to indicate reception completed. Software can read the received byte from SBUF.

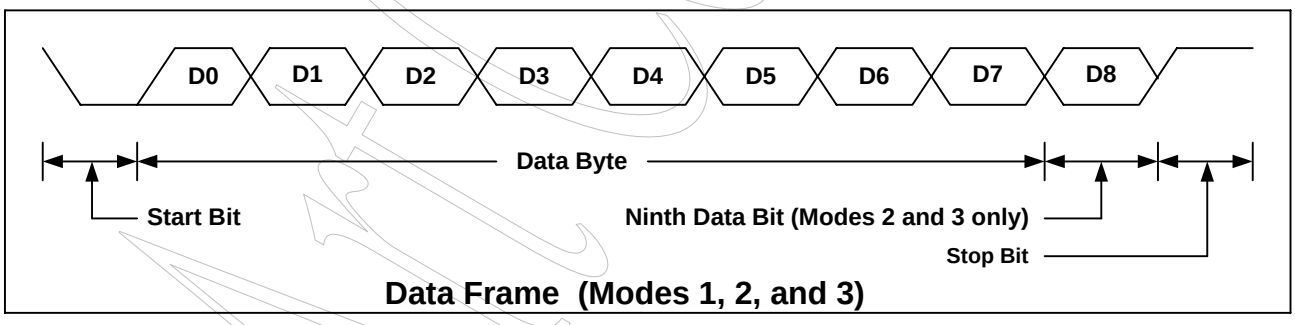
Asynchronous Modes (Modes 1, 2, and 3)

Mode 1

Mode 1 is a full-duplex, asynchronous mode. The data frame consists of 10 bits. They are one start bit, 8 data bits, and one stop bit. Serial data is transmitted via TXD pin and received through RXD pin. When a data frame is received, the stop bit is read from RB8 bit in SCON. The baud rate is generated by overflow of Timer 1 or Timer 2.

Mode 2 and Mode 3

Modes 2 and 3 are full-duplex, asynchronous modes. There are 11 bits per transfer frame. They are one start bit, 8 data bits (LSB first), one programmable 9th data bit, and one stop bit is read from the RB8 bit in the SCON register. When transmit, the 9th data bit is written to TB8 bit in SCON. The 9th data bit can be used as a command/data flag.
- In mode 2, the baud rate is programmable to 1/32 or 1/64 of the oscillator frequency.
- In mode 3, the baud rate is generated by overflow of timer 1 or timer 2.



Data Frame (Modes 1, 2, and 3)

Transmission (Modes 1, 2, 3)

Follow these steps to initiate a transmission:
1. Write to the SCON register. Select the mode with the SM0 and SM1 bits, and clear the REN bit. For modes 2 and 3, also write the ninth bit to the TB8 bit.
2. Write the byte to be transmitted to the SBUF register. This write stars the transmission.

Reception (Modes 1, 2, 3)

To prepare for a reception, set the REN bit in the SCON register. The actual reception is

then initiated by a detected high-to-low transition on the RXD pin.

Baud Rates

Baud Rate for Mode 0: The baud rate for mode 0 id fixed at Fosc/12.

Baud Rtes for Mode 2

Mode 2 has two baud rates, which are selected by the SMOD bit in the PCON register. The following expression defines the baud rate:

$$\text{Sreial I/O Mode 2 Baud Rate} = 2^{SMOD} \times \frac{Fosc}{64}$$

Baud Rates for Modes 1 and 3

In modes 1 and 3, the baud rate is generated by overflow of timer (default) and/or timer 2. You may select either or both timer(s) to generate the baud rate(s) for the transmitter and/or the receiver.

Timer 1 Generated Baud Rates (Mode 1 and 3)

Timer 1 is the default baud rate generator for the transmitter and the receiver in modes 1 and 3. The baud rate is determined by the timer 1 overflow rate and the value of SMOD, as shown in the following formula:

$$\text{Sreial I/O Mode 1 and 3 Baud Rate} = 2^{SMOD} \times \frac{\text{Timer 1 Onerflow Rate}}{32}$$

Selecting Timer 1 as the Baud Rate Generator

To select timer 1 as the baud rate generator:

- Disable the timer interrupt by clearing the IE0 register.
- Configure timer 1 as a timer or an event counter (set or clear the C/T bit in the TMOD register).
- Select timer mode 0-3 by programming the M1, M0 bits in the TMOD register.

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$$\text{Sreial I/O Mode 1 and 3 Baud Rate} = 2^{SMOD} \times \frac{Fosc}{32 \times 12 \times [256 - (Th1)]}$$

In most applications, timer 1 is configured as a timer in auto-reload mode (high nibble of TMOD = 0010B). The resulting baud rate is defined by the following expression:

Timer 1 can generate very low baud rates with the following setup:

- Enable the timer 1 interrupt by setting the ET1 bit in the IE register.
- Configure timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B).
- Use the timer 1 interrupt to initiate a 16-bit software reload.

Timer 2 Generated Baud Rates (Modes 1 and 3)

Timer 2 may be selected as the baud rate generator for the transmitter and/or receiver. The timer 2 baud rate generator mode is similar to the auto-reload mode. A rollover in the TH2 register reloads registers TH2 and TL2 with the 16-bit value on registers RCAP2H and RCAP2L, which are preset by software.

The timer 2 baud rate is expressed by the following formula:

$$\text{Sreial I/O Mode 1 and 3 Baud Rate} = \frac{\text{Timer 2 Onerflow Rate}}{16}$$

Selecting Timer 2 as the Baud Rate Generator

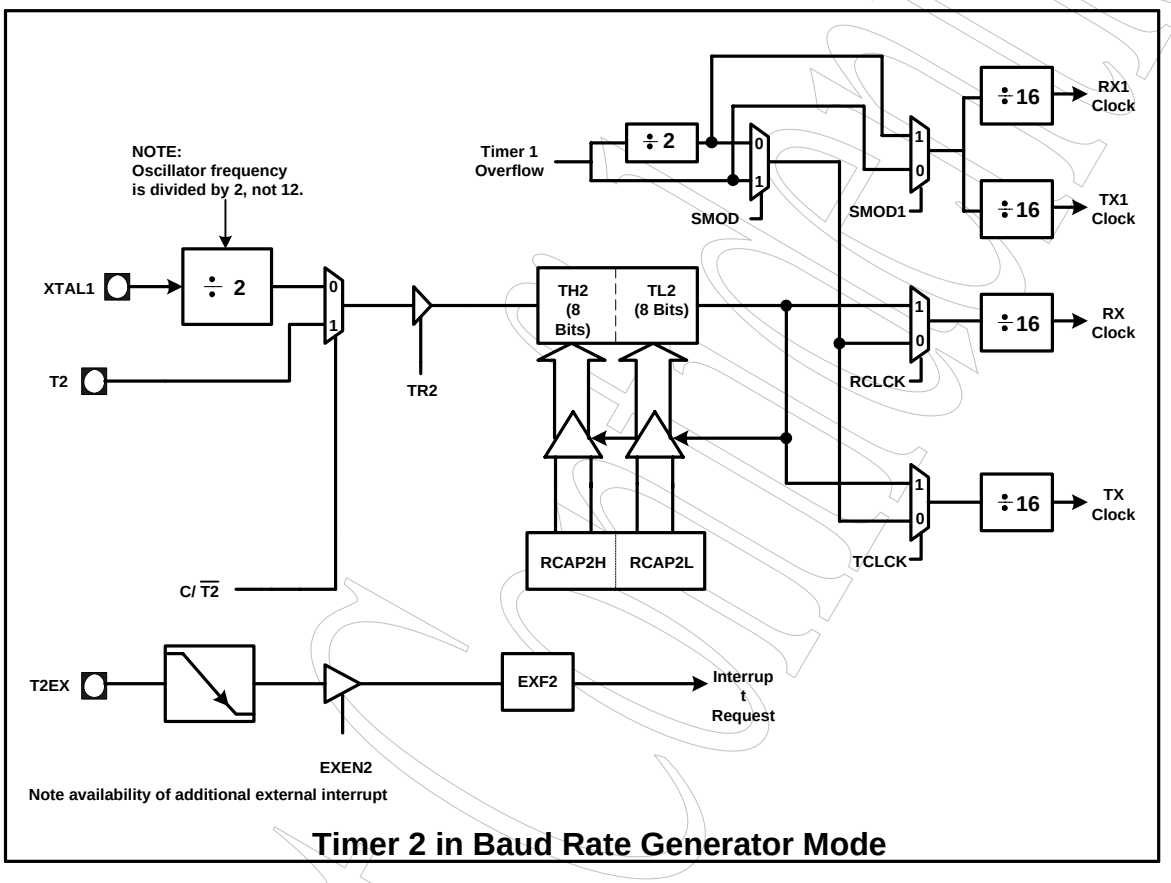
Program the RCLCK and TCLCK bits in the T2CON. A rollover in the TH2 register does not set the TF2 bit in the T2CON register. And a high-to-low transition at T2EX pin sets the EXF2 bit in the T2CON register but does not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). TT2EX pin cab be used as an additional external interrupt by setting the EXEN2 bit in T2CON.

NOTE : Please turn off the timer before accessing registers TH2, TL2, RCAP2H, and RCAP2L(clear the TR2 bit in the T2CON register).

You may configure timer 2 as a timer or a counter. In most applications, it is configured for timer operation (i.e., the C/T2 bit is clear in the T2CON register).

Selecting the Baud Rate Generator(s)

RCLK Bit	TCLCK Bit	Receiver Baud Rate Generator	Transmitter Baud Rate generator
0	0	Timer 1	Timer 1
0	1	Timer 1	Timer 2
1	0	Timer 2	Timer 1
1	1	Timer 2	Timer 2



Timer 2 in Baud Rate Generator Mode

Note: Timer 2 advanced for every state time (2Tosc) when it is in the baud rate generator mode. In the baud rate formula that follows, “RCAP2H,RCAP2L” denotes the contents of RCAP2H and RCAP2L taken as a 16-bit unsigned integer:

$$\text{Sreial I/O Mode 1 and 3 Baud Rate} = \frac{\text{Fosc}}{32 \times [65536 - (\text{RCAP2H,RACAP2L})]}$$

NOTE : When timer 2 is configured as a timer and is in baud rate generator mode, do not read or write the TH2 or TL2 registers. The timer is being incremented every state time, and the result of a read or write may not be accurate. In addition, you may read, but not write to, the RCAP2 registers; a write may overlap a reload and cause write and/or reload errors.

Serial I/O Port 1

Serial I/O port 1 is the same as serial I/O port mentioned above. RXD1 is at P1.2 and TXD1 at P1.3. The Serial I/O port 1 has its own buffer (SBUF1, C1h) and control register (SCON1, C0h). All functions and structures are the same as serial I/O port. But the only difference is that serial I/O port 1 only uses timer 1 for baud rate at mode 1 and mode 3. The double baud rate bit SMODE1 is at WDCON (D8h) register.

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5. Electrical Specifications

DC Electrical Characteristics (VDD=3.0V±20%, Ta=10°C~40°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type :PWR					
VDD	Analog and digital operating voltage	2.4	3.0	3.6	V
ICC1f	Operation Current of full function, full speed		30		mA
ICC1m	Operation Current of full function, 14.3181Mhz		14		mA
ICC2f	Operation Current of MCU, Sensor shut down		24	30	mA
ICC2m	Operation Current of MCU, Sensor shut down		8	14	mA
ICC3	Power down MCU, Sensor alive	2.5	6	8	mA
Type :IN & I/O Reset and SYSCLK					
VIH	Input voltage HIGH	2.0		VDD	V
VIL	Input voltage LOW	0		0.8	V
Cin	Input capacitor			10	pF
Ilkg	Input leakage current		TBD		uA

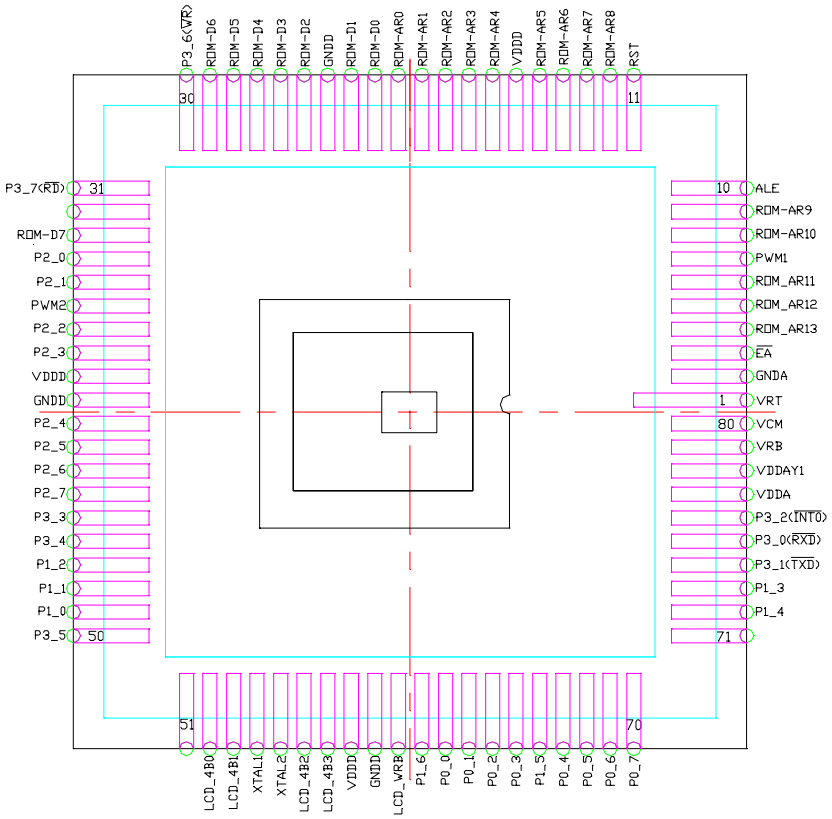
AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
SYSCLK	System clock frequency		14.3181	40	MHz
SENCLK	Sensor clock frequency	4			MHz
PXCLK	Pixel clock output frequency			1.5	MHz

6. Package Information

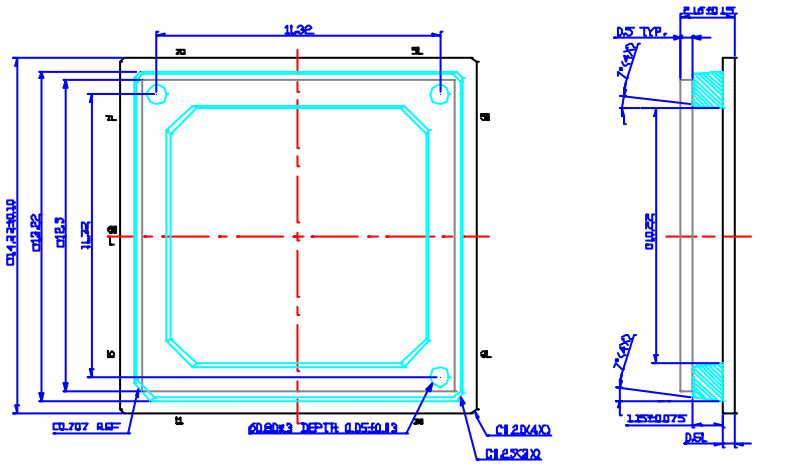
6.1 80-pin LCC

6.1.1 Pin connection diagram



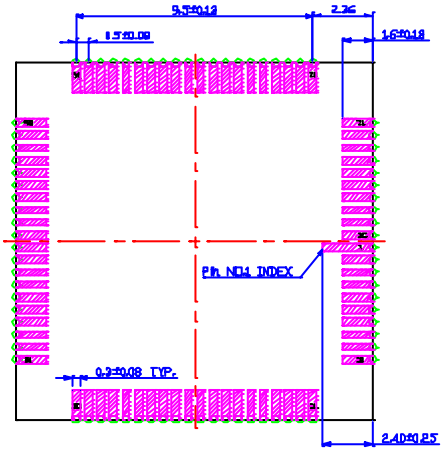
-- TOP VIEW --

6.1.2 Package outline



-- TOP VIEW --

-- SIDE VIEW --

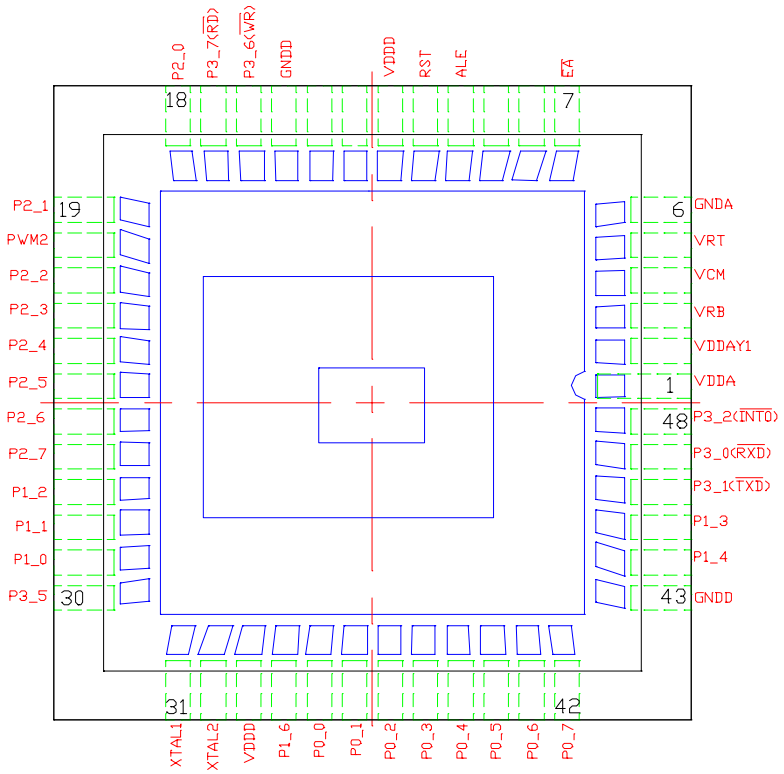


-- BOTTOM VIEW --

Unit: mm

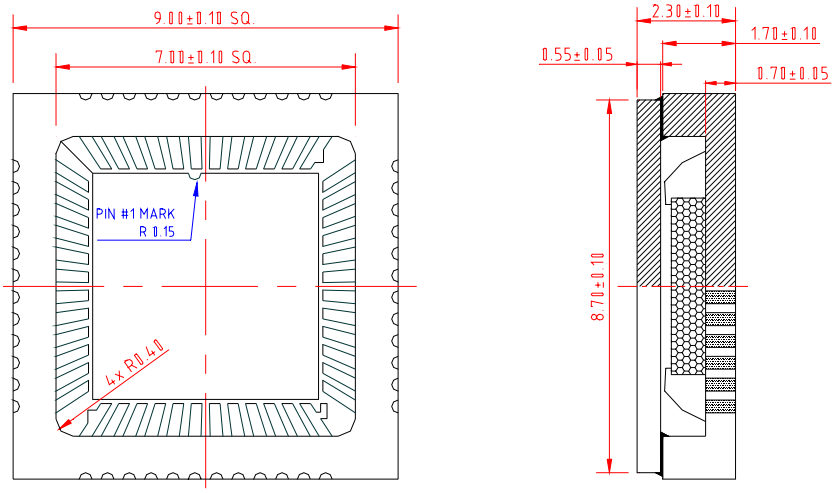
6.2 48-pin LCC

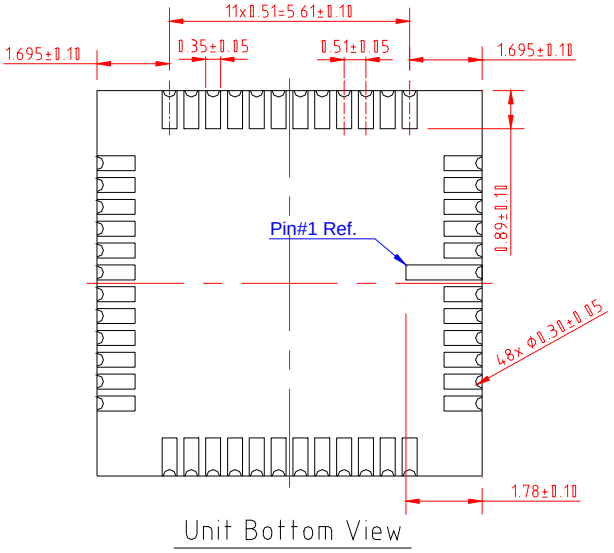
6.2.1 Pin connection diagram



-- Top View --

6.2.2 Package outline





7. Lens Information

7.1 Lens for 48-pin LCC package-1

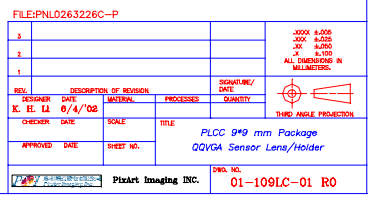
7.1.1 Lens

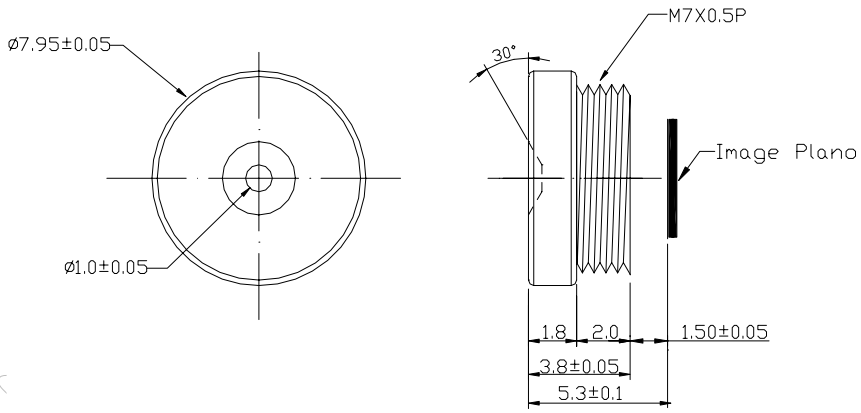
DIGITAL IMAGING LENS

Model No: PNL0263226C-P

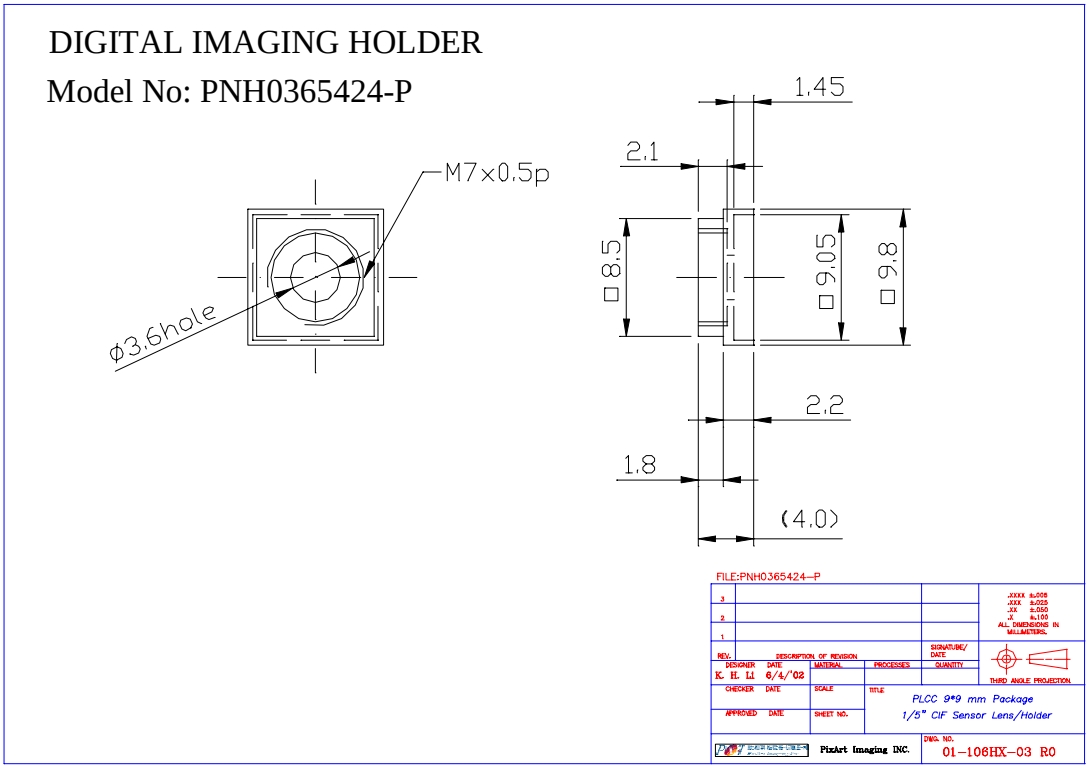
Lens Specification :

EFL (f) (Focal Length): 2.80 mm
BFL (Back Focal Length) : 2.50 mm
Flange Back Focal Length : 1.50 mm
F/# : 2.6
Diagonal field of view : 32°
Distortion : < -3.5%
Mount : M7 x P0.5 mm
Lens Construction : 1Plastic & 1 Filter
IR Cut-off Filter : 650+/-10 nm @ T50%



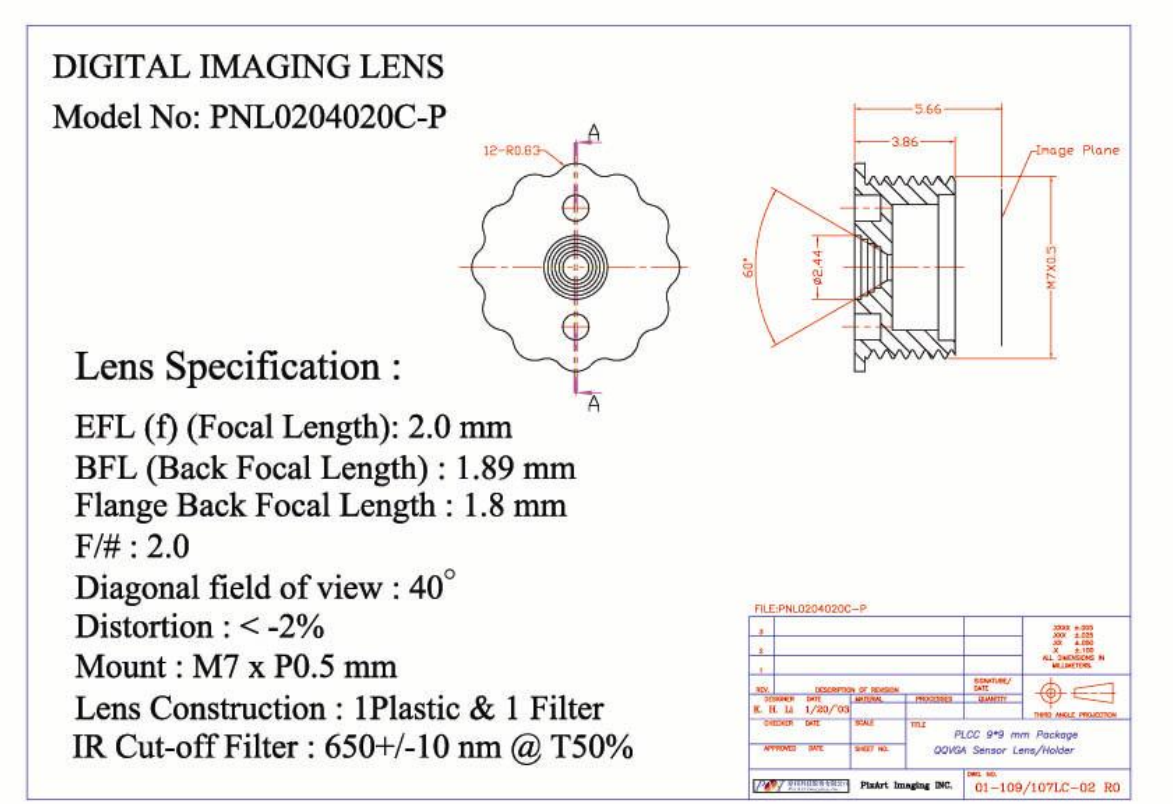


7.1.2 Holder

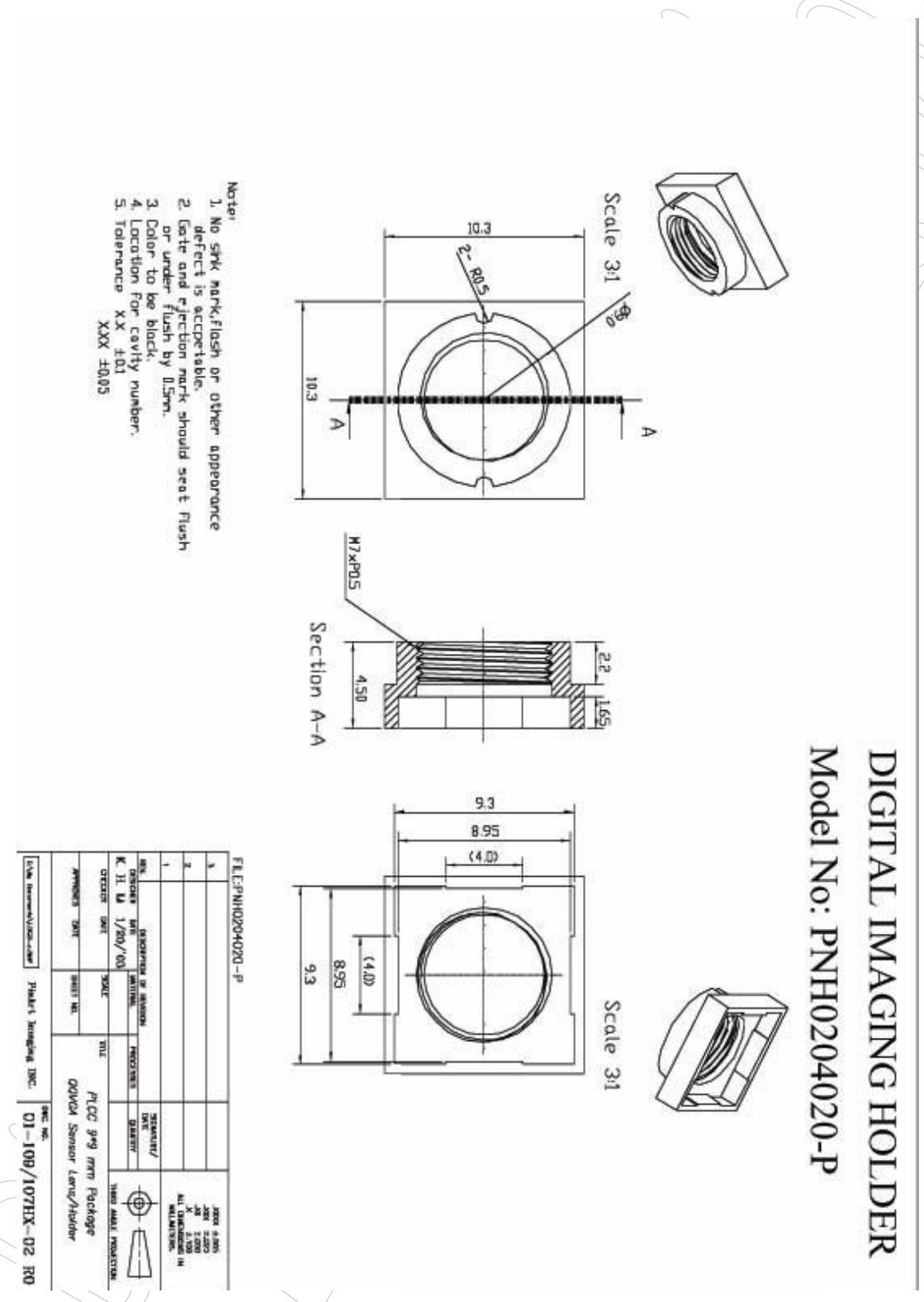


7.2 Lens for 48-pin LCC package-2

7.2.1 Lens

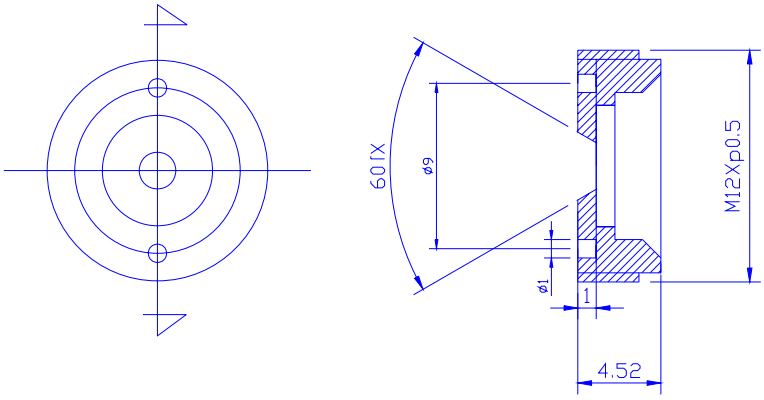


7.2.2 Holder



7.3 Lens for 80-pin LCC package

7.3.1 Lens



Specification
EFL : 2.0 mm
BFL : 1.89 mm
Fno: 2.0
Flange Back Focal Length : 1.12 mm
Field of View (for Pixart sensor)
Horizontal Field of View : 38.5°
Vertical Field of View: 32.5°
Diagonal Field of View: 40°
Distortion: -2%
IR Cut Coating : 650±10nm

7.3.2 Holder