

February 2008

FSB52006S

Smart Power Module (SPM)

Features

- 60V, R_{DS(ON).MAX}=80mΩ @ 25°C 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.
- · Surface mounted device package
- · Moisture Sensitive Level 3

General Description

FSB52006S is a tiny smart power module (SPM) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB52006S provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB52006S is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.

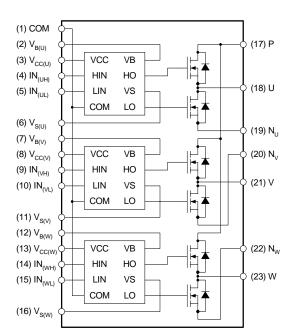


Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		60	V
I _{D25}	Each FRFET Drain Current, Continuous	T _C = 25°C	2.6	Α
I _{D100}	Each FRFET Drain Current, Continuous	$T_{C} = 100^{\circ}C$	1.3	Α
I _{DP}	Each FRFET Drain Current, Peak	T _C = 25°C, PW < 100μs	5	Α
P_{D}	Maximum Power Dissipation	T _C = 25°C, Each FRFET	11	W
V _{CC}	Control Supply Voltage	Applied between V _{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
V _{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ VCC+0.3	V
T_J	Operating Junction Temperature		-20 ~ 125	°C
T _{STG}	Storage Temperature		-50 ~ 150	°C
$R_{ heta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	9.2	°C/W
V _{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V _{rms}

Pin Descriptions

Pin Number	Pin Name	Pin Description	
1	СОМ	IC Common Supply Ground	
2	V _{B(U)}	Bias Voltage for U Phase High Side FRFET Driving	
3	V _{CC(U)}	Bias Voltage for U Phase IC and Low Side FRFET Driving	
4	IN _(UH)	Signal Input for U Phase High-side	
5	IN _(UL)	Signal Input for U Phase Low-side	
6	V _{S(U)}	Bias Voltage Ground for U Phase High Side FRFET Driving	
7	V _{B(V)}	Bias Voltage for V Phase High Side FRFET Driving	
8	V _{CC(V)}	Bias Voltage for V Phase IC and Low Side FRFET Driving	
9	IN _(VH)	Signal Input for V Phase High-side	
10	IN _(VL)	Signal Input for V Phase Low-side	
11	V _{S(V)}	Bias Voltage Ground for V Phase High Side FRFET Driving	
12	V _{B(W)}	Bias Voltage for W Phase High Side FRFET Driving	
13	V _{CC(W)}	Bias Voltage for W Phase IC and Low Side FRFET Driving	
14	IN _(WH)	Signal Input for W Phase High-side	
15	IN _(WL)	Signal Input for W Phase Low-side	
16	V _{S(W)}	Bias Voltage Ground for W Phase High Side FRFET Driving	
17	Р	Positive DC-Link Input	
18	U, V _{S(U)}	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving	
19	N _U	Negative DC-Link Input for U Phase	
20	N _V	Negative DC-Link Input for V Phase	
21	V, V _{S(V)}	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving	
22	N _W	Negative DC–Link Input for W Phase	
23	W, V _{S(W)}	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving	



Note:

Source terminal of each MOSFET is not connected to supply ground or bias voltage ground inside SPM. External connections should be made as indicated in Figure 2 and 5.

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

$\textbf{Electrical Characteristics} \ \, (\text{T}_{\text{J}} = 25^{\circ}\text{C}, \, \text{V}_{\text{CC}} = \text{V}_{\text{BS}} = 15 \text{V Unless Otherwise Specified})$

Inverter Part (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{IN} = 0V, I _D = 250μA (Note 2)		-	-	V
$\Delta BV_{DSS} / \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.06	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{IN} = 0V, V _{DS} = 60V	-	-	1	μА
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{CC} = V_{BS} = 15V, V_{IN} = 5V, I_D = 2.2A$	-	-	0.08	Ω
V_{SD}	Drain-Source Diode Forward Voltage	V _{CC} = V _{BS} = 15V, V _{IN} = 0V, I _D = -2.2A		-	1.0	٧
t _{ON}		$V_{PN} = 45V, V_{CC} = V_{BS} = 15V, I_D = 2.2A$		620	-	ns
t _{OFF}		$V_{IN} = 0V \leftrightarrow 5V$	-	360	-	ns
t _{rr}	Switching Times	Inductive load L=3mH High- and low-side FRFET switching	-	70	-	ns
E _{ON}			-	40	-	μJ
E _{OFF}		(Note 3)		5	-	μJ
RBSOA	Reverse-bias Safe Operating Area	V_{PN} = 55V, V_{CC} = V_{BS} = 15V, I_D = I_{DP} , V_{DS} =BV _{DSS} , T_J = 150°C High- and low-side FRFET switching (Note 4)	Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter		Conditions	Min	Тур	Max	Units
I _{QCC}	Quiescent V _{CC} Current	V _{CC} =15V, V _{IN} =0V	Applied between V _{CC} and COM	-	-	160	μΑ
I _{QBS}	Quiescent V _{BS} Current	V _{BS} =15V, V _{IN} =0V	$ \begin{array}{c} \text{Applied between } V_{B(U)}\text{-}V_{S(U)}, \\ V_{B(V)}\text{-}V_{S(V)}, \ V_{B(W)}\text{-}V_{S(W)} \end{array} $	-	-	100	μΑ
UV _{CCD}	Low-side Undervoltage	V _{CC} Undervoltage	Protection Detection Level	7.4	8.0	9.4	V
UV _{CCR}	Protection (Figure 6)	V _{CC} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV _{BSD}	High-side Undervoltage	V _{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV _{BSR}	Protection (Figure 7)	V _{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V _{IH}	ON Threshold Voltage	Logic High Level	Applied between IN and COM	3.0	-	-	V
V _{IL}	OFF Threshold Voltage	Logic Low Level	Applied between in and COM	-	-	0.8	V
I _{IH}	Input Pige Current	V _{IN} = 5V	Applied between IN and COM	-	10	20	μΑ
I _{IL}	Input Bias Current	V _{IN} = 0V	Applied between IN and COM	-	-	2	μΑ

Note:

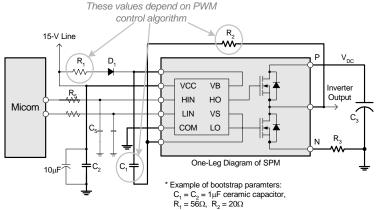
- 1. For the measurement point of case temperature $T_{\mbox{\scriptsize C}}$, please refer to Figure 3 in page 4.
- 2. BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.
- 3. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.
- 4. The peak current and voltage of each FRFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSB52006S	FSB52006S	SPM23-BA	330mm	Tape & reel	450

Recommended Operating Conditions

Symbol	Parameter	Conditions		Value		Units
	Parameter	Conditions	Min.	Тур.	Max.	Units
V_{PN}	Supply Voltage	Applied between P and N	-	45	55	V
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	13.5	15	16.5	V
V_{BS}	High-side Bias Voltage	Applied between V_B and V_S	13.5	15	16.5	V
V _{IN(ON)}	Input ON Threshold Voltage	Applied between IN and COM	3.0	-	V _{CC}	V
V _{IN(OFF)}	Input OFF Threshold Voltage	Applied between IIV and COM	0	-	0.6	V
t _{dead}	Blanking Time for Preventing Arm-short	$V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{V}, T_{J} \le 125 ^{\circ}\text{C}$	1.0	-	-	μS
f _{PWM}	PWM Switching Frequency	$T_J \le 125^{\circ}C$	_	15	-	kHz
T _C	Case Temperature	$T_J \le 125^{\circ}C$	-20	-	100	°C

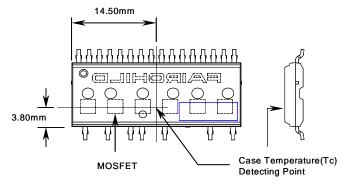


HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low-side FRFET On
1	0	V _{DC}	High-side FRFET On
1	1	Forbidden	Shoot-through
Open	Open	Z	Same as (0, 0)

Note:

- (1) It is recommended the bootstrap diode ${\rm D}_1$ to have soft and fast recovery characteristics with 100-V rating
- (2) Parameters for bootsrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- (3) RC coupling(R₅ and C₅) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM is compatible with standard CMOS or LSTTL outptus.
- (4) Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as C₁, C₂ and C₃ should have good high-frequency characteristics to absorb high-frequency ripple current.

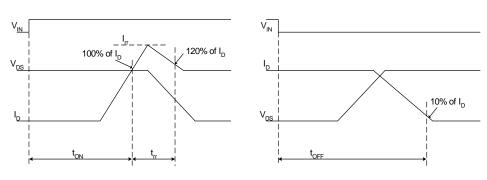
Figure 2. Recommended CPU Interface and Bootstrap Circuit with Parameters



Note:

Attach the thermocouple on top of the heatsink-side of SPM (between SPM and heatsink if applied) to get the correct temperature measurement.

Figure 3. Case Temperature Measurement



(a) Turn-on (b) Turn-off Figure 4. Switching Time Definition

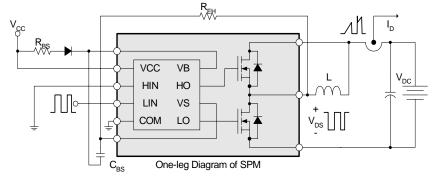


Figure 5. Switching and RBSOA(Single-pulse) Test Circuit (Low-side)

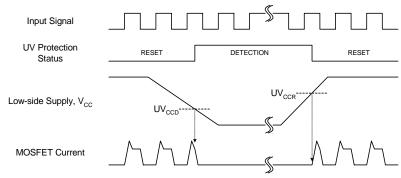


Figure 6. Undervoltage Protection (Low-side)

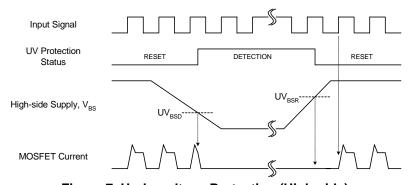


Figure 7. Undervoltage Protection (High-side)

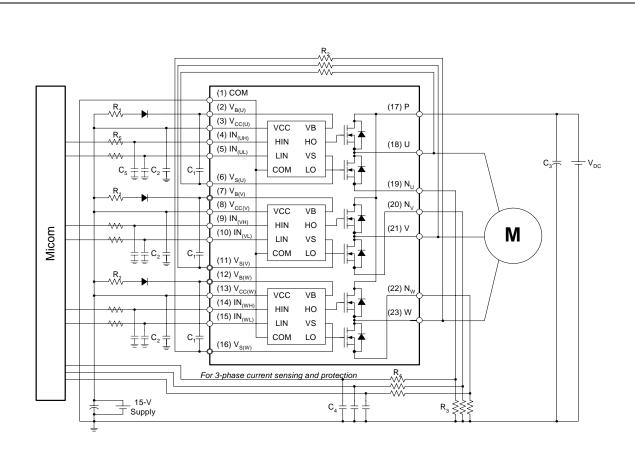
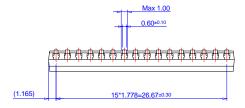
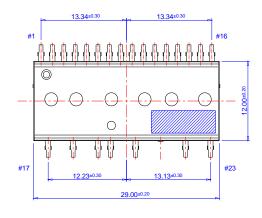
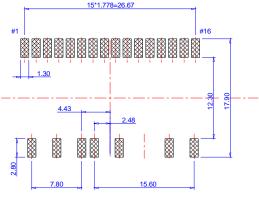


Figure 8. Example of Application Circuit

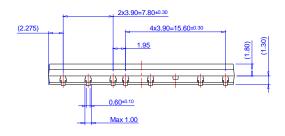
Detailed Package Outline Drawings

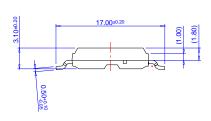


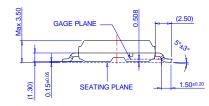




LAND PATTERN RECOMMENDATIONS







TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	GlobalOptoisolator™	Power247 [®]	SyncFET™
Across the board. Around the world.™	GTO™	PowerEdge™	TCM™
ActiveArray™	HiSeC™	PowerSaver™	The Power Franchise [®]
Bottomless™	i-Lo™	PowerTrench [®]	(I) TM
Build it Now™	ImpliedDisconnect™	Programmable Active Droop™	
CoolFET™	IntelliMAX™	QFET [®]	TinyBoost™
CROSSVOLT™	ISOPLANAR™	QS™	TinyBuck™
CTL™	MICROCOUPLER™	QT Optoelectronics™	TinyLogic [®]
Current Transfer Logic™	MicroPak™	Quiet Series™	TINYOPTO™
DOME™	MICROWIRE™	RapidConfigure™	TinyPower™
E ² CMOS TM	MSX™	RapidConnect™	TinyWire™
EcoSPARK [®]	MSXPro™	ScalarPump™	TruTranslation™
EnSigna™	OCX™	SMART START™	µSerDes™
FACT Quiet Series™	OCXPro™	SPM [®]	UHC®
FACT [®]	OPTOLOGIC [®]	STEALTH™	UniFET™
FAST [®]	OPTOPLANAR [®]	SuperFET™	VCX™
FASTr™	PACMAN™	SuperSOT™-3	Wire™
FPS™	POP™	SuperSOT™-6	
FRFET [®]	Power220 [®]	SuperSOT™-8	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS Definition of Terms

Datasheet Identification		Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I15