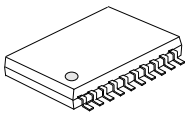
U74AHC374

CMOS IC

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



TSSOP-20

■ DESCRIPTION

The **U74AHC374** is a octal edge-triggered D-type flip-flops with 3-state outputs and it has 8 channels.

When the $\overline{OE}$ input is low, on the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

When the $\overline{OE}$ input is high, the outputs are in the high-impedance.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

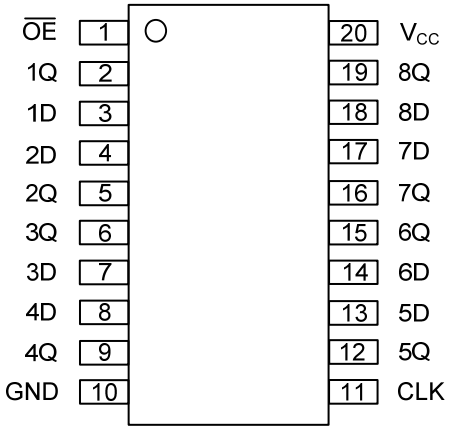
* Operate from 2V to 5.5V
* Max t_{PD} of 12.7ns at V_{CC}=3.3V, C_L=15pF
* Max I_{CC} of 4uA
* Typ V_{OL}< 0.36V at V_{CC}=4.5V,I_O=8mA,T_A=25°C
* Typ V_{OH}> 3.94V at V_{CC}=4.5V,I_O=-8mA, T_A=25°C

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC374L-P20-R	U74HC374G-P20-R	TSSOP-20	Tape Reel
U74HC374L-P20-T	U74HC374G-P20-T	TSSOP-20	Tube

U74AHC374L-P20-R (1)Packing Type (2)Package Type (3)Lead Free	(1) R: Tape Reel, T: Tube (2) P20: TSSOP-20 (3) G: Halogen Free, L: Lead Free

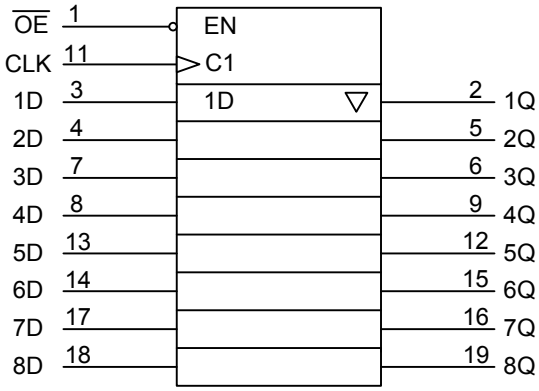
■ PIN CONFIGURATION



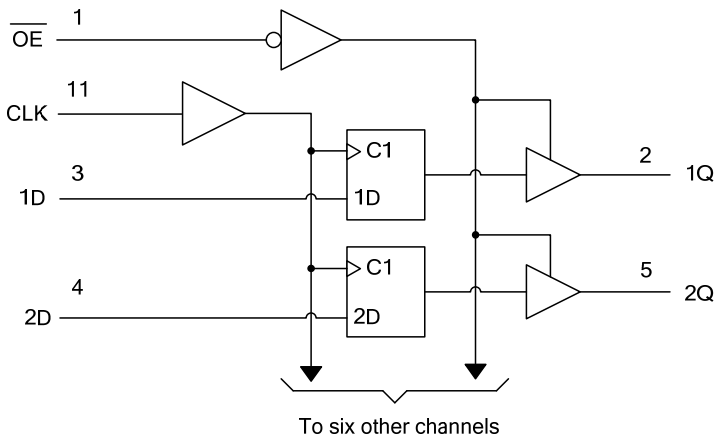
■ FUNCTION TABLE

INPUTS($\overline{OE}$)	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	↑	H	H
L	↑	L	L
L	H or L	X	Q0
H	X	X	Z

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Voltage	V_{IN}	-0.5 ~ 7	V
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5	V
V_{CC} or GND Current	I_{CC}	±75	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Operating Temperature	T_{OPR}	-40 ~ + 85	℃
Storage Temperature	T_{STG}	-65 ~ + 150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2		5.5	V
High-level Input Voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=3V	2.1			
		V_{CC}=5.5V	3.85			
Low-level Input Voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=3V			0.9	
		V_{CC}=5.5V			1.65	
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
High-level Output Current	I_{OH}	V_{CC} = 2 V			-50	μA
		V_{CC} = 3.3 V ± 0.3 V			-4	mA
		V_{CC} = 5 V ± 0.5 V			-8	
Low-level Output Current	I_{OL}	V_{CC} = 2 V			50	μA
		V_{CC} = 3.3 V ± 0.3 V			4	mA
		V_{CC} = 5 V ± 0.5 V			8	
Input Rise or Fall Times	t_R, t_F	V_{CC} = 3.3 V ± 0.3 V			100	ns
		V_{CC} = 5 V ± 0.5 V			20	

■ ELECTRICAL CHARACTERISTICS (T_A=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	V_{CC}=2V, I_{OH}=-50μA	1.9	2		V
		V_{CC}=3V, I_{OH}=-50μA	2.9	3		
		V_{CC}=4.5V, I_{OH}=-50μA	4.4	4.5		
		V_{CC}=3V, I_{OH}=-4mA	2.58			
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			
Output Voltage Low-Level	V_{OL}	V_{CC}=2V, I_{OH}=50μA			0.1	V
		V_{CC}=3V, I_{OH}=50μA			0.1	
		V_{CC}=4.5V, I_{OH}=50μA			0.1	
		V_{CC}=3V, I_{OH}=4mA			0.36	
		V_{CC}=4.5V, I_{OH}=8mA			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}= 0 to 5.5V, V_{IN}=5.5V or GND			±0.1	μA
3-state Leakage Current	I_{OZ}	V_{CC}=5.5V, V_{OUT}= V_{CC} or GND			±0.25	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	μA
Input Capacitance	C_I	V_{CC}=5V, V_{IN}=V_{CC} or GND		4	10	pF
Output Capacitance	C_O	V_{CC}=5V, V_{OUT}=V_{CC} or GND		6		pF

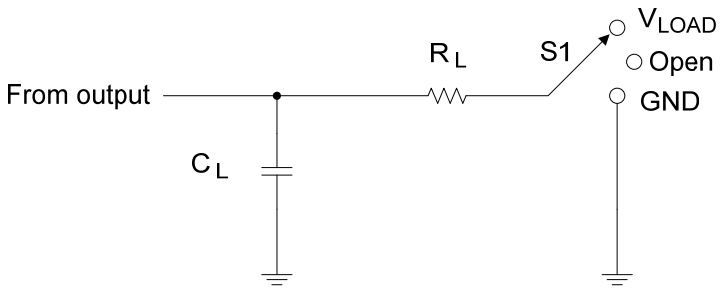
■ SWITCHING CHARACTERISTICS (See TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
From CLK to Q	t_{PLH}/t_{PHL}	V_{CC} = 3.3V ± 0.3V	C_L =15pF		8.1	12.7	ns
			C_L =50pF		10.6	16.2	
		V_{CC} = 5V ± 0.5V	C_L =15pF		5.4	8.1	
			C_L =50pF		6.9	10.1	
From $\overline{OE}$ to Q	t_{PZL}/t_{PZH}	V_{CC} = 3.3V ± 0.3V	C_L =15pF		7.1	11	ns
			C_L =50pF		9.6	14.5	
		V_{CC} = 5V ± 0.5V	C_L =15pF		5.1	7.6	
			C_L =50pF		6.6	9.6	
From $\overline{OE}$ to Q	t_{PLZ}/t_{PHZ}	V_{CC} = 3.3V ± 0.3V	C_L =15pF		7.5	10.5	ns
			C_L =50pF		10.2	14	
		V_{CC} = 5V ± 0.5V	C_L =15pF		4.6	6.8	
			C_L =50pF		6.1	8.8	
Maximum Clock Frequency	f_{MAX}	V_{CC} = 3.3V ± 0.3V	C_L =15pF	80	130		MHz
			C_L =50pF	55	85		
		V_{CC} = 5V ± 0.5V	C_L =15pF	130	185		
			C_L =50pF	85	120		
Pulse Width	t_W	V_{CC} = 3.3 V ± 0.3 V		5			ns
		V_{CC} = 5 V ± 0.5 V		5			
Setup Time	t_{SU}	V_{CC} = 3.3 V ± 0.3 V		4.5			ns
		V_{CC} = 5 V ± 0.5 V		3			
Hold Time	t_H	V_{CC} = 3.3 V ± 0.3 V		2			ns
		V_{CC} = 5 V ± 0.5 V		2			

■ OPERATING CHARACTERISTICS(T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	C_{PD}	No load, V_{CC} = 5 V, f=1MHz	32	pF

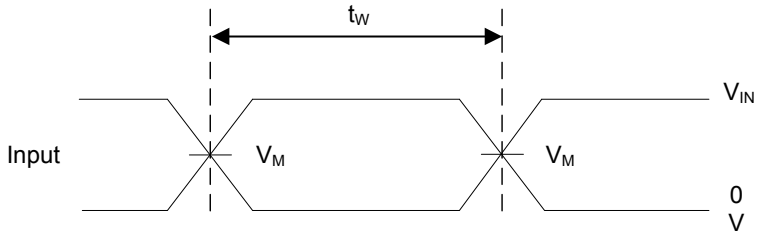
■ TEST CIRCUIT AND WAVEFORMS



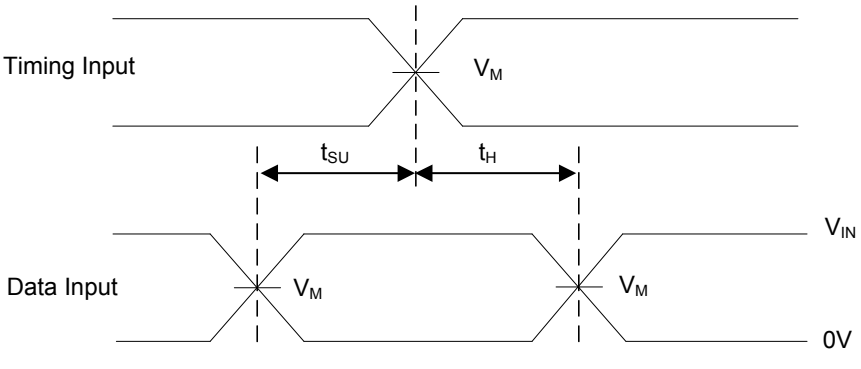
TEST CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
3.3V±0.3V	V_{CC}	≤3ns	$V_{CC}/2$	V_{CC}	15pF 50pF	1kΩ	0.3V
5V±0.5V	V_{CC}	≤3ns	$V_{CC}/2$	V_{CC}	15pF 50pF	1kΩ	0.5V

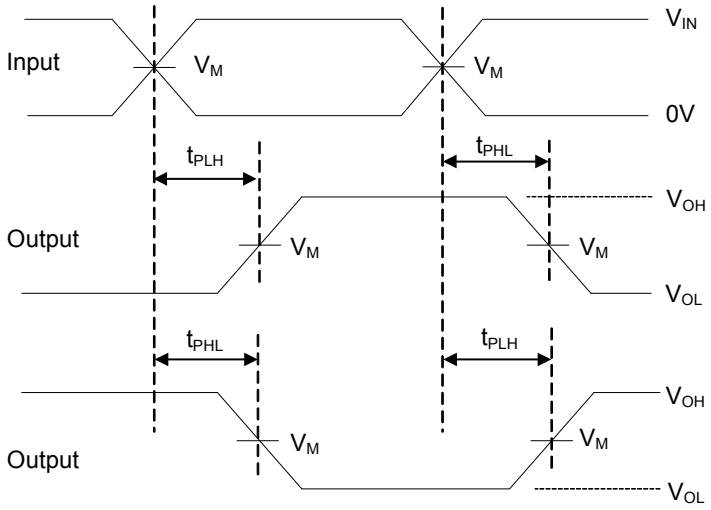


Pulse Duration

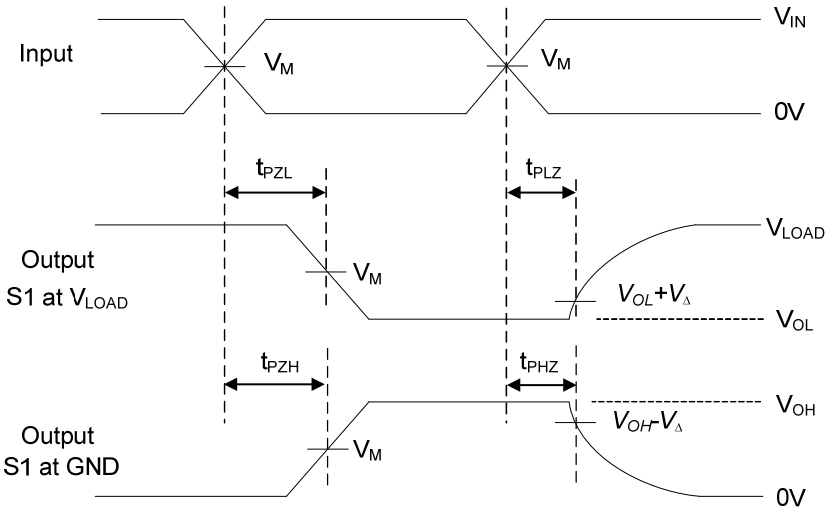


Setup and Hold Times

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enble and Disable Times

Note: A. C_L includes probe and jig capacitance.

B. P_{RR} ≤1MHz, Z_O = 50Ω, t_R ≤3ns, t_F ≤3ns.