MP8666

6A, 21V, 600kHz Step-Down Converter with Synchronizable Gate Driver

The Future of Analog IC Technology

DESCRIPTION

The MP8666 is a monolithic step-down switch mode converter with a built in high-side internal power MOSFET and a gate driver for a low-side external MOSFET. It achieves 6A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP8666 requires a minimum number of readily available standard external components and is available in an 8-pin SOIC package with exposed pad.

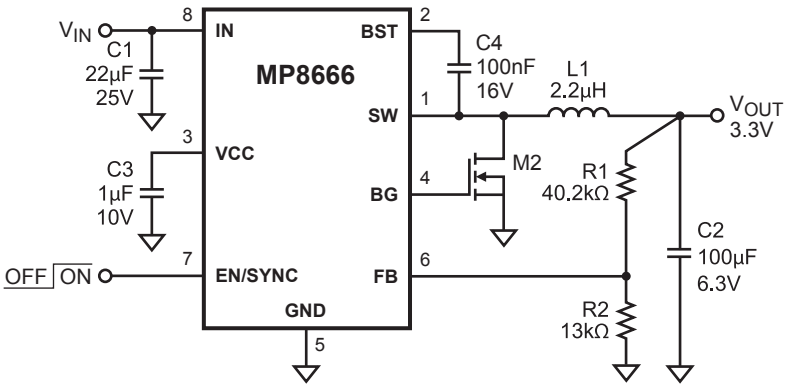
FEATURES

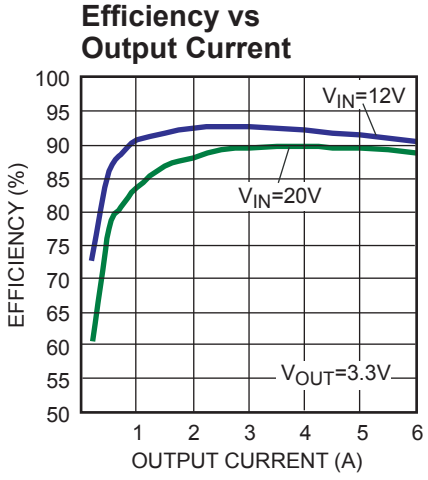
- Wide 4.5V to 21V Operating Input Range
- 6A Continuous Output Current
- 45mΩ Internal Power MOSFET Switch
- Synchronizable Gate Driver Delivers up to 95% Efficiency
- Fixed 600KHz Frequency
- Synchronizable up to 1.5MHz
- Cycle-by-Cycle Over Current Protection with Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Stable with Low ESR Output Ceramic Capacitors
- Available in a Thermally Enhanced 8-Pin SOIC Package

APPLICATIONS

- Point of Load Regulator in Distributed Power System
- Digital Set Top Boxes
- Personal Video Recorders
- Broadband Communications
- Flat Panel Television and Monitors

TYPICAL APPLICATION



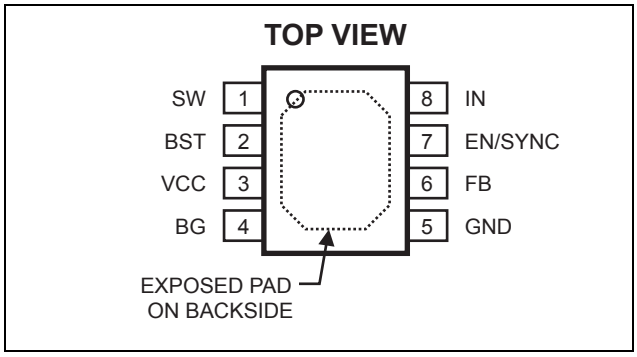


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP8666DN	SOIC8E	MP8666DN	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP8666DN–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP8666DN–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 23V
V_{SW} .....-0.3V(-5V for < 10ns) to 24V
V_{BST} - V_{SW} 6V
All Other Pins .....–0.3V to +6V
Continuous Power Dissipation (T_A = +25°C)(2)
SOIC8E 2.5W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.5V to 21V
Operating Temperature..... –40°C to +85°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8E ..... 50 ..... 10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 21V	0.788	0.808	0.828	V
Feedback Current	I_{FB}	V_{FB} = 0.8V		10		nA
Switch On Resistance (5)	$R_{DS(ON)}$			45		mΩ
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Current Limit (5)			7.5	8.0		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	400	600	800	KHz
Fold-back Frequency		V_{FB} = 0V	60	150	240	KHz
Maximum Duty Cycle		V_{FB} = 0.6V	85	90		%
Minimum On Time (5)	t_{ON}			100		ns
Under Voltage Lockout Threshold Rising	$V_{CC\ UVLO}$		3.9	4.1	4.3	V
Under Voltage Lockout Threshold Hysteresis				880		mV
EN Input Low Voltage					0.4	V
EN Input High Voltage			1.2			V
EN Input Current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
Sync Frequency Range (Low)	F_{SYNCL}			300		KHz
Sync Frequency Range (High)	F_{SYNCH}			1.5		MHz
Enable Turnoff Delay	T_{OFF}			5.0		us
Supply Current (Shutdown)		V_{EN} = 0V		1	10	μA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V		0.9	1.1	mA
Thermal Shutdown	T_J			150		°C
Thermal Shutdown Hysteresis				10		°C
BG Driver Bias Supply Voltage	V_{CC}		4.5	5		V
Gate Driver Sink Impedance (5)	R_{SINK}			1		Ω
Gate Driver Source Impedance (5)	R_{SOURCE}			4		Ω
Gate Drive Current Sense Trip Threshold	V_{SW}			20		mV

Note:

5) Guaranteed by design.

PIN FUNCTIONS

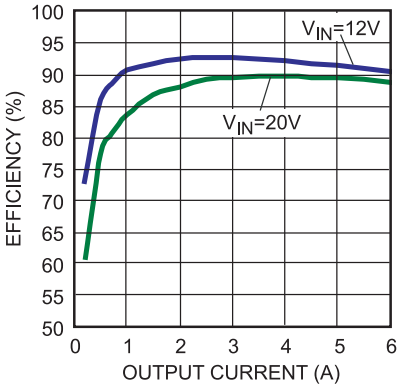
Pin #	Name	Description
1	SW	Switch Output.
2	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BS pins to form a floating supply across the power switch driver.
3	VCC	BG Driver Bias Supply. Decouple with a 1µF ceramic capacitor. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
4	BG	Gate Driver Output. Connect this pin to the gate of the synchronous MOSFET.
5	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the M2 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
6	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV.
7	EN/SYNC	On/Off Control and External Frequency Synchronization Input.
8	IN	Supply Voltage. The MP8666 operates from a +4.5V to +21V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.

TYPICAL PERFORMANCE CHARACTERISTICS

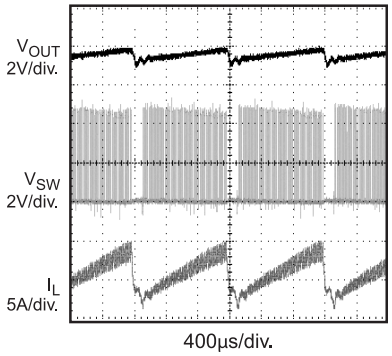
V_{IN} = 12V, V_{OUT} = 2.5V, L = 2.2µH, T_A = +25ºC, unless otherwise noted.

Efficiency vs Output Current

V_{OUT} = 3.3V

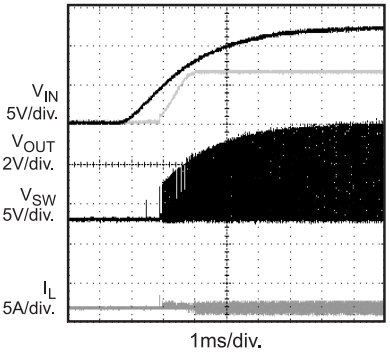


Hiccup with Outupt Short Circuit



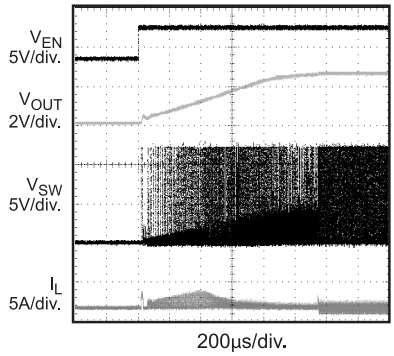
Power up

No Load



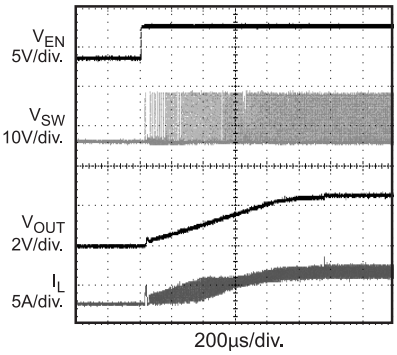
Startup through Enable

No Load



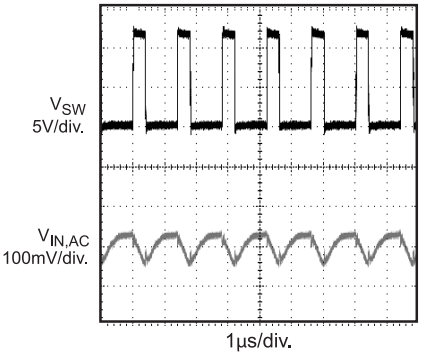
Startup through Enable

I_{OUT} = 6A (Resistive Load)



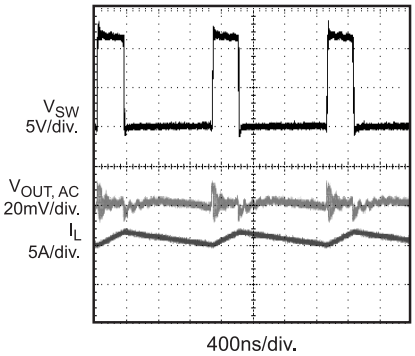
Input Ripple Voltage

I_{OUT} = 6A



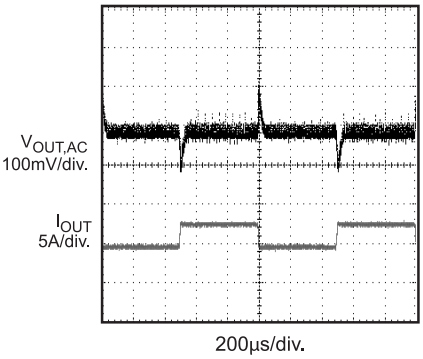
Output Ripple Voltage

I_{OUT} = 6A

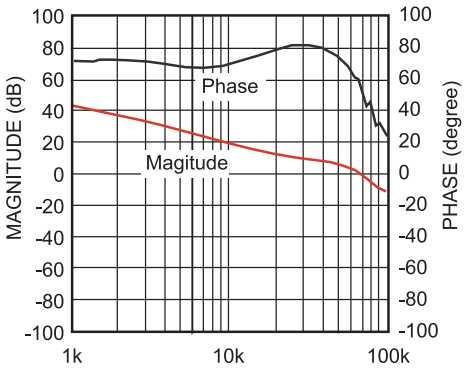


Load Transient Response

I_{OUT} = 1A to 4A step @ 1A/ms



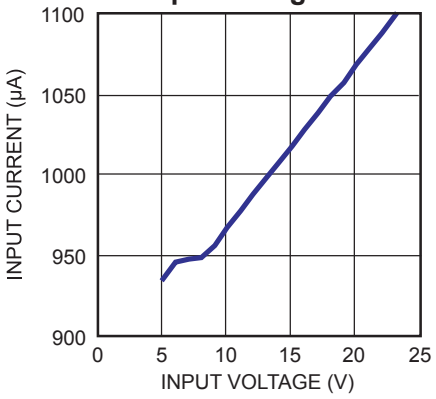
Close Loop Bode Plot



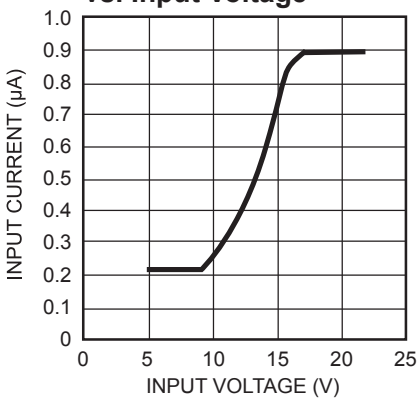
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 2.5V, L = 2.2µH, T_A = +25ºC, unless otherwise noted.

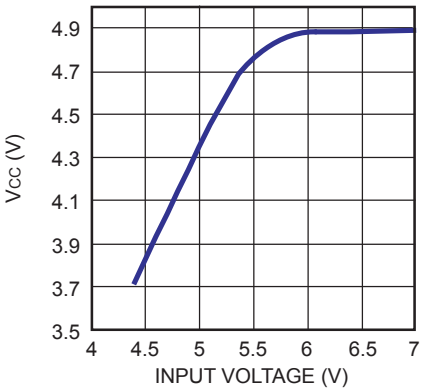
Enabled Supply Current vs. Input Voltage



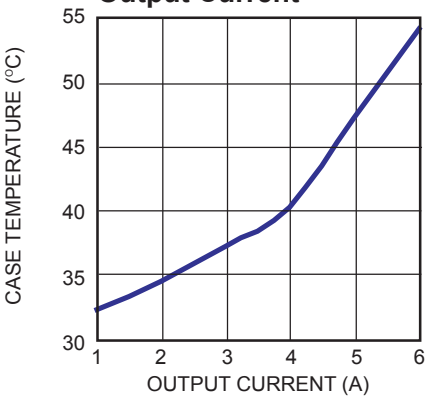
Disabled Supply Current vs. Input Voltage



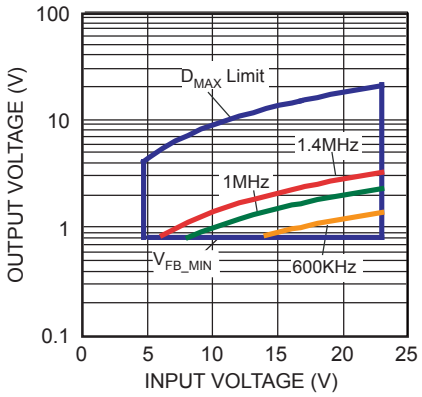
Vcc Regulator Line Regulation (Icc = 10mA)



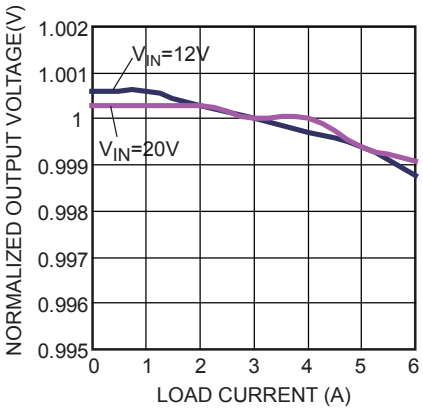
Case Temperature vs. Output Current



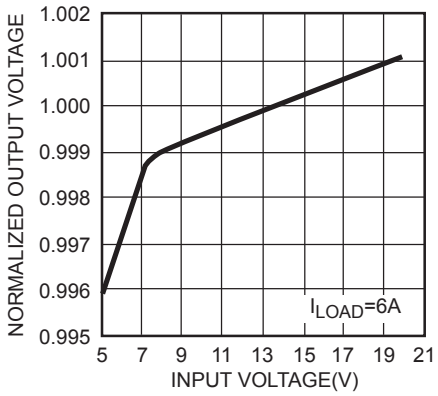
Operating Range



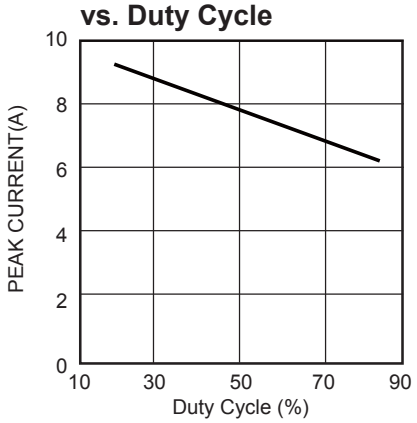
Load Regulation



Line Regulation



Peak Current vs. Duty Cycle



OPERATION

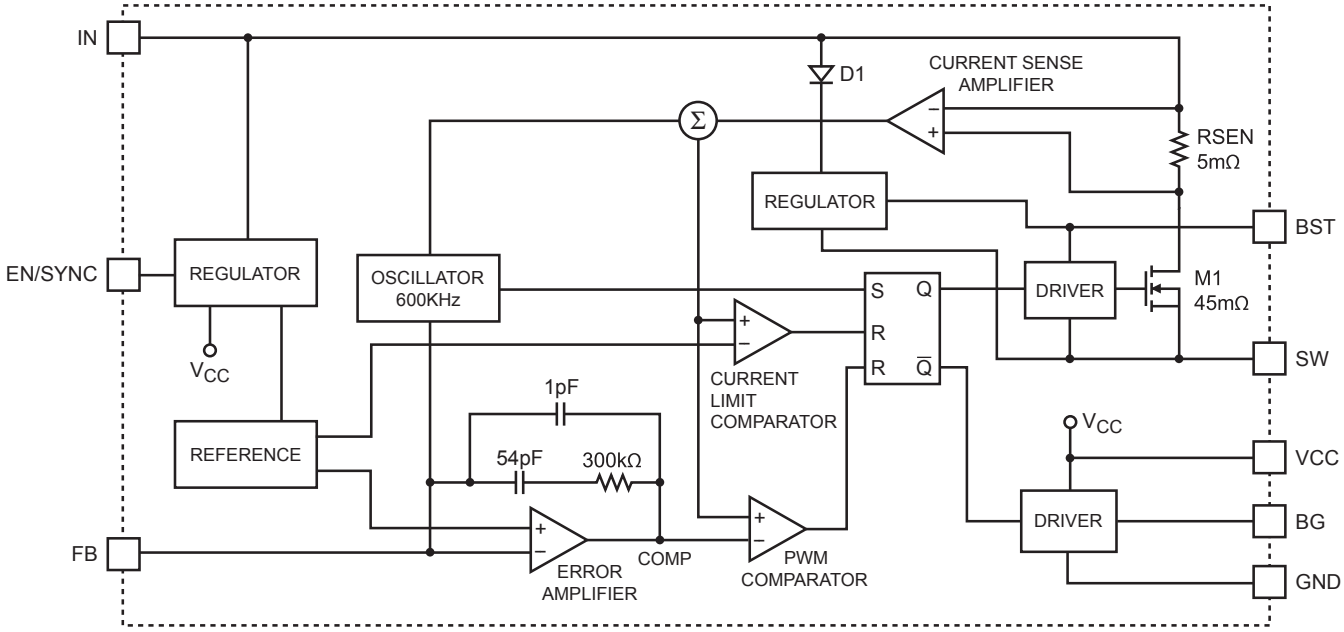


Figure 1—Functional Block Diagram

The MP8666 is a fixed frequency, synchronous, step-down switching regulator with an integrated high-side power MOSFET and a gate driver for a low-side external MOSFET. It achieves 6A continuous output current over a wide input supply range with excellent load and line regulation. It provides a single highly efficient solution with current mode control for fast loop response and easy compensation.

The MP8666 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases. Since this internal regulator provides the bias current for the bottom gate driver that requires significant amount of current depending upon the external MOSFET selection, a 1μF ceramic capacitor for decoupling purpose is required.

Enable/Synch Control

The MP8666 has a dedicated Enable/Synch control pin (EN/SYNC). By pulling it high or low, the IC can be enabled and disabled by EN. Tie EN to VIN for automatic start up. To disable the part, EN must be pulled low for at least 5μs.

The MP8666 can be synchronized to external clock range from 300KHz up to 1.5MHz through the EN/SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP8666 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

Over-Current-Protection and Hiccup

The MP8666 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the MP8666 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MP8666 exits the hiccup mode once the over current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M3, C4, L1 and C2 (Figure 2). If (V_{IN}-V_{SW}) is more than 5V, U2 will regulate M3 to maintain a 5V BST voltage across C4.

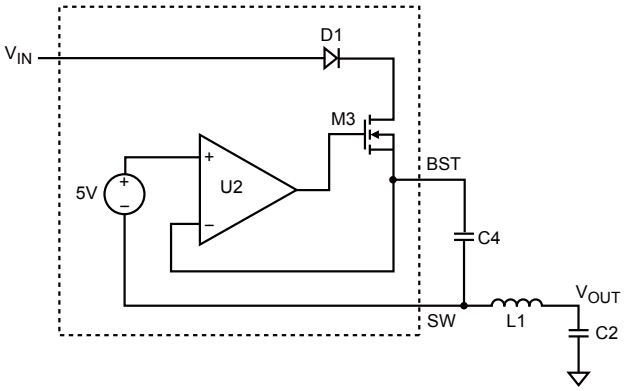


Figure 2—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

The schematic on the front page shows a typical MP8666 application. The IC can provide up to 6A output current at a nominal output voltage of 3.3V. For proper thermal performance, the exposed pad of the device must be soldered down to the printed circuit board.

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.808V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	40.2 (1%)	32.4 (1%)
2.5	40.2 (1%)	19.1 (1%)
3.3	40.2 (1%)	13 (1%)
5	40.2 (1%)	7.68 (1%)

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current, 6A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Synchronous MOSFET

The external synchronous MOSFET is used to supply current to the inductor when the internal high-side switch is off. It significantly reduces the power loss when compared against a Schottky rectifier.

Table 2 lists example synchronous MOSFETs and manufacturers.

Table 2—Synchronous MOSFET Selection Guide

Part No.	Manufacture
FDS6670AS	Fairchild
IRF7821	International Rectifier
AM4874	Analog Power

Selecting the Input Capacitor

The input capacitor (C1) reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For 6A output applications, a 22μF capacitor is sufficient.

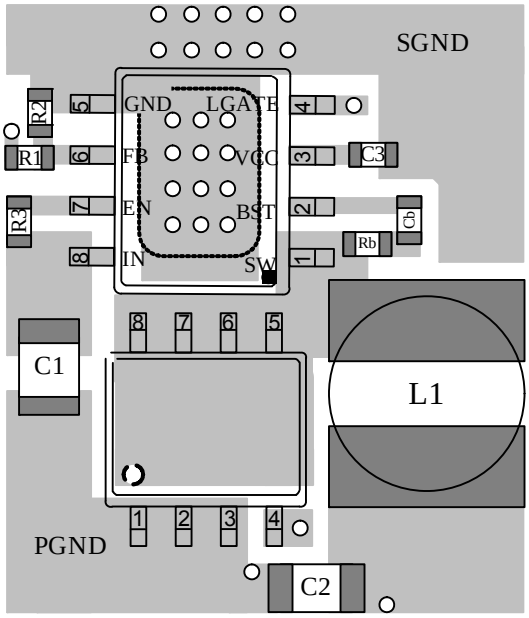
Selecting the Output Capacitor

The output capacitor (C2) keeps output voltage small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

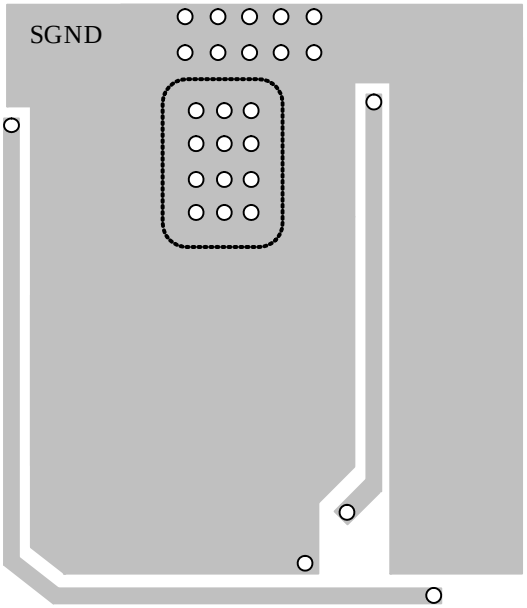
PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure3 for references.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side and low-side MOSFETs.
2) Keep the connection of low-side MOSFET between SW pin and input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer



Bottom Layer

Figure 3—PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode is:

- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Fig.4

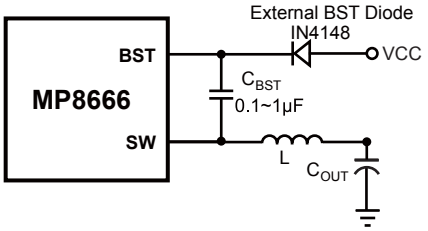
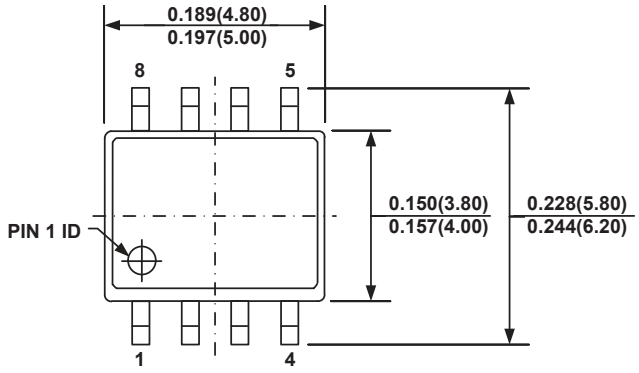


Figure 4—Add Optional External Bootstrap Diode to Enhance Efficiency

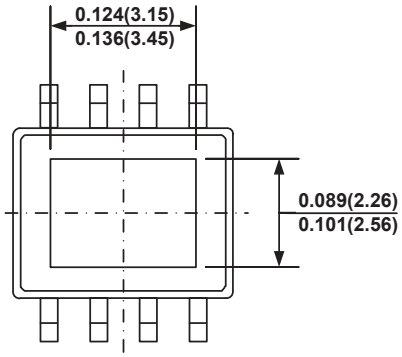
The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

PACKAGE INFORMATION

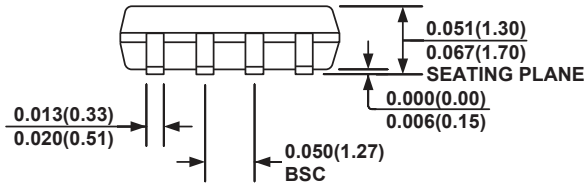
SOIC8E (EXPOSED PAD)



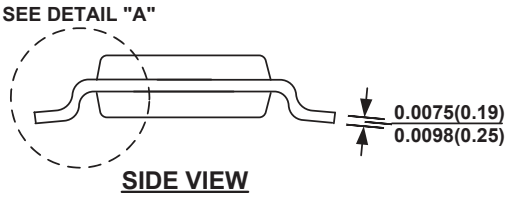
TOP VIEW



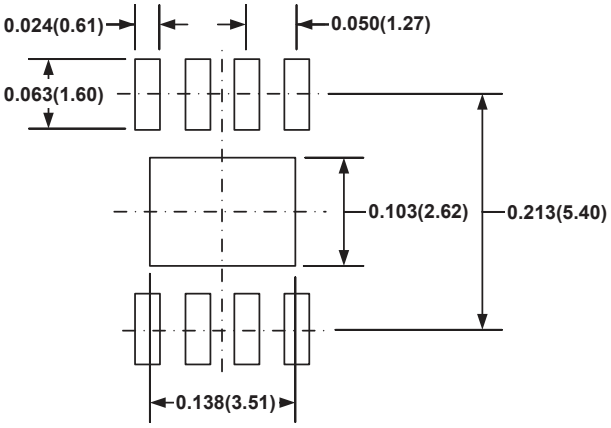
BOTTOM VIEW



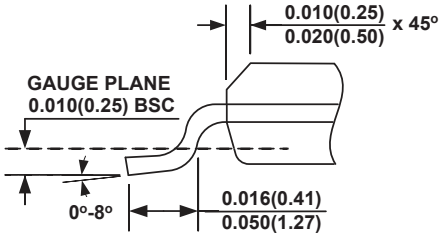
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.