TMC1175
CMOS 8-Bit Video A/D Converter

Description

The TMC1175 analog-to-digital (A/D) converter employs a two-step architecture with integral track/hold. The device converts analog signals into 8-bit digital words at rates up to 40 Msps (Megasamples per second). The architecture and CMOS technology reduce typical power dissipation to less than 150 mW.

The TMC1175 operates from a single +5 Volt power supply and has internal voltage reference resistors which allow self-bias operation. The input capacitance is very low, simplifying the design of, or eliminating, the need for video driving amplifiers. All digital inputs and three-state outputs are TTL-compatible.

The TMC1175 is available in 24-pin plastic DIP, 24-Lead plastic SOIC, and 28-lead J-lead PLCC packages. Mil-temperature versions are available in CERDIP or ceramic LCC packages. Performance specifications are guaranteed over the -20 to 75°C and -55 to 125°C temperature ranges.

Features

- ◆ 8-bit resolution
- ◆ 10, 20, and 40 Msps conversion rate
- ◆ Integral track/hold

- ◆ Differential linearity error <±0.5 LSB
- ◆ Single +5V Power Supply
- ◆ <150 mW power dissipation
- ◆ Differential phase <0.5°
- ◆ Differential gain <1%
- ◆ Three-state 3V TTL-compatible outputs
- ◆ Very low cost

Applications

- ◆ Digital television
- ◆ Video digitizing
- ◆ Low cost, high speed data conversion
- ◆ Image scanners
- ◆ Personal computer video boards
- ◆ Multimedia

Related Products

- ◆ TMC1173 Low-Voltage, Low-Power 8-Bit Video A/D Converter
- ◆ TMC22070 Genlocking Video Digitizer
- ◆ TDC3310 10-Bit Video D/A Converter
- ◆ TMC22090/TMC22190 Digital Video Encoder
- ◆ TMC2242/TMC2243/TMC2246 Video Filter
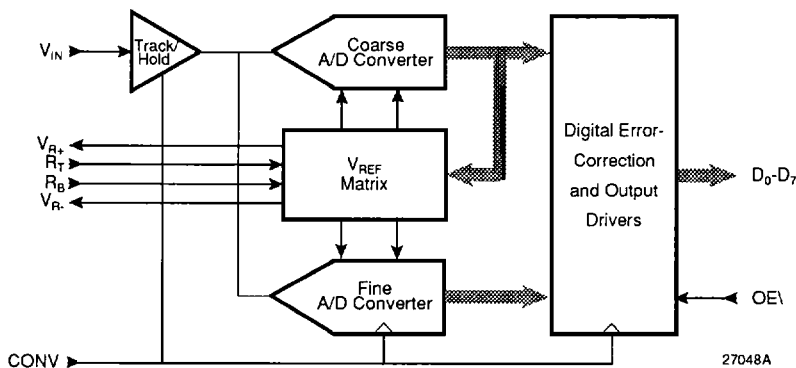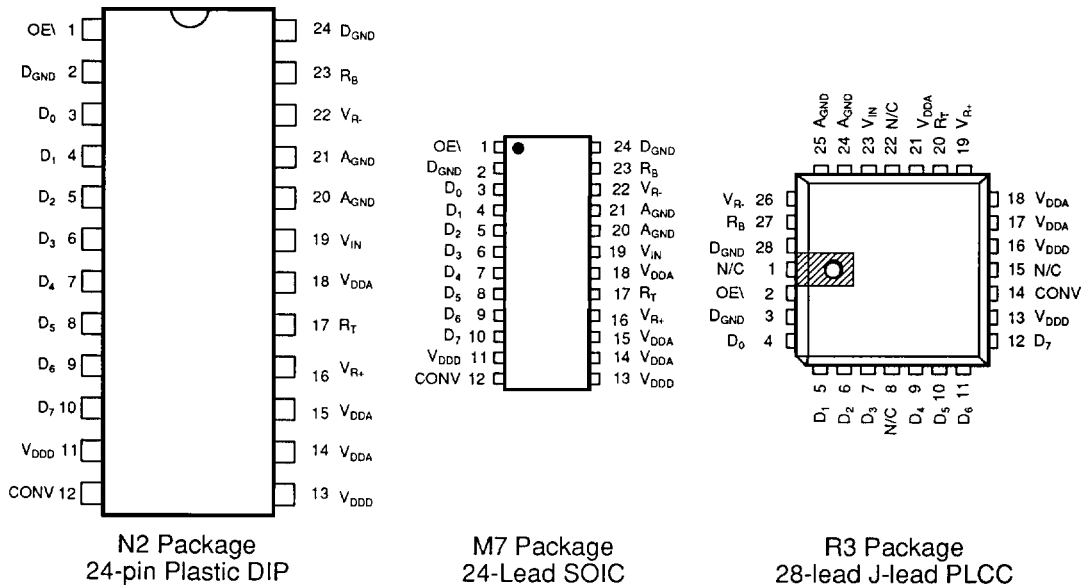- ◆ TMC2302 Image Manipulation Sequencer

Block Diagram

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TMC1175

Figure 2. Pin Assignments and Packages

N2 Package	M7 Package	R3 Package
24-pin Plastic DIP	24-Lead SOIC	28-lead J-lead PLCC

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General Description

The TMC1175 is an 8-bit A/D converter which uses a two-step architecture to perform analog-to-digital conversion at rates up to 40 Msps. The input signal is held in an integral track/hold stage during the conversion process. Pipelined operation is achieved with one input sample taken and one output word provided for each convert cycle. The first step in the conversion process is a coarse 4-bit conversion. The coarse 4-bit result determines the range of the subsequent fine 4-bit A/D conversion step. To eliminate spurious codes, the fine 4-bit A/D converter output is gray-coded and converted to binary before combining with the coarse result to form the complete 8-bit result.
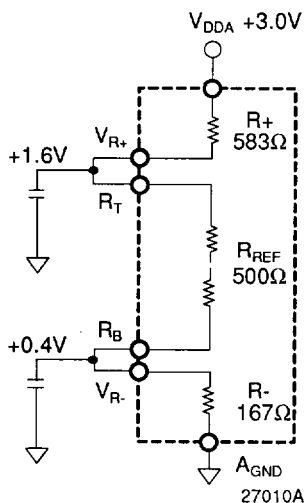
Analog Input and Voltage References

The TMC1175 converts analog signals in the range $R_T \leq V_{IN} \leq R_B$ into digital data. The A/D converter input range is very flexible and extends from the +5 Volt power supply to ground. Normally, external

voltage reference sources are connected to the R_T and R_B pins or R_B is grounded.

Two reference pull-up and pull-down resistors connected to V_{R+} and V_{R-}, are provided for operation without external voltage reference circuitry. These voltages applied to R_T and R_B may be generated externally, or are self-generated by connecting V_{R+} to R_T and V_{R-} to R_B. In the latter case the power supply voltage is divided by on-chip resistors to bias the R_T and R_B points.

The self-bias reference voltages are useful in applications where overall circuit cost is important and absolute accuracy and stability of the A/D converter gain is not critical.

The V_{IN} input range is from R_B to R_T. The device will not be damaged by signals within the range A_{GND} to V_{DD}.

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Figure 3. Reference Resistors

V_{DDA} +3.0V

+1.6V V_{R+}

R+ 583Ω

R_T

R_{REF} 500Ω

+0.4V R_B

V_{R-}

R- 167Ω

A_{GND}

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Table 1. Output Coding Table

Input Voltage	Output Code MSB LSB
$<R_B$	00000000
R_B	00000000
R_B + 1 LSB	00000001
•	•
•	•
$(R_T + R_B)/2$	01111111
$(R_T + R_B)/2$ + 1 LSB	10000000
•	•
•	•
R_T - 1 LSB	11111110
R_T	11111111
$>R_T$	11111111

Note: 1 LSB = $(R_T - R_B)/255$

Digital Inputs and Outputs

The sampling of the applied input signal takes place on the falling edge of the CONV signal. The output word is available after the rising edge of CONV, delayed by 2 1/2 CONV cycles. The output remains valid for t_{HO} (Output Hold Time) and new data becomes valid t_D (Output Delay Time) after the rising edge of CONV.

The outputs of the TMC1175 are TTL-compatible and are capable of driving four low-power Schottky TTL (54/74LS) loads. An output enable control, OE\, places the outputs in a high-impedance state when HIGH. The outputs are enabled when OE\ is LOW.

Power and Ground

The TMC1175 operates from a single +5 Volt power supply. For optimum performance, it is recommended that A_{GND} and D_{GND} pins of the TMC1175 be connected to the system analog ground plane.

Pin Functions

V_{IN} The input voltage conversion range extends from the voltage applied to the R_T and R_B pins.

R_T, R_B The top and bottom inputs to the reference resistor ladder. DC voltages applied to R_T and R_B define the V_{IN} conversion range.

V_{R+}, V_{R-} Internal pull-up and pull-down reference resistors used in self-bias operation.

CONV   A/D converter clock input. V_{IN} is sampled on the falling edge of CONV.

OE\   Output Enable. When LOW, D_0-D_7 are enabled. When HIGH, D_0-D_7 are in a high-impedance state.

D_0-D_7 Eight-bit TTL-compatible digital outputs. Valid data is output on the rising edge of CONV.
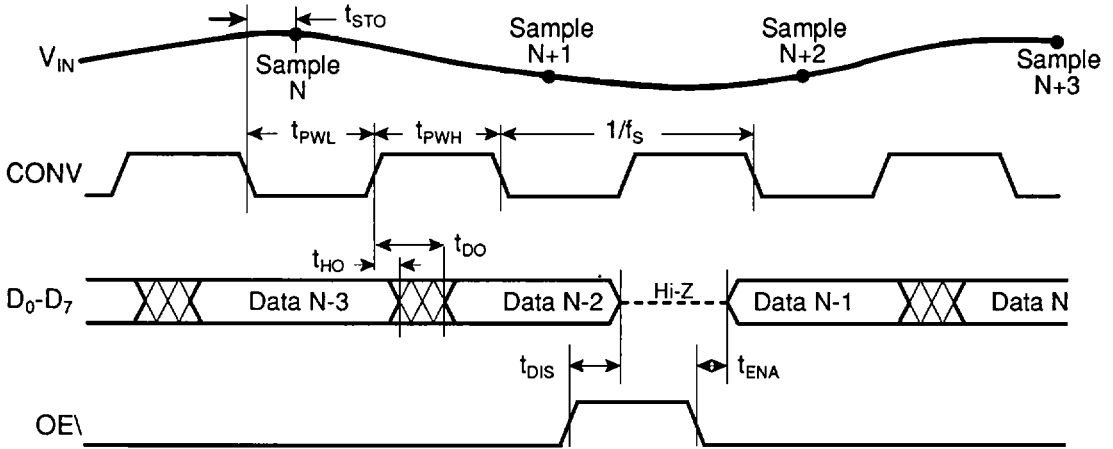
TMC1175

V_{DDA}, V_{DDD} +5 Volt power inputs. These should come from the same power source and be decoupled to A_{GND}.

A_{GND}, D_{GND} Ground inputs should be connected to the system analog ground plane.

Table 2. Package Interconnections

Signal Type	Name	Function	Value	N2, M7 Pin	R3, C3 Pin
Inputs	V_{IN}	Analog Input	R_B-R_T	19	23
	R_T	Reference Voltage Top Input	2.6V	17	20
	R_B	Reference Voltage Bottom Input	0.6V	23	27
	V_{R+}	Reference Voltage Top Source	2.6V	16	19
	V_{R-}	Reference Voltage Bottom Source	0.6V	22	26
	OE\	Output enable	TTL	1	2
	CONV	Convert (Clock) input	TTL	12	14
Outputs	D_0	Least Significant Bit	TTL	3	4
	D_1		TTL	4	5
	D_2		TTL	5	6
	D_3		TTL	6	7
	D_4		TTL	7	9
	D_5		TTL	8	10
	D_6		TTL	9	11
	D_7	Most Significant Bit	TTL	10	12
Power	V_{DDA}	Analog Supply Voltage	+5V	14, 15, 18	17, 18, 21
	V_{DDD}	Digital Supply Voltage	+5V	11, 13	13, 16
	A_{GND}	Analog Ground	0.0V	20, 21	24, 25
	D_{GND}	Digital Ground	0.0V	2, 24	3, 28
No Connect	N/C	Not Connected	open		1, 8, 15, 22

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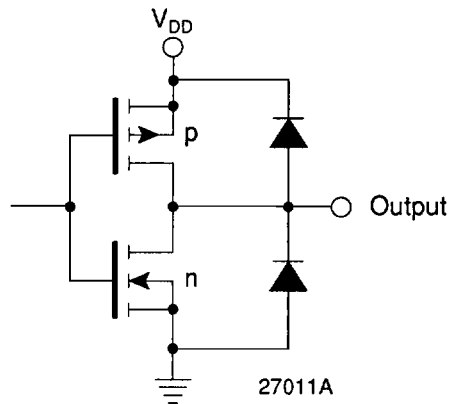**Figure 4. Timing Diagram**

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Figure 5. Equivalent Digital Input Circuit
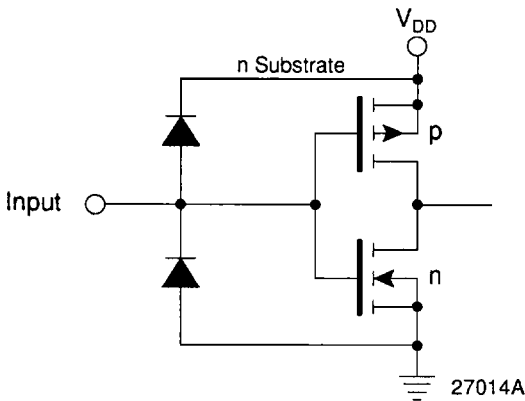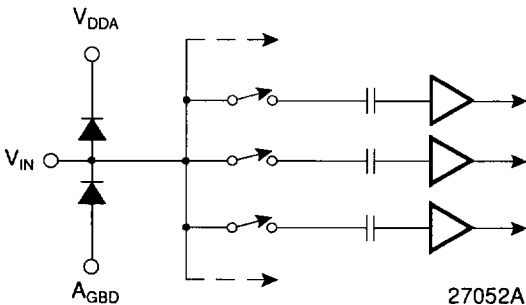

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Figure 7. Equivalent Digital Output Circuit
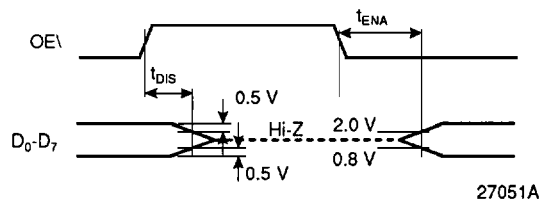

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Figure 6. Equivalent Analog Input Circuit

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Figure 8. Transition Levels for Three-State Measurements

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Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{DDA} (measured to A_{GND})..-0.5 to +7.0V

V_{DDD} (measured to D_{GND})..-0.5 to +7.0V

V_{DDA} (measured to V_{DDD})..-0.5 to +0.5V

D_{GND} (measured to A_{GND})..-0.5 to +0.5V

Inputs

Applied voltage[2] CONV, OE\ ....-0.5 to V_{DDD} V

Applied voltage[2] R_T, R_B, V_{IN} [2]...A_{GND} to V_{DDA} V

Outputs

Applied Voltage[2]...-0.5 to (V_{DD}+0.5) V

Forced Current[3,4]...-6.0 to 6.0 mA

Short Circuit Duration

(Single output in HIGH state to GND)...1 second

Temperature

Operating, ambient...-55 to +125°C

Junction..+140°C

Lead, soldering (10 seconds)..+300°C

Vapor phase soldering (1 minute)..+220°C

Storage..-65 to +150°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
   2. Applied voltage must be current limited to specified range, and measured with respect to GND.
   3. Forcing voltage must be limited to specified range.
   4. Current is specified as conventional current, flowing into the device.

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Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
T_A	Ambient Temperature, Still Air	-20		75				°C
T_C	Case Temperature, Still Air				-55		125	°C
V_{DDA}	Analog Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{DDD}	Digital Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
A_{GND}	Analog Ground Voltage (Measured to D_{GND})	-0.1	0	0.1	-0.1	0.0	0.1	V
f_S	Conversion Rate							
	TMC1175-20	20			20			Msps
	TMC1175-30	30						Msps
	TMC1175-40	40						Msps
t_{PWH}	CONV pulse width, HIGH							
	TMC1175-20	15			17			ns
	TMC1175-30	13						ns
	TMC1175-40	12						ns
t_{PWL}	CONV pulse width, LOW							
	TMC1175-20	15			17			ns
	TMC1175-30	15						ns
	TMC1175-40	12						ns
R_T	Reference, Top	0		V_{DD}	0		V_{DD}	V
R_B	Reference, Bottom	0		2.7	0		2.7	V
$R_T - R_B$	Reference Voltage Differential	1.8		5	1.8		5	V
V_{IN}	Analog Input Range	R_B		R_T	R_B		R_T	V
V_{IH}	Input Voltage, Logic HIGH	4.0			4.0			V
V_{IL}	Input Voltage, Logic LOW			1.0			1.0	V
I_{OH}	Output Current, Logic HIGH			-1.5			-1.0	mA
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA

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Electrical characteristics

Parameter		Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
I_{DD}	Total Power Supply Current	$V_{DDA}=V_{DDD}$=Max, worst-case, C_{LOAD} = 35pF							
		TMC1175-20, f_S = 20 Msps		35	60		35	65	mA
		TMC1175-30, f_S = 30 Msps		43	70				mA
		TMC1175-40, f_S = 40 Msps		50	80				mA
I_{DDQ}	Quiescent Power Supply Current	$V_{DDA}=V_{DDD}$=Max,CONV=LOW		13			13		mA
		$V_{DDA}=V_{DDD}$=Max,CONV=HIGH		24			24		mA
P_D	Total Power Dissipation	$V_{DDA} = V_{DDD}$ = Nom, C_{LOAD} = 35pF							
		TMC1175-20, f_S = 20 Msps		175			175		mW
		TMC1175-30, f_S = 30 Msps		215					mW
		TMC1175-40, f_S = 40 Msps		250					mW
C_{IN}	Input Capacitance	CONV = HIGH		16	18		16	18	pF
R_{IN}	Input Resistance		100			100			kΩ
I_{CB}	Analog Input Current				±5			±10	µA
I_{REF}	Reference Current			7.5	10.5		7.5	10.5	mA
R_{REF}	Reference Resistance		190	270		190	270		Ω
V_{RT}	Ref. Voltage, Top	$R_B = V_{R-}$, $R_T = V_{R+}$		2.6			2.6		V
V_{RB}	Ref. Voltage, Bottom	$R_B = V_{R-}$, $R_T = V_{R+}$		0.6			0.6		V
V_{RT} -V_{RB}	Ref.Voltage Diff.	$R_B = V_{R-}$, $R_T = V_{R+}$		2.0			2.0		V
I_{IH}	Input Current, HIGH	V_{DD} = Max, $V_{IN} = V_{DD}$			±5			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±5			±10	µA
I_{OZH}	Leakage Current, HIGH	OE\ = HIGH, $V_{OUT} = V_{DD}$			±5			±10	µA
I_{OZL}	Leakage Current, LOW	OE\ = HIGH, $V_{OUT} = D_{GND}$			±5			±10	µA
I_{OS}	Short-Circuit Current				30			30	mA
V_{OH}	Output Voltage, HIGH	D_{0-7}, I_{OH} = Max	4.0			4.0			V
V_{OL}	Output Voltage, LOW	D_{0-7}, I_{OH} = Max			0.4			0.4	V

Note: Values shown in Typ column are typical for V_{DD} = +5.0 V and T_A = 25°C.

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Switching Characteristics

Parameter		Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	Units
t_{STO}	Sampling Time Offset	TMC1175-20	0	3	8	0	5	10	ns
		TMC1175-30	0	3	8				ns
		TMC1175-40	0	3	8				ns
t_{DO}	Output Delay Time	$C_{LOAD} = 15pF$							
		TMC1175-20			30			38	ns
		TMC1175-30			30				ns
		TMC1175-40			20				ns
t_{HO}	Output Hold Time	$C_{LOAD} = 15pF$							
		TMC1175-20	5			5			ns
		TMC1175-30	5						ns
		TMC1175-40	5						ns
t_{ENA}	Output Enable Time				65			65	ns
t_{DIS}	Output Disable Time				65			65	ns

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System Performance Characteristics

Parameter		Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
E_{LI}	Integral Linearity Error	$R_B = V_{R-}, R_T = V_{R+}$		±0.75	±1.0			±1.0	LSB
		$R_B = A_{GND}, R_T = +2.5$ V		±0.75	±1.0		±0.75		LSB
		$R_B = A_{GND}, R_T = V_{DDA}$		±0.75			±0.75		LSB
E_{LD}	Differential Linearity Error	$R_B = V_{R-}, R_T = V_{R+}$		±0.3	±0.5			±0.5	LSB
		$R_B = A_{GND}, R_T = +2.5$ V		±0.3	±0.5		±0.3		LSB
		$R_B = A_{GND}, R_T = V_{DDA}$		±0.3			±0.3		LSB
CS	Code Size		10		190	5		195	%nom
BW	Bandwidth	TMC1175-20			10			10	MHz
		TMC1175-30			12				MHz
		TMC1175-40, $V_{DD} = 5.0$V, $T_A = 0°C$ to $70°C$			12				MHz
E_{ap}	Aperture Error			30			30		ps
E_{OT}	Offset Voltage, Top	$R_T - V_{IN}$ for most positive code transition			-75			-75	mV
E_{OB}	Offset Voltage, Bottom	$R_B - V_{IN}$ for most negative code transition			±40			±40	mV
DG	Differential Gain	$f_S = 14.3$ Msps, NTSC 40 IRE ramp, for $R_B = V_{R-}, R_T = V_{R+}$ and $R_B = A_{GND}, R_T = +2.5$ V $V_{DD} = +5.0$ V, $T_A = 25°C$			2.0			2.0	%
DP	Differential Phase	$f_S = 14.3$ Msps, NTSC 40 IRE ramp, for $R_B = V_{R-}, R_T = V_{R+}$ and $R_B = A_{GND}, R_T = +2.5$ V $V_{DD} = +5.0$ V, $T_A = 25°C$			1.0			1.0	°

Note: Values shown in Typ column are typical for $V_{DD} = +5.0$ V and $T_A = 25°C$. Bandwidth is the frequency band in which a full-scale sinewave can be digitized without spurious codes.

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## System Performance Characteristics

Parameter	Conditions	Standard			Extended			Units
		Min	Typ	Max	Min	Typ	Max	
SNR Signal-to-Noise Ratio	TMC1175-20, f_S = 20 Msps,							
	f_{IN} = 1.24 MHz	44	46		43	46		dB
	f_{IN} = 2.48 MHz	43	45		42	45		dB
	f_{IN} = 6.98 MHz	42	45		40	45		dB
	f_{IN} = 10.0 MHz	42	45		40	45		dB
	TMC1175-30, f_S = 30 Msps,							
	t_{PWH} = 13 ns							
	f_{IN} = 1.24 MHz	42	44					dB
	f_{IN} = 6.98 MHz	41	43					dB
	f_{IN} = 10.0 MHz	40	43					dB
	f_{IN} = 12.0 MHz	39	42					dB
	TMC1175-40, f_S = 40 Msps,							
	T_A = 0°C to 70°C							
	f_{IN} = 1.24 MHz	40	43					dB
	f_{IN} = 6.98 MHz	39	42					dB
	f_{IN} = 10.0 MHz	38	41					dB
	f_{IN} = 12.0 MHz	38	41					dB
SFDR Spurious Free Dynamic Range	TMC1175-20, f_S = 20 Msps,							
	f_{IN} = 1.24 MHz	44	51		41	51		dB
	f_{IN} = 2.48 MHz	43	47		39	47		dB
	f_{IN} = 6.98 MHz	32	38		30	38		dB
	f_{IN} = 10.0 MHz	30	35		27	35		dB
	TMC1175-30, f_S = 30 Msps,							
	f_{IN} = 1.24 MHz	42	48					dB
	f_{IN} = 6.98 MHz	32	36					dB
	f_{IN} = 10.0 MHz	30	34					dB
	f_{IN} = 12.0 MHz	28	32					dB
	TMC1175-40, f_S = 40 Msps,							
	T_A = 0°C to 70°C							
	f_{IN} = 1.24 MHz	41	44					dB
	f_{IN} = 6.98 MHz	31	34					dB
	f_{IN} = 10.0 MHz	30	33					dB
	f_{IN} = 12.0 MHz	30	32					dB

Note: SNR values do not include the harmonics of the fundamental frequency.
SFDR is the ratio in dB of fundamental amplitude to the harmonic with highest amplitude.
Values shown in Typ column are typical for V_{DD} = +5.0 V and T_A = 25°C.

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Figure 9. Typical Interface Circuit



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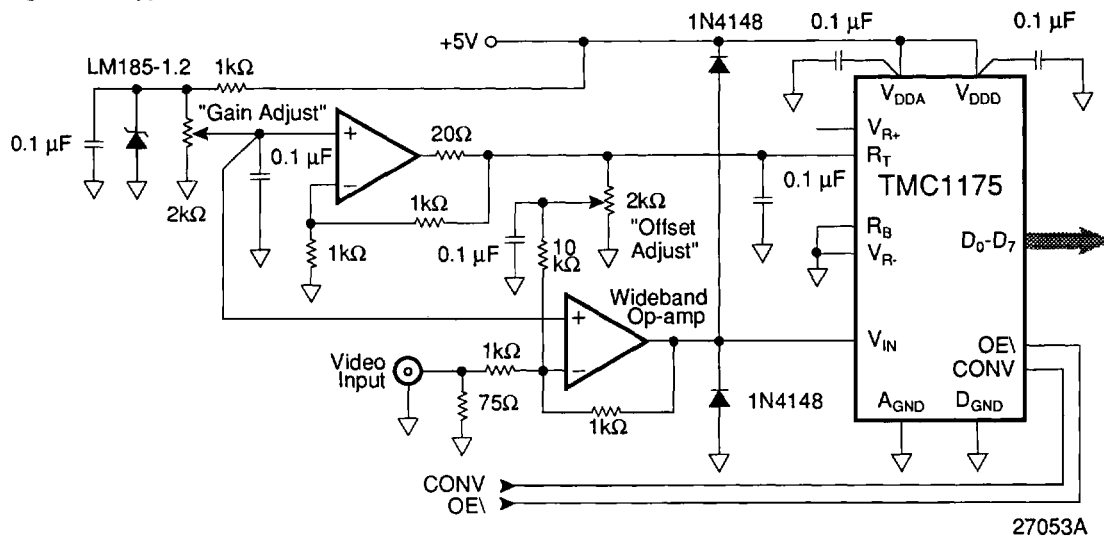
Application Notes

The circuit in Figure 9 uses a band-gap reference to generate a variable R_T reference voltages for the TMC1175 as well as a bias voltage to offset the wideband input amplifier to mid-range. An "offset adjust" is also shown for varying the mid-range voltage level. The operational amplifier in the reference circuitry is a standard general-purpose 741-type.

The voltage reference is variable from 0.0 to 2.4 volts on R_T while R_B is grounded. Note the diode clamps on the wideband op-amp output. These prevent the A/D input from being driven beyond the power supply. Diode protection is advised as good practice to limit analog input voltages to within the power supply range.

The circuit in Figure 10a shows the self-bias of R_T and R_B by connection to V_{R+} and V_{R-}. This sets up a 0.6 to 2.6 Volt input range for V_{IN}. The input range is susceptible to power supply variation since the voltages on R_T and R_B are directly derived from V_{DDA}. The video input is AC-coupled and biased at a variable midpoint of the A/D input range. This circuit offers the advantage of minimum support circuitry for the most cost-sensitive applications.

In Figure 10b, an external band-gap reference sets R_T to +1.2 Volts while R_B is grounded. The internal pull-up resistor, R+, provides the bias current for the band-gap diode. The input impedance of the Rf input is approximately 50Ω and the A/D converter input is biased at the mid-point of the input range.

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Figure 10. Typical Interface Circuit

(a.)

(b.)

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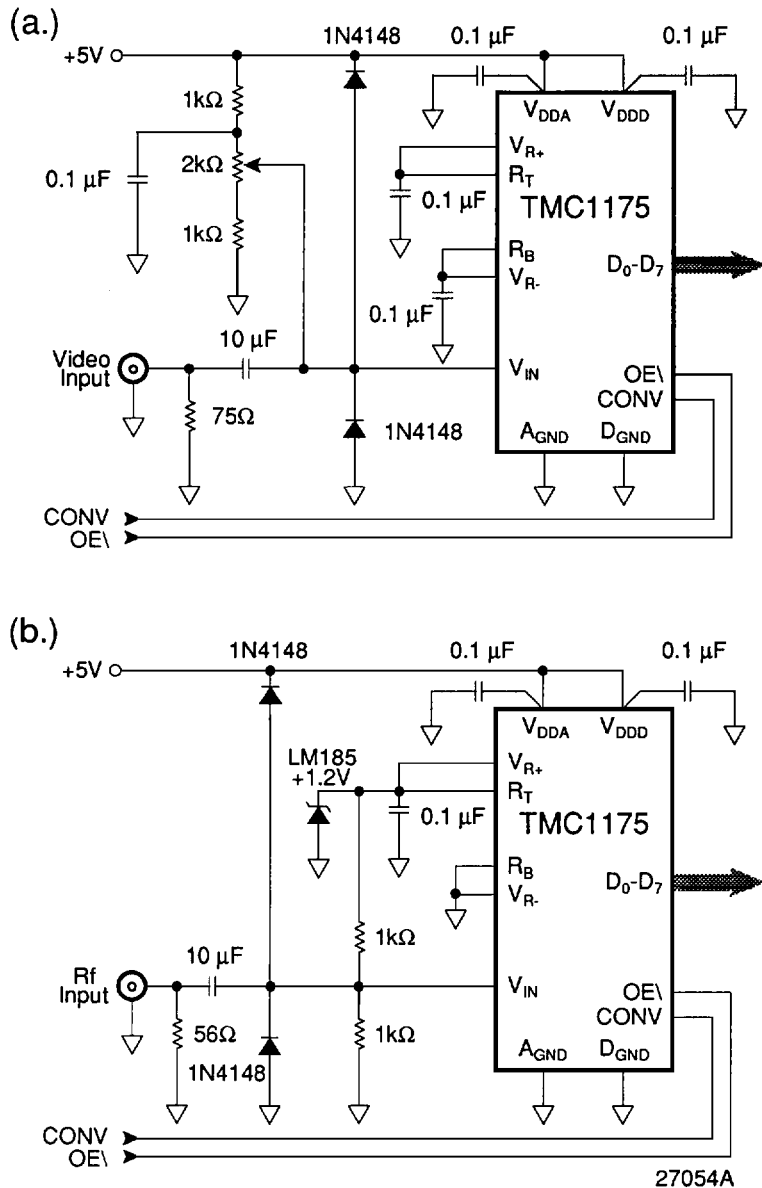
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Grounding

The TMC1175 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) come from the same source and ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

The digital circuitry that gets its input from the TMC1175 should be referred on the system digital ground plane.
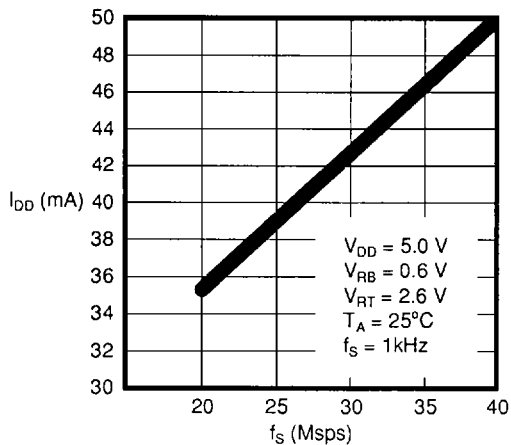
Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option, even for breadboarding. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:
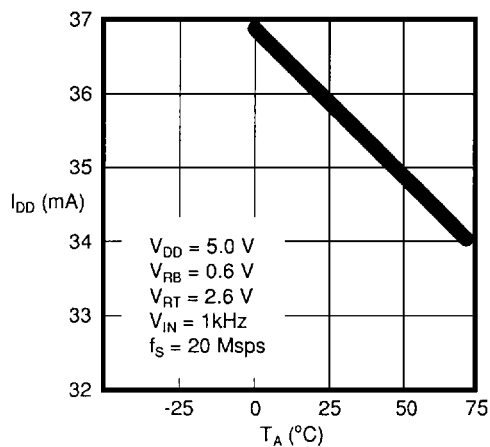
1. Keep the critical analog traces (V_{IN}, R_T, R_B, V_{R+}, V_{R-}) as short as possible and as far as possible from all digital signals. The TMC1175 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC1175 should be separate from that which supplies the rest of the digital circuitry. A single power plane

should be used for all of the V_{DD} pins. If the power supply for the TMC1175 is the same as that of the system's digital circuitry, power to the TMC1175 should be decoupled with ferrite beads and 0.1μF capacitors to reduce noise.

3. the ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power-supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1μF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC1175, the voltage reference or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1175 and its related analog circuitry can have an adverse effect on performance.

6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.
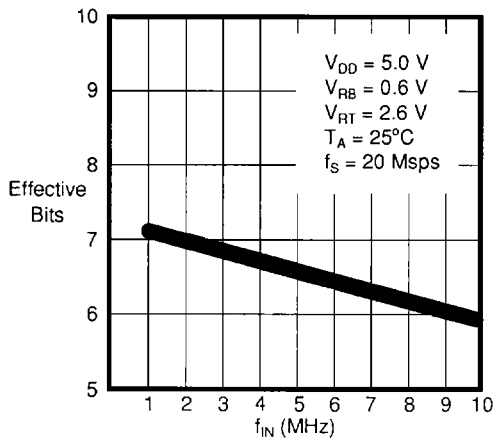
Typical Performance Curves
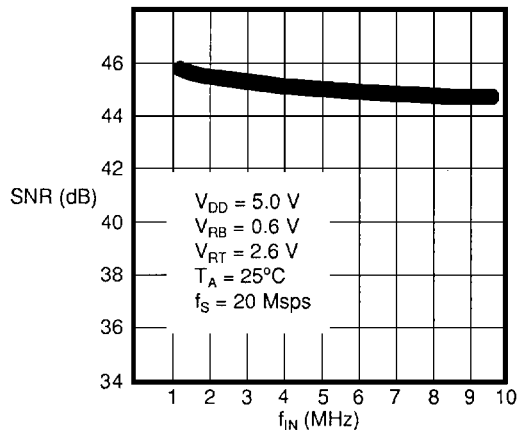
A. I_{DD} vs. f_S at 25°C

I_{DD} (mA)

$V_{DD} = 5.0$ V
$V_{RB} = 0.6$ V
$V_{RT} = 2.6$ V
$T_A = 25°C$
$f_S = 1kHz$

f_S (Msps)

B. I_{DD} vs. T_A at $f_S = 20$ Msps

I_{DD} (mA)

$V_{DD} = 5.0$ V
$V_{RB} = 0.6$ V
$V_{RT} = 2.6$ V
$V_{IN} = 1kHz$
$f_S = 20$ Msps

T_A (°C)

C. EFB vs. f_{IN}

Effective Bits

$V_{DD} = 5.0$ V
$V_{RB} = 0.6$ V
$V_{RT} = 2.6$ V
$T_A = 25°C$
$f_S = 20$ Msps

f_{IN} (MHz)

D. SNR vs. f_{IN}

SNR (dB)

$V_{DD} = 5.0$ V
$V_{RB} = 0.6$ V
$V_{RT} = 2.6$ V
$T_A = 25°C$
$f_S = 20$ Msps

f_{IN} (MHz)

27055A

TMC1175

Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC1175M7C20	20	T_A: -20°C to 75°C	Commercial	24-Lead SOIC	1175M7C20
TMC1175M7C30	30	T_A: -20°C to 75°C	Commercial	24-Lead SOIC	1175M7C30
TMC1175M7C40	40	T_A: -20°C to 75°C	Commercial	24-Lead SOIC	1175M7C40
TMC1175N2C20	20	T_A: -20°C to 75°C	Commercial	24-Pin Plastic DIP	1175N2C20
TMC1175N2C30	30	T_A: -20°C to 75°C	Commercial	24-Pin Plastic DIP	1175N2C30
TMC1175N2C40	40	T_A: -20°C to 75°C	Commercial	24-Pin Plastic DIP	1175N2C40
TMC1175R3C20	20	T_A: -20°C to 75°C	Commercial	28-Lead Plastic PLCC	1175R3C20
TMC1175R3C30	30	T_A: -20°C to 75°C	Commercial	28-Lead Plastic PLCC	1175R3C30
TMC1175R3C40	40	T_A: -20°C to 75°C	Commercial	28-Lead Plastic PLCC	1175R3C40
TMC1175B2F20	20	T_A: -55°C to 125°C	Commercial	24-Pin CERDIP	1175B2F20
TMC1175C3F20	20	T_A: -55°C to 125°C	Commercial	28-lead Ceramic LCC	1175C3F20
TMC1175E1C	30	T_A: -20°C to 75°C	Commercial	Eurocard PC Board	TMC1175E1C

Raytheon Semiconductor   For More Information call 1-800-722-7074.