

General Description

The AOZ8818 is a transient voltage suppressor array designed to protect high speed data lines from damaging ESD events.

This device incorporates 16 surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

The AOZ8818 provides a typical capacitance of 0.3 pF and low insertion loss up to 6GHz providing greater signal integrity, making it ideally suited for high speed data line applications such as Digital TVs, DVD players, Computing, set-top boxes and MDDI applications in mobile computing devices.

The AOZ8818 comes in a RoHS compliant and Halogen Free 2.5 mm x 1.0 mm x 0.55 mm DFN-10 package and is rated -40 °C to +85 °C junction temperature range.

Features

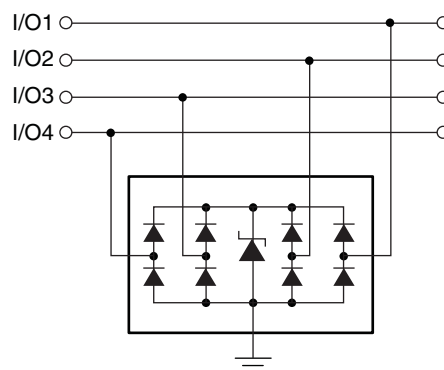
- ESD protection for high-speed data lines:
 - IEC61000-4-2, level 4 (ESD) immunity test
 - Air discharge: ±15 kV; contact discharge: ±15 kV
 - IEC61000-4-4 (EFT) 40A (5/50 ns)
 - IEC61000-4-5 (Lightning) 4 A (8/20 μs)
 - Human Body Model (HBM) ±24 kV
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects four I/O lines
- Low capacitance: 0.3 pF
- Low clamping voltage
- Low operating voltage: 3.3V, 5.0 V

Applications

- High speed serial ports
- Monitors and flat panel displays
- Set-top box
- Video graphics cards
- Digital Video Interface (DVI)
- Notebook computers



Typical Application



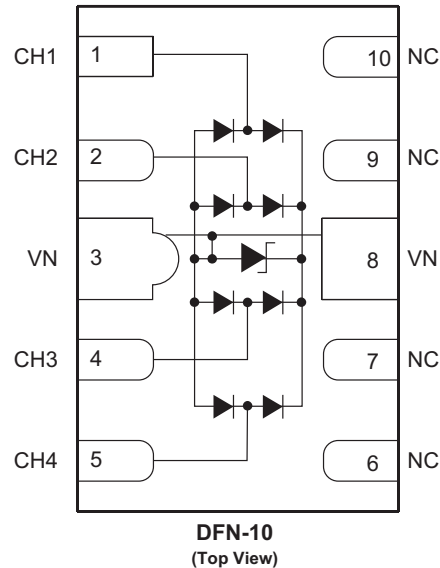
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8818DI-03	-40 °C to +85 °C	2.5 mm x 1.0 mm x 0.55 mm DFN-10	RoHS Compliant Green Product
AOZ8818DI-05			



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	AOZ8818DI-03	AOZ8818DI-05
Storage Temperature (T_S)	-65°C to +150°C	
ESD Rating per IEC61000-4-2, contact ⁽¹⁾	±15 kV	
ESD Rating per IEC61000-4-2, air ⁽¹⁾	±15 kV	
ESD Rating per Human Body Model ⁽²⁾	±24 kV	

Notes:

- IEC 61000-4-2 discharge with $C_{Discharge} = 150$ pF, $R_{Discharge} = 330$ Ω.
- Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge} = 100$ pF, $R_{Discharge} = 1.5$ kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40 °C to +125 °C

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to $+85^\circ\text{C}$.

Symbol	Parameter	Symbol	Parameter
I_{PP}	Maximum Reverse Peak Leakage Current	$V_{BR}^{(5)}$	Breakdown Voltage
$V_{CL}^{(3)}$	Clamping Voltage @ I_{PP}	I_T	Test Current
$V_{RWM}^{(4)}$	Working Peak Reverse Voltage	C_J	Max. Capacitance @ $V_R = 0$ and $f = 1$ MHz
I_R	Maximum Reverse Leakage Current		

Device	Device Marking	V_{RWM} (V) Max.	V_{BR} (V) Min. $I_T = 100 \mu\text{A}$	I_R (μA) Max.	V_{CL} Max.		C_J (pF)	
					$I_{PP} = 1$ A	$I_{PP} = 12$ A	Typ.	Max
AOZ8818DI-03	G	3.3	3.5	1.0	5	17.5	0.30	0.45
AOZ8818DI-05	E	5.0	6.0	1.0	6	18	0.30	0.45

Notes:

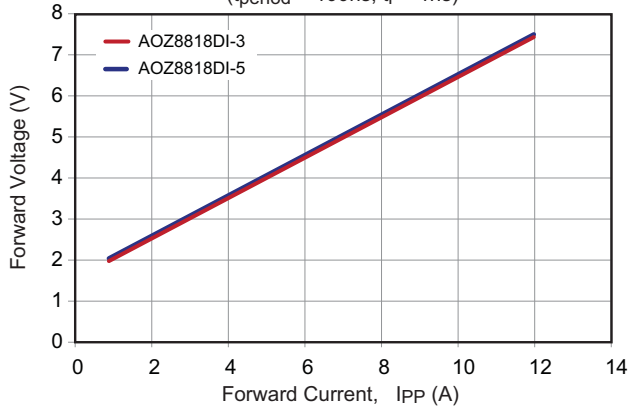
3. Measurements performed using a 100 ns Transmission Line Pulse (TLP) system.

4. The working peak reverse voltage, V_{RWM} , should be equal to or greater than the DC or continuous peak operating voltage level.

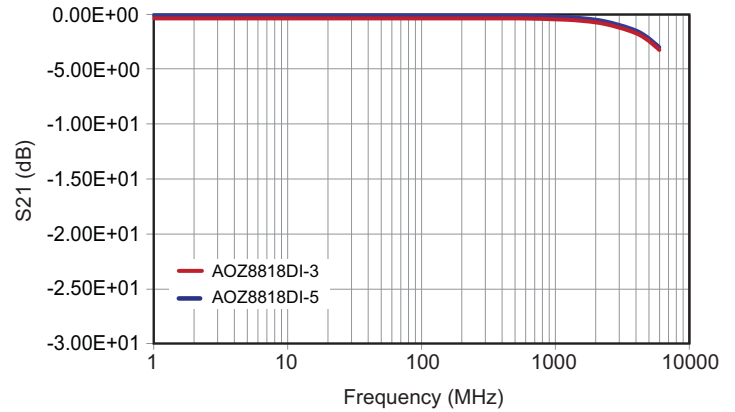
5. V_{BR} is measured at the pulse test current I_T .

Typical Performance Characteristics

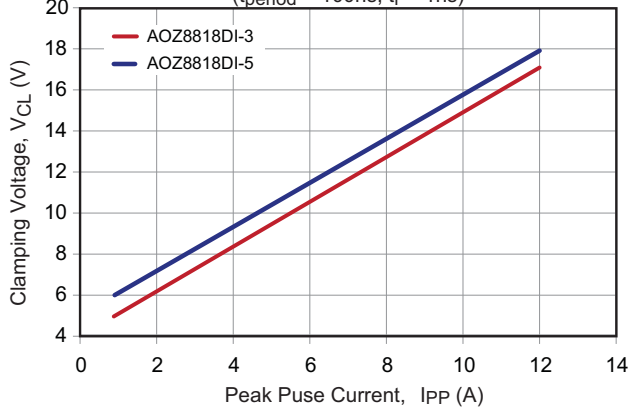
Forward Voltage vs. Forward Peak Pulse Current
($t_{period} = 100ns, t_r = 1ns$)



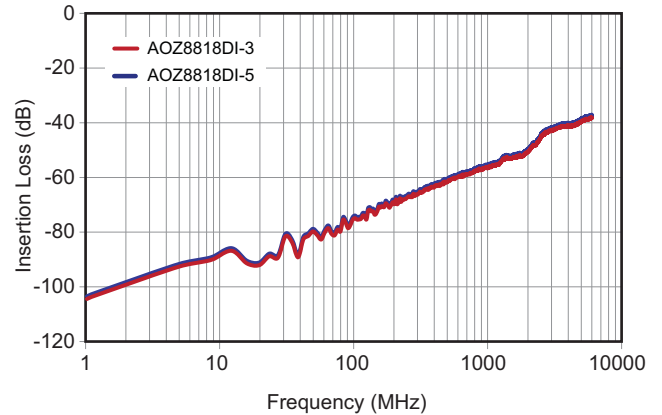
I/O – Gnd Insertion Loss (S21) vs. Frequency



Clamping Voltage vs. Peak Pulse Current
($t_{period} = 100ns, t_r = 1ns$)



Analog Crosstalk (I/O–I/O) vs. Frequency



High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8808DI devices should be located as close as possible to the noise source. The AOZ8808DI device should be placed on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8808DI devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8808DI device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground

PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The AOZ8808DI ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The AOZ8808DI is designed for ease of PCB layout by allowing the traces to run underneath the device. The pinout of the AOZ8808DI is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI) or USB 3.0 design without having to divert the signal lines that may add more parasitic inductance. Pins 1, 2, 4 and 5 are connected to the internal TVS devices and pins 6, 7, 9 and 10 are no connects. The no connects was done so the package can be securely soldered onto the PCB surface.

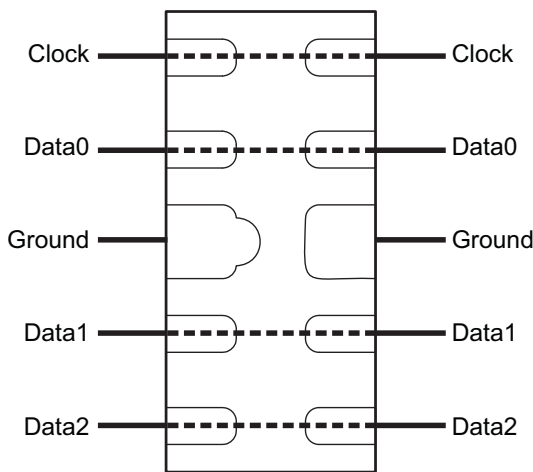


Figure 3. Flow Through Layout for HDMI

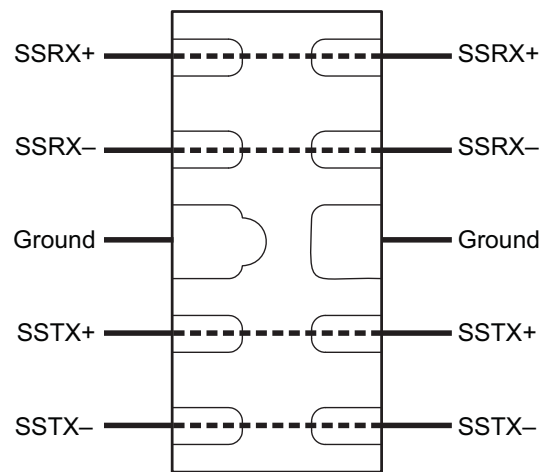
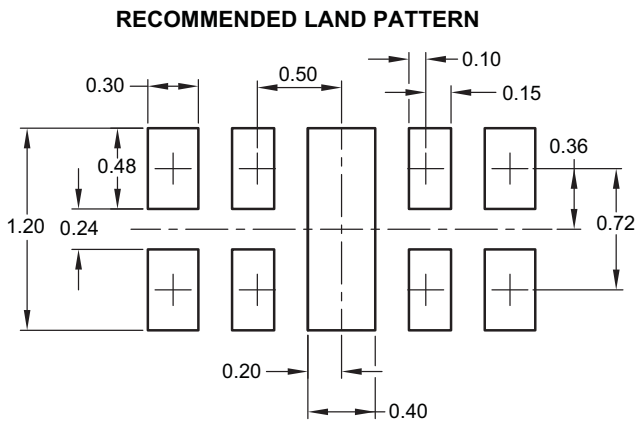
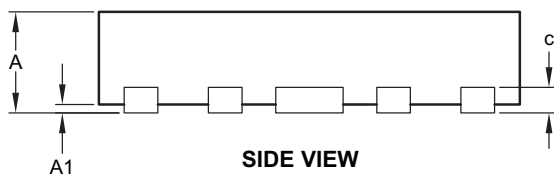
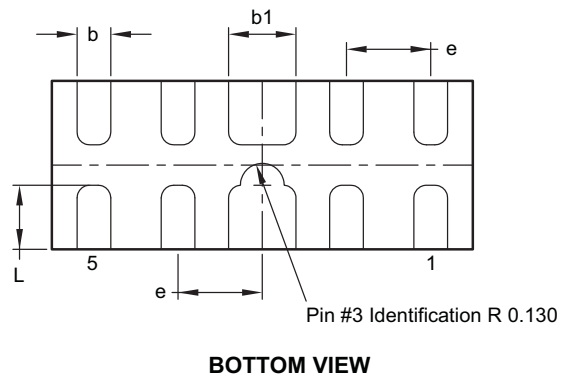
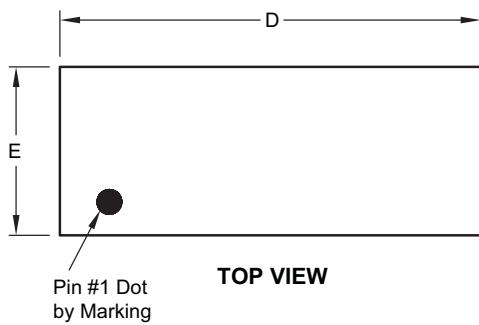


Figure 4. Flow Through Layout for USB 3.0

Package Dimensions, DFN 2.5mm x 1.0mm x 0.55mm, 10L



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	—	0.05
b	0.15	0.20	0.25
b1	0.40		
c	0.152 Ref.		
D	2.45	2.50	2.55
E	0.95	1.00	1.05
e	0.50 BSC		
L	0.33	0.38	0.43

Dimensions in inches

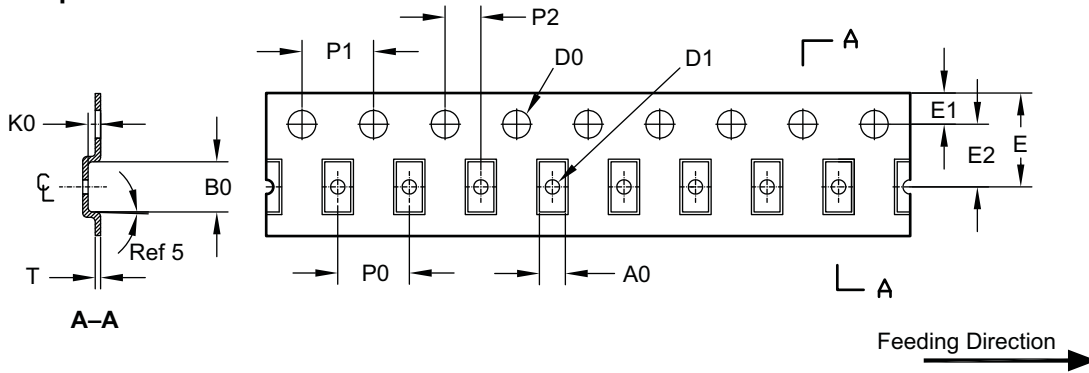
Symbols	Min.	Nom.	Max.
A	0.020	0.022	0.024
A1	0.000	—	0.002
b	0.006	0.008	0.010
b1	0.016		
c	0.006 Ref.		
D	0.096	0.098	0.100
E	0.037	0.039	0.041
e	0.020 BSC		
L	0.013	0.015	0.017

Note:

1. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, DFN 2.5mm x 1.0mm x 0.55mm, 10L

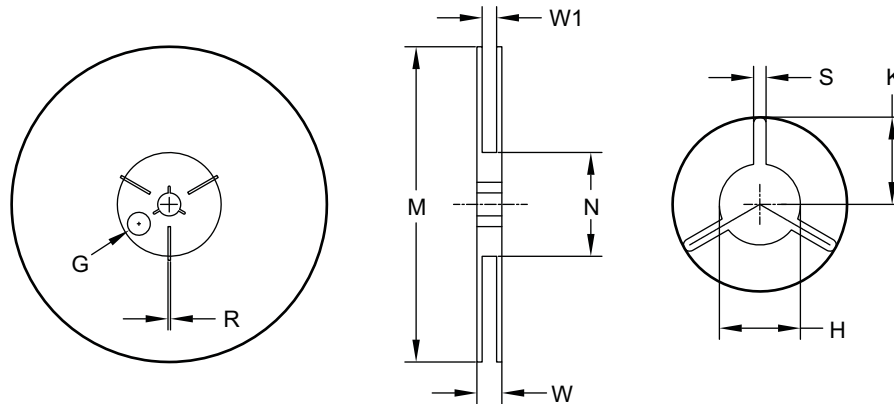
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 2.5x1.0	1.12 0.05	2.62 0.05	0.70 0.05	ø1.55 0.05	ø0.55 0.05	8.00 +0.3/-0.1	1.75 0.1	3.50 0.05	4.00 0.10	4.0 0.10	2.0 0.05	0.25 0.05

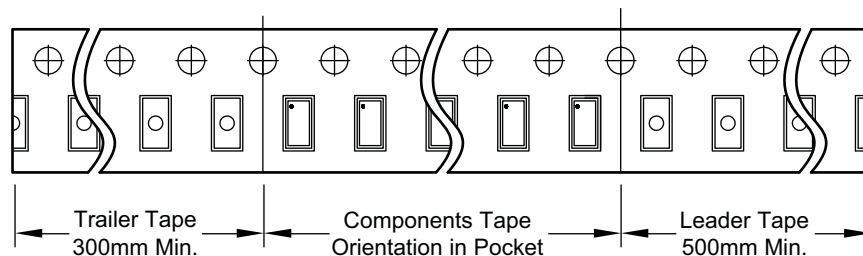
Reel



UNIT: mm

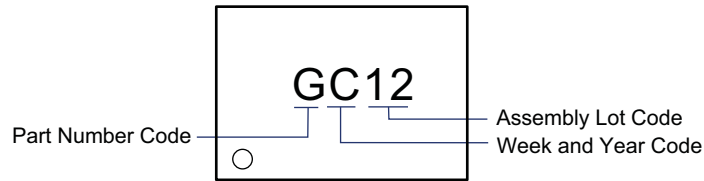
Tape Size	Reel Size	M	N	W	W1	H	S	K	E	R
8mm	ø178	ø178.0 1.0	ø60.0 0.5	11.80 0.5	9.0 0.5	ø13.0 +0.5 / -0.2	2.40 0.10	10.25 0.2	ø9.8	—

Leader / Trailer & Orientation

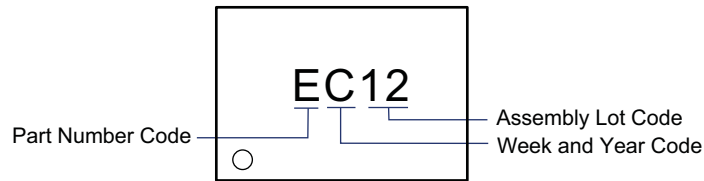


Part Marking

AOZ8818DI-03
(2.5 x 1.0 DFN)



AOZ8818DI-05
(2.5 x 1.0 DFN)



This datasheet contains preliminary data; supplementary data may be published at a later date. Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.