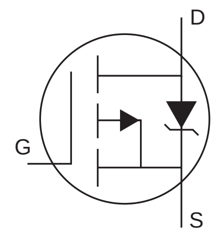
PD - 91402A

IRFR/U5305

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Surface Mount (IRFR5305)
- Straight Lead (IRFU5305)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = -55V

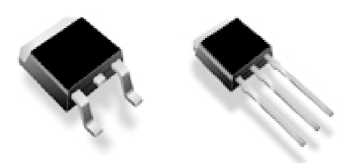
$R_{DS(on)}$ = 0.065Ω

I_D = -31A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



D-Pak IRFR5305 I-Pak IRFU5305

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-31	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-22	
I_{DM}	Pulsed Drain Current ①⑥	-110	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑥	280	mJ
I_{AR}	Avalanche Current①⑥	-16	A
E_{AR}	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	——	50	
$R_{\theta JA}$	Junction-to-Ambient**	——	110	

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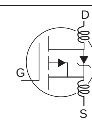
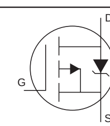
Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	——	——	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	-0.034	——	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.065	Ω	V_{GS} = -10V, I_D = -16A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	——	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	8.0	——	——	S	V_{DS} = -25V, I_D = -16A⑥
I_{DSS}	Drain-to-Source Leakage Current	——	——	-25	µA	V_{DS} = -55V, V_{GS} = 0V
		——	——	-250		V_{DS} = -44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	63	nC	I_D = -16A
Q_{gs}	Gate-to-Source Charge	——	——	13		V_{DS} = -44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	29		V_{GS} = -10V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	——	14	——	ns	V_{DD} = -28V
t_r	Rise Time	——	66	——		I_D = -16A
$t_{d(off)}$	Turn-Off Delay Time	——	39	——		R_G = 6.8Ω
t_f	Fall Time	——	63	——		R_D = 1.6Ω, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑤ 
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	1200	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	520	——		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	——	250	——		f = 1.0MHz, See Fig. 5 ⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	-31	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	-110		
V_{SD}	Diode Forward Voltage	——	——	-1.3	V	T_J = 25°C, I_S = -16A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	71	110	ns	T_J = 25°C, I_F = -16A
Q_{rr}	Reverse Recovery Charge	——	170	250	nC	di/dt = -100A/µs ④⑥

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② V_{DD} = -25V, starting T_J = 25°C, L = 2.1mH R_G = 25Ω, I_{AS} = -16A. (See Figure 12)

③ $I_{SD} \leq$ -16A, di/dt ≤ -280A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.

⑥ Uses IRF5305 data and test conditions.

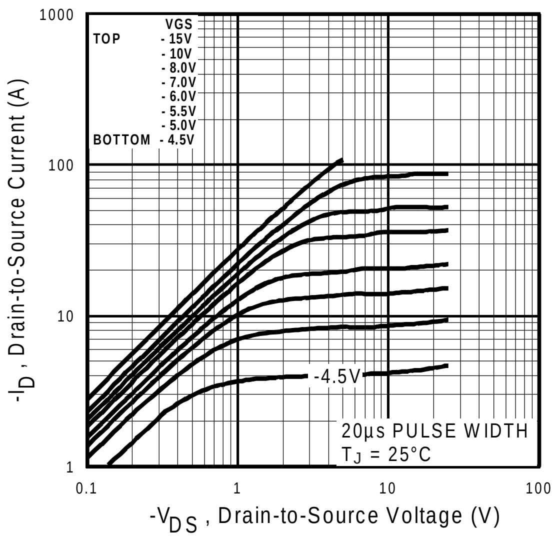


Fig 1. Typical Output Characteristics

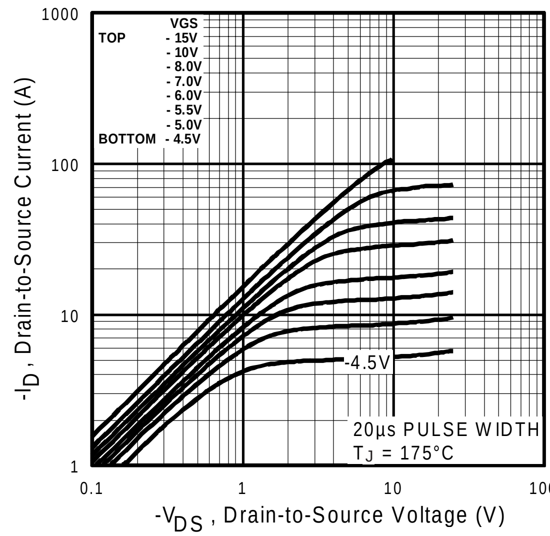


Fig 2. Typical Output Characteristics

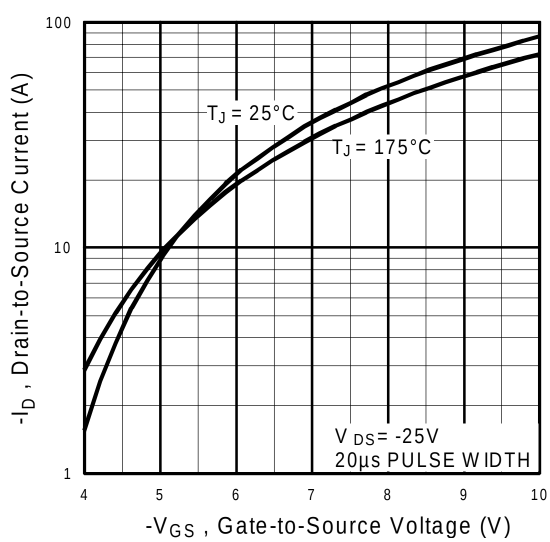


Fig 3. Typical Transfer Characteristics

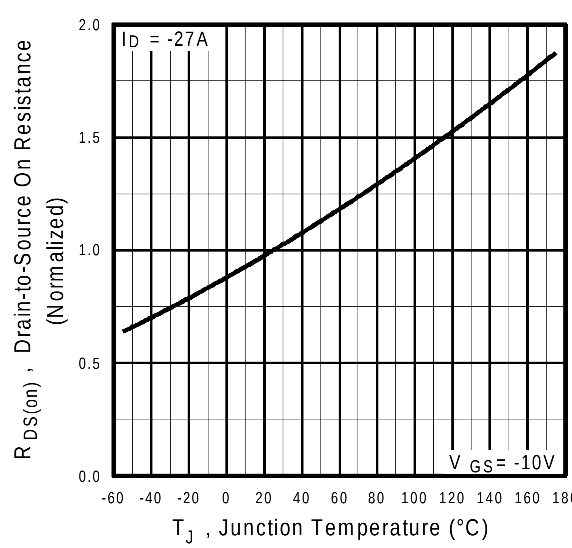


Fig 4. Normalized On-Resistance Vs. Temperature

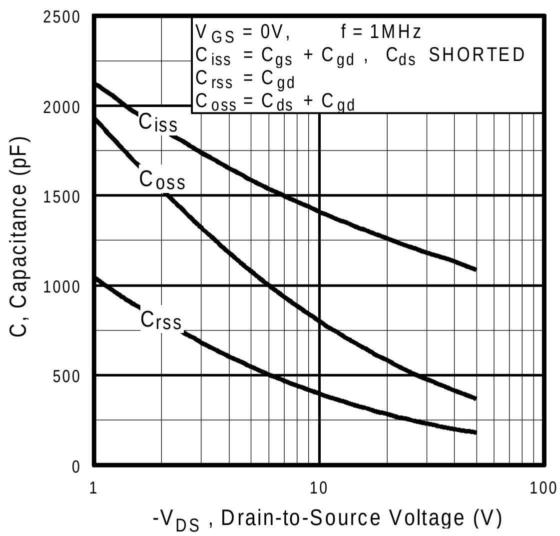


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

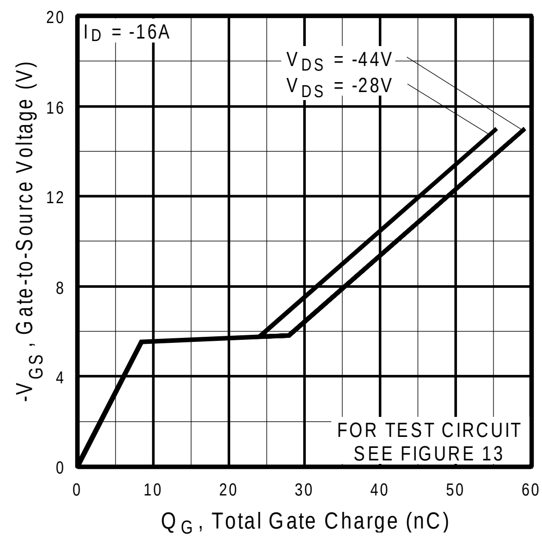


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

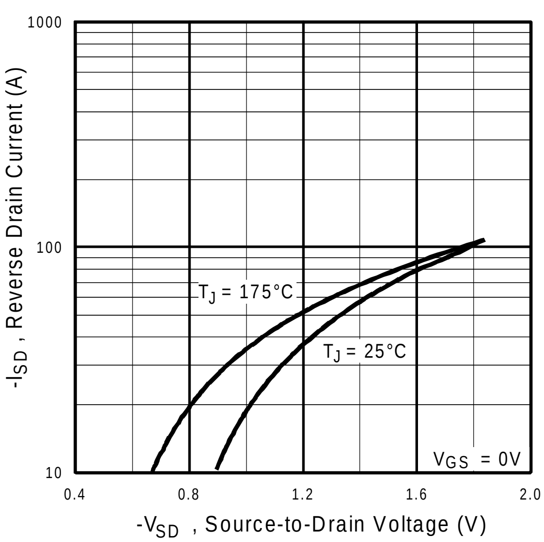


Fig 7. Typical Source-Drain Diode Forward Voltage

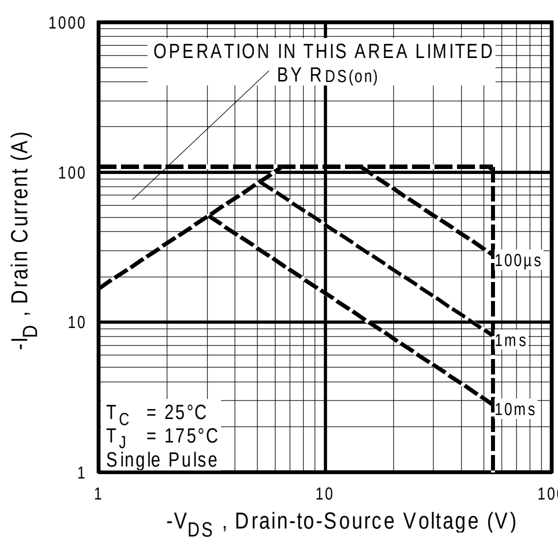


Fig 8. Maximum Safe Operating Area

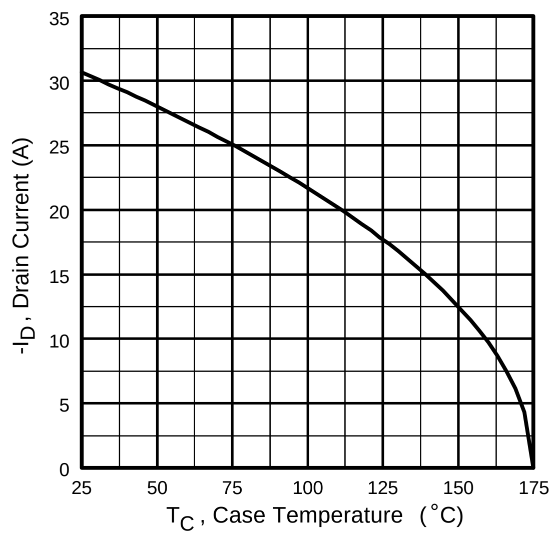


Fig 9. Maximum Drain Current Vs. Case Temperature

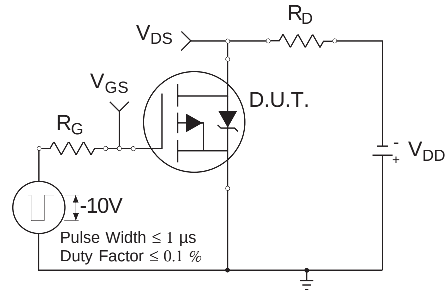


Fig 10a. Switching Time Test Circuit

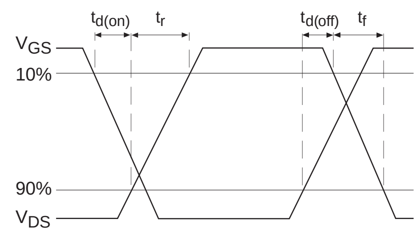


Fig 10b. Switching Time Waveforms

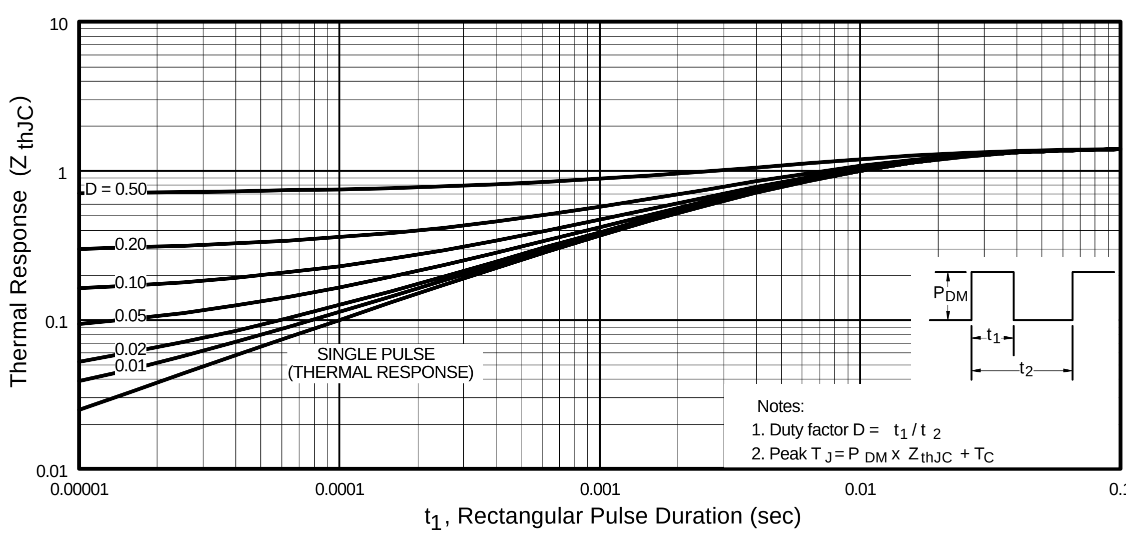


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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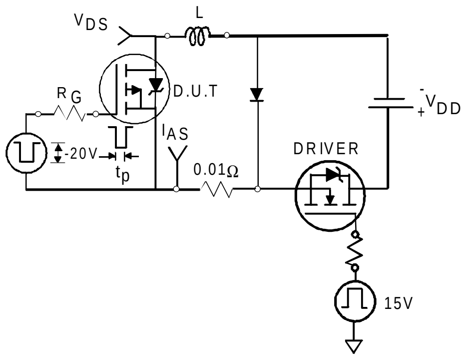


Fig 12a. Unclamped Inductive Test Circuit

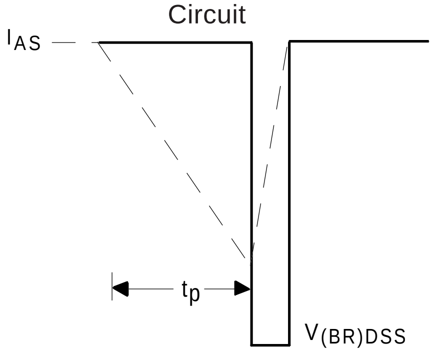


Fig 12b. Unclamped Inductive Waveforms

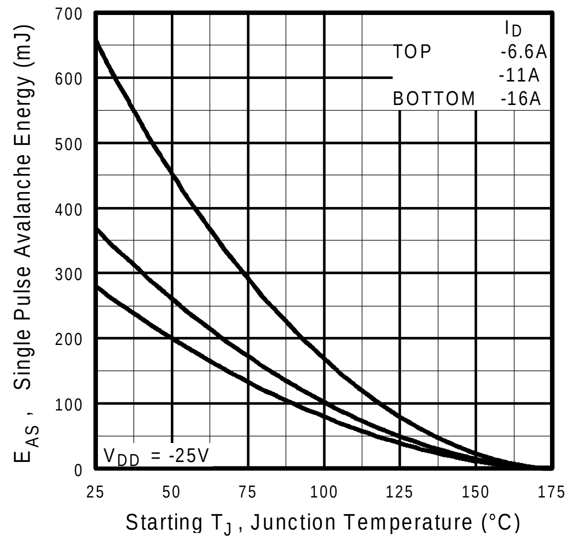


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

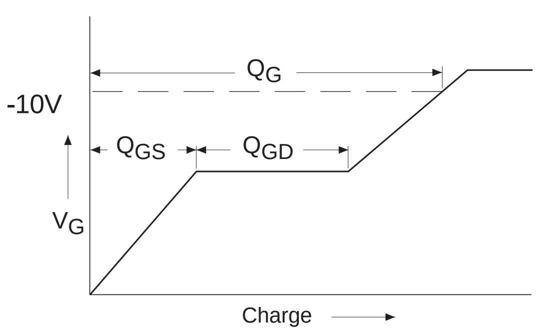


Fig 13a. Basic Gate Charge Waveform

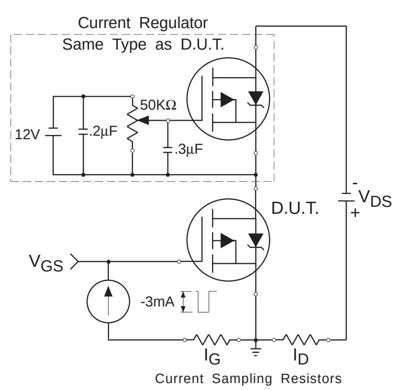
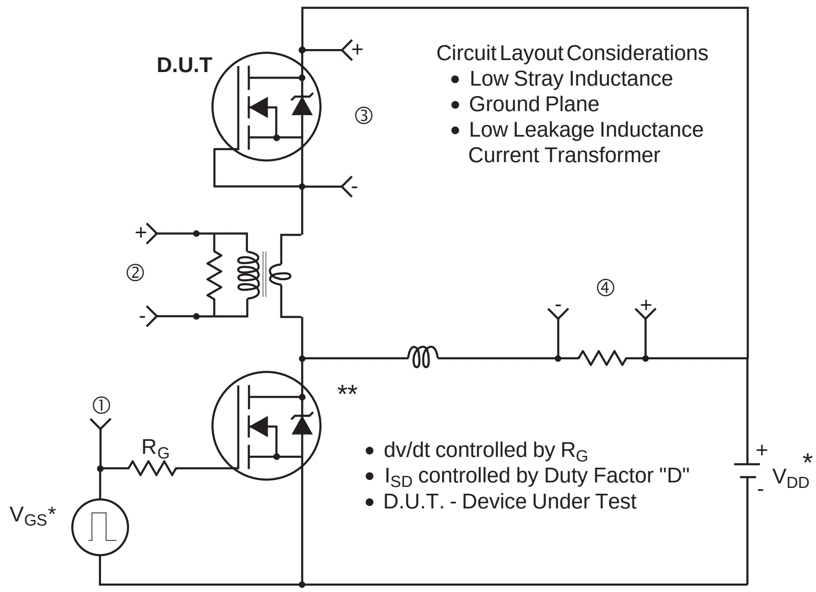
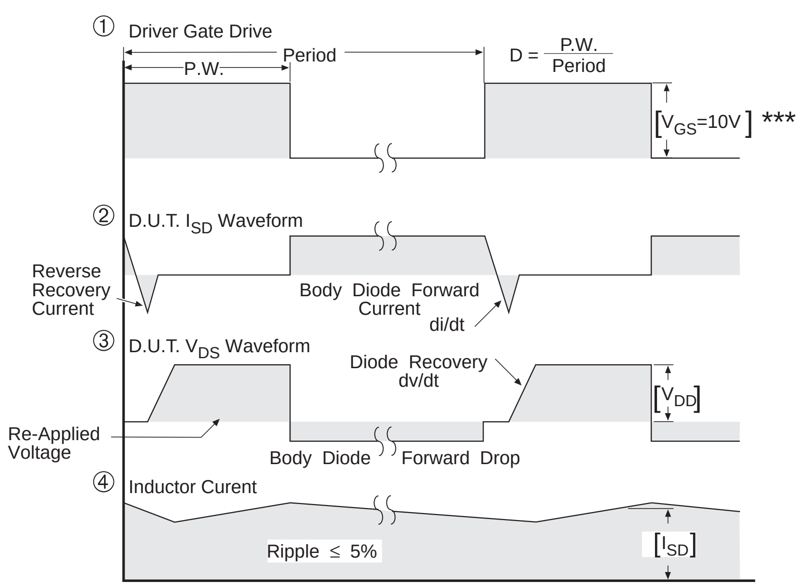


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

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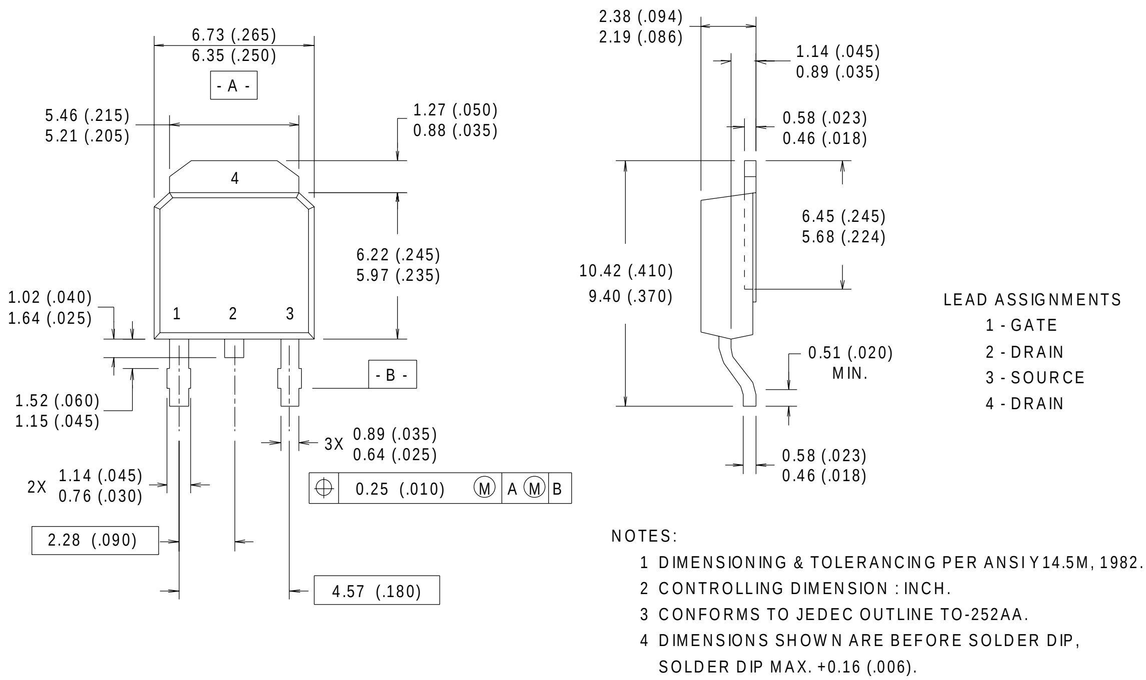
D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



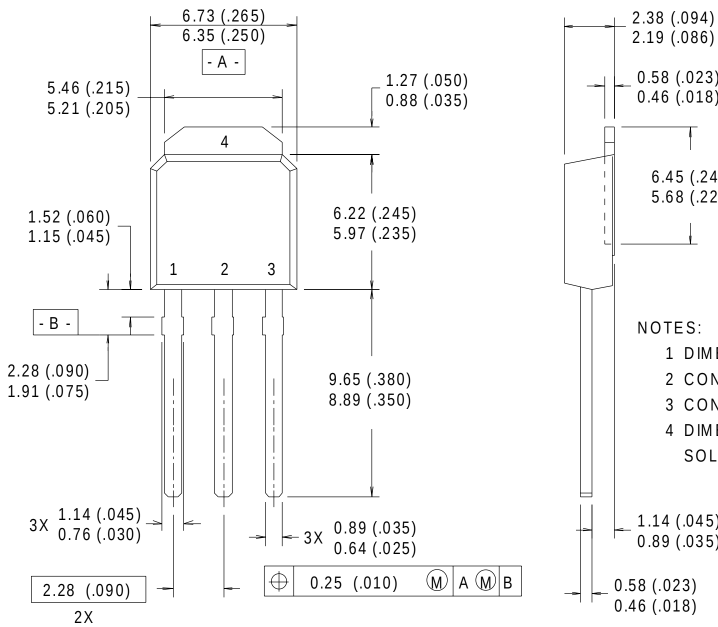
D-Pak (TO-252AA) Part Marking Information

KERSEMI

IRFR/U5305

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

I-Pak (TO-251AA) Part Marking Information

PLE: ¯HIS IS AN IRFU120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

INTERNATIONAL
RECTIFIER
LO

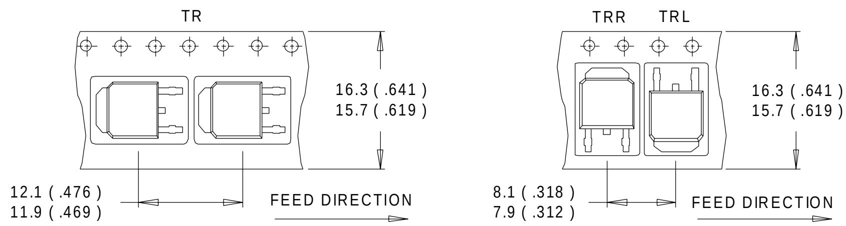
ASSEMBLY

OF PART NUMBER

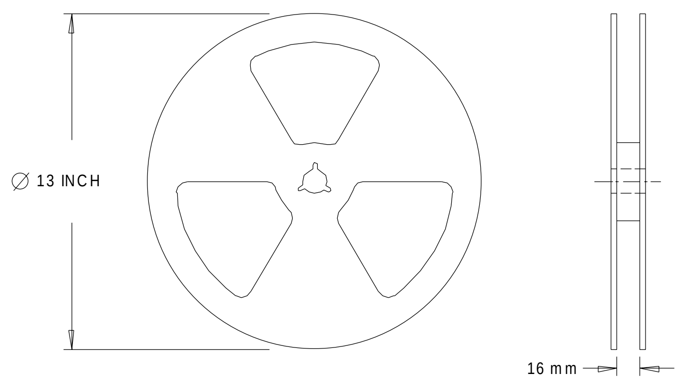
DATE CODE
YEAR 7 = 1997
WEEK 19
LINΓ

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.