T-73-43

Model LC-1010 Integrated Circuit



FEI Microwave's new integrated circuit, the LC-1010, is designed for use in a wide range of logarithmic amplifiers. It contains nine logging stages, biasing elements and an output amplifier capable of swings up to 6 volts.

(67.5 dB of RF range when used with detectors, due to the square law conversion characteristic). Each stage can have its bias current adjusted, thus allowing deviations from the square law in the detectors to be compensated.

Each stage can handle 15 dB of video signal, giving the chip the potential range of 135 dB

The adjustment ability can also be used to create transfer responses which are not logarithmic.

Brief Specifications

Logging Range: 18 mV to 560 mV for 2 sections

18 mV to 100 mV for 1 section

Total Range: 135 dB at Video

67.5 dB at RF (with no extension)
Estimated 75 dB with Linear Detector

signal used for extension

Available Output Swing: > 6 V (with a + 10 V supply)

Rise Time: <20 nS worst case at 6 V

<12 nS typical at 50 mV/dB

Power Supply: $< 10 \text{ mA at } \pm 8 \text{ V}$, excluding load current

Maximum voltage 20 V total with a minimum

of 5 V on either rail; does not have to be

symmetrical

Delay Time: <11 nS

Operating Temperature: -54 to +125°C

Package: 28 pin ceramic LCC

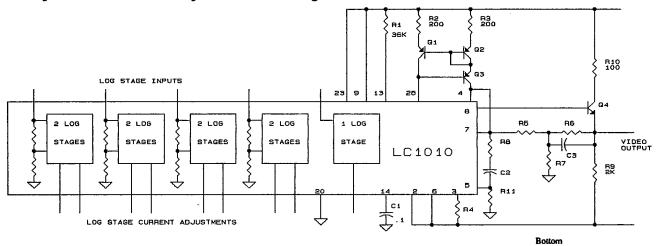
The block diagram found on the following page, shows the LC-1010 and its external components. The inputs are fed to the internal log stages which are of the standard parallel summed differential pair type. These give good linearity, coupled with high speed. Internal dividers are supplied for the two-stage sections.

The current output from the log stages is fed to a PNP current mirror, Q1, Q2, and Q3, which drives the output amplifier. Q4 is the actual output transistor and is external in order to reduce the power dissipation in the chip.

Other parts are used as described below:

R1	Sets all of the log stages at a fixed slope	C3	Frequency compensation of the output amplifier
R2, R3	Help keep the mirror balanced	C1	Compensates the internal bias
R4	Sets the output DC offset		generator
R5, R6, & R	7 Set the output slope	R10	Short circuit protection
R8 & C2	Frequency compensation of the		-
	output amplifier		

In addition, the slope of each individual stage can be adjusted with a resistor to the appropriate set point. A resistor to - V power will increase the slope while a resistor to ground will decrease it.

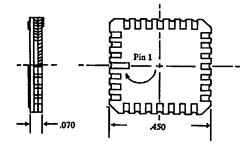


Pin Number Allocations for the 28 Lead LCC

P	in
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Number Description

- 1 Current Adjust for Log Stage 5
- 2 Negative Power Supply for Log Stages
- 3 Output Offset Adjust
- 4 Current to Cancel that from the PNP Mirror and balance the output
- 5 Output Amp Positive Input
- 6 Negative Power Supply for Output Stage
- 7 Output Amp Negative Input
- 8 Drive to External Output Transistor
- 9 Positive Power Supply
- 10 Output Short Circuit Protection
- 11 Log Stage 9 Input
- 12 Current Adjust for Log Stage 9
- 13 Current Adjust for All Log Stages Together
- 14 Decoupling for Bias Generator
- 15 Current Adjust for Log Stage 4
- 16 Current Adjust for Log Stage 3



- Number Description
- 17 Current Adjust for Log Stage 1
- 18 Current Adjust for Log Stage 2
- 19 Log Stage 1 and 2 Input
- 20 Ground

Pin

- 21 Log Stage 3 and 4 Input
- 22 Log Stage 5 and 6 Input
- 23 Log Stage OP (normally + V Power Rail)
- 24 Log Stage 7 and 8 Input
- 25 Log Stage Output to Mirror
- 26 Current Adjust for Log Stage 7
- 27 Current Adjust for Log Stage 8
- 28 Current Adjust for Log Stage 6



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