PR5331C3HN

Contactless Interface Controller

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206430

Product short data sheet
PUBLIC

1. General description

The PR5331C3HN is a highly integrated transceiver module for contactless reader/writer communication at 13.56 MHz.

A dedicated ROM code is implemented to handle different RF protocols by an integrated microcontroller. The system host controller communicates with the PR5331C3HN by using the USB or the HSU link.

The protocol between the host controller and the PR5331C3HN, on top of this physical link is the CCID protocol.

1.1 RF protocols

PR5331C3HN supports the PCD mode for FeliCa (212 kbps and 424 kbps), ISO/IEC14443 Type A and B (from 106 kbps to 847 kbps), MIFARE (106 kbps), B' cards (106 kbps), picoPass tag (106 kBps) and Innovision Jewel cards (106 kbps)

The Initiator passive mode (from 106 kbps to 424 kbps) can be supported through the PC/SC transparent mode.

1.2 Interfaces

The PR5331C3HN supports USB 2.0 full speed interface (bus powered or host powered mode).

PR5331C3HN has also a master I^2C-bus interface enabling the drive of following peripherals:

- An external EEPROM: in this case the PR5331C3HN is configured as master and is able to communicate with external EEPROM (address A0h) which can store configuration data like PID, UID and RF parameters
- A TDA8029 contact smart card reader
- High Speed UART (from 9600b up to 1.2 Mb)

1.3 Standards compliancy

PR5331C3HN offers commands in order for applications to be compliant with “EMV Contactless Communication Protocol Specification V2.0.1”.

PR5331C3HN supports RF protocols ISO/IEC 14443A and B such as compliancy with Smart eID standard can be achieved at application level.

Support of USB 2.0 full speed, interoperable with USB 3.0 hubs

The PR533C3HN in PCD mode is compliant with EMV contactlesss specification V2.0.1.

1.4 Supported operating systems

- Microsoft Windows 2000
- Microsoft Windows XP (32 and 64 bits)
- Microsoft Windows 2003 Server (32 and 64 bits)
- Microsoft Windows 2008 Server (32 and 64 bits)
- Microsoft Windows Vista (32 and 64 bits)
- Microsoft Windows 7 (32 and 64 bits)

The PR533 is supported by the following OS through the PCSC-Lite driver:

- GNU/Linux using libusb 1.0.x and later
- Mac OS Leopard (1.5.6 and newer)
- Mac OS Snow Leopard (1.6.X)
- Solaris
- FreeBSD

2. Features and benefits

- USB 2.0 full speed host interface and CCID protocol support
- Integrated microcontroller implements high-level RF protocols
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated data mode detector
- Supports ISO/IEC 14443A Reader/Writer mode up to 848 kbit/s
- Supports ISO/IEC 14443B Reader/Writer mode up to 848 kbit/s
- Supports contactless communication according to the FeliCa protocol at 212 kbit/s and 424 kbit/s
- Supports MIFARE encryption
- Typical operating distance in Read/Write mode for communication to ISO/IEC 14443A/MIFARE, ISO/IEC 14443B or FeliCa cards up to 50 mm depending on antenna size and tuning
- I^2C-bus master interface allows to connect an external I^2C EEPROM for configuration data storage or to control a TDA8029 contact smart card reader
- Low power modes
  - Hard power-down mode
  - Soft power-down mode
- Only one external oscillator required (27.12 MHz Crystal oscillator)
- Power modes
  - USB bus power mode
  - 2.5 V to 3.6 V power supply operating range in non USB bus power mode
- Dedicated I/O ports for external device control

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3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BUS}	bus supply voltage			4.02	5	5.25	V
		(non USB mode); $V_{BUS} = V_{DDD}$; $V_{SSD} = 0$ V		2.5	3.3	3.6	V
V_{DDA}	analog supply voltage	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage		[1]	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage		[1]	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage			1.6	-	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V; reserved for future use		V_{DDD} −0.1	-	V_{DDD}	V
I_{BUS}	bus supply current	maximum load current (USB mode); measured on V_{BUS}				150	mA
		maximum inrush current limitation; at power-up (curlimoff = 0)				100	mA
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V; not powered from USB					
		hard power-down; RF level detector off				10	µA
		soft power-down; RF level detector on				30	µA
I_{CCSL}	suspended low-power device supply current	RF level detector on, (without resistor on DP/DM)		-	-	250	µA
I_{DDD}	digital supply current	RF level detector on, $V_{DD(SVDD)}$ switch off	[1]	-	15	-	mA
$I_{DD(SVDD)}$	SVDD supply current	$V_{DDS} = 3$ V		-	-	30	mA
I_{DDA}	analog supply current	RF level detector on		-	6	-	mA
$I_{DD(TVDD)}$	TVDD supply current	during RF transmission; $V_{DD(TVDD)} = 3$ V		-	60	100	mA
P_{tot}	total power dissipation	$T_{amb} = -30$ to +85 °C		-	-	0.55	W
T_{amb}	ambient temperature			−30	-	+85	°C

[1] V_{DDD}, V_{DDA} and $V_{DD(TVDD)}$ must always be at the same supply voltage.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PR5331C3HN/C350[1][2][3]	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm	SOT618-1

[1] 70 refers to the ROM code version described in the User Manual.

[2] Refer to Section 14.4 “Licenses”.

[3] MSL 2 (Moisture Sensitivity Level).

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5. Block diagram

The following block diagram describes hardware blocks controlled by PR5331C3HN firmware or which can be accessible for data transaction by a host baseband.

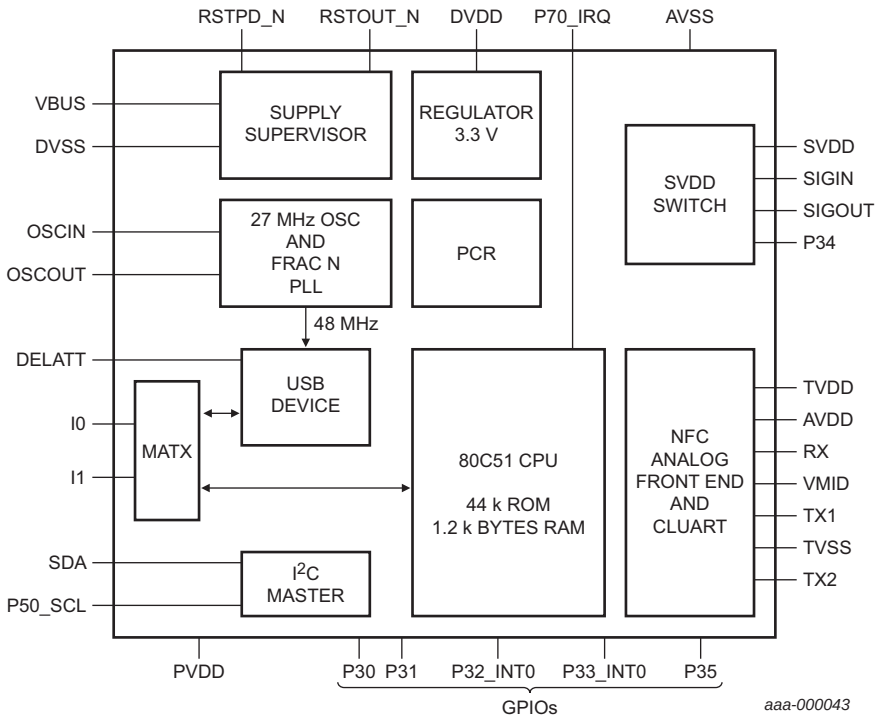

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

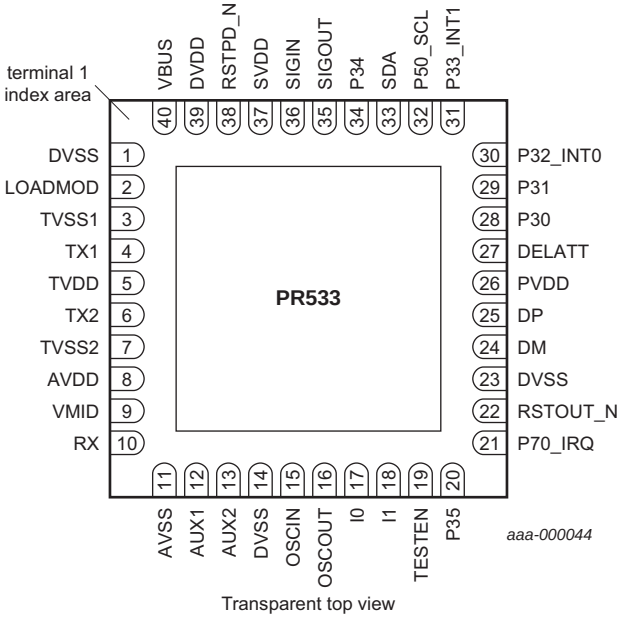

Fig 2. Pin configuration for HVQFN 40 (SOT618-1)

6.2 Pin description

Table 3. PR533 Pin description

Symbol	Pin	Type	Pad ref voltage	Description
DVSS	1	G		digital ground
LOADMOD	2	O	DVDD	load modulation output provides digital signal for FeliCa and MIFARE card operating mode
TVSS1	3	G		transmitter ground: supplies the output stage of TX1
TX1	4	O	TVDD	transmitter 1: transmits modulated 13.56 MHz energy carrier
TVDD	5	P		transmitter power supply: supplies the output stage of TX1 and TX2
TX2	6	O	TVDD	transmitter 2: delivers the modulated 13.56 MHz energy carrier
TVSS2	7	G		transmitter ground: supplies the output stage of TX2
AVDD	8	P		analog power supply
VMID	9	P	AVDD	internal reference voltage: This pin delivers the internal reference voltage.
RX	10	I	AVDD	receiver input: Input pin for the reception signal, which is the load modulated 13.56 MHz energy carrier from the antenna circuit
AVSS	11	G		analog ground
AUX1	12	O	DVDD	auxiliary output 1: This pin delivers analog and digital test signals
AUX2	13	O	DVDD	auxiliary output 2: This pin delivers analog and digital test signals
DVSS	14	G		digital ground

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Table 3. PR533 Pin description *…continued*

Symbol	Pin	Type	Pad ref voltage	Description
OSCIN	15	I	AVDD	crystal oscillator input: input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{clk} = 27.12 MHz).
OSCOUT	16	O	AVDD	crystal oscillator output: output of the inverting amplifier of the oscillator.
I0	17	I	DVDD	interface mode lines: selects the used host interface; in test mode I0 is used as test signals.
I1	18	I	DVDD	
TESTEN	19	I	DVDD	test enable pin: when set to 1 enable the test mode. when set to 0 reset the TCB and disable the access to the test mode.
P35	20	I/O	DVDD	general purpose I/O signal
P70_IRQ	21	I/O	PVDD	interrupt request: output to signal an interrupt event to the host (Port 7 bit 0)
RSTOUT_N	22	O	PVDD	output reset signal; when LOW it indicates that the circuit is in reset state.
DVSS	23	G		digital ground
DM	24	I/O	PVDD	USB D– data line in USB mode or TX in HSU mode; in test mode this signal is used as input and output test signal
DP	25	I/O	PVDD	USB D+ data line in USB mode or RX in HSU mode; in test mode this signal is used as input and output test signal.
PVDD	26	P		I/O pad power supply
DELATT	27	O	PVDD	optional output for an external 1.5 kΩ resistor connection on D+.
P30	28	I/O	PVDD	general purpose I/O signal. Can be configured to act either as RX line of the second serial interface UART or general purpose I/O. In test mode this signal is used as input and output test signal.
P31	29	I/O	PVDD	general purpose I/O signal. Can be configured to act either as TX line of the second serial interface UART or general purpose I/O. In test mode this signal is used as input and output test signal.
P32_INT0	30	I/O	PVDD	general purpose I/O signal. Can also be used as an interrupt source In test mode this signal is used as input and output test signal.
P33_INT1	31	I/O	PVDD	general purpose I/O signal. Can be used to generate an HZ state on the output of the selected interface for the Host communication and to enter into power-down mode without resetting the internal state of PR533. In test mode this signal is used as input and output test signal.
P50_SCL	32	I/O	DVDD	I^2C-bus clock line - open-drain in output mode
SDA	33	I/O	DVDD	I^2C-bus data line - open-drain in output mode
P34	34	I/O	SVDD	general purpose I/O signal or clock signal for the SAM
SIGOUT	35	O	SVDD	contactless communication interface output: delivers a serial data stream according to NFCIP-1 and output signal for the SAM. In test mode this signal is used as test signal output.
SIGIN	36	I	SVDD	contactless communication interface input: accepts a digital, serial data stream according to NFCIP-1 and input signal from the SAM. In test mode this signal is used as test signal input.
SVDD	37	P		output power for SAM power supply. Switched on by Firmware with an overload detection. Used as a reference voltage for SAM communication.

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Table 3. PR533 Pin description *…continued*

Symbol	Pin	Type	Pad ref voltage	Description
RSTPD_N	38	I	PVDD	reset and power-down: When LOW, internal current sources are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a negative edge on this pin the internal reset phase starts.
DVDD	39	P		digital power supply
VBUS	40	P		USB power supply.

[1] Pin types: I= Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA}	analog supply voltage			−0.5	+4	V
V_{DDD}	digital supply voltage			−0.5	+4	V
$V_{DD(TVDD)}$	TVDD supply voltage			−0.5	+4	V
$V_{DD(PVDD)}$	PVDD supply voltage			−0.5	+4	V
$V_{DD(SVDD)}$	SVDD supply voltage			−0.5	+4	V
V_{BUS}	bus supply voltage			−0.5	+5.5	V
P_{tot}	total power dissipation			-	500	mW
$I_{DD(SVDD)}$	SVDD supply current	maximum current in V_{DDS} switch		-	30	mA
V_i	input voltage	TX1, TX2, RX pins		−0.5	+4	V
V_{ESD}	electrostatic discharge voltage	HBM	[1]		±2.0	kV
		MM	[2]	-	200	V
		CDM	[3]	-	±1	kV
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+125	°C

[1] 1500 Ω, 100 pF; EIA/JESD22-A114-A

[2] 0.75 mH, 200 pF; EIA/JESD22-A115-A

[3] Field induced model; EIA/JESC22-C101-C

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BUS}	bus supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		4.02	5	5.25	V
		supply voltage (non USB mode); $V_{BUS} = V_{DDD}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		2.5	3.3	3.6	V
V_{DDA}	analog supply voltage	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V

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Table 5. Operating conditions *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDD}	digital supply voltage	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage	supply pad for host interface; $V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[2]	1.6	1.8 to 3.3	3.6	V
T_{amb}	ambient temperature			−30	+25	+85	°C

[1] V_{SSA}, V_{DDD} and $V_{DD(TVDD)}$ shall always be on the same voltage level.

[2] Supply voltages below 3 V reduces the performance (e.g. the achievable operating distance).

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer Jedec PCB-0.5	-	37	41.1	K/W

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10. Characteristics

Unless otherwise specified, the limits are given for the full operating conditions. The typical value is given for 25 °C, V_{DDD} = 3.4 V and $V_{DD(PVDD)}$ = 3 V in non-USB bus power mode, V_{BUS} = 5 V in USB power mode.

Timings are only given from characterization results.

10.1 Power management characteristics

10.1.1 Current consumption characteristics

Typical value using a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz.

Table 7. Current consumption characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$ = 3 V; not powered from USB					
		hard power-down current; not powered from USB; RF level detector off	[1]	-	1.3	10	µA
		soft power-down current; not powered from USB; RF level detector on	[1]	-	9	30	µA
I_{CCSL}	suspended low-power device supply current	V_{BUS} = 5 V; $V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$ = 3 V; V_{DDS} = 0 V; RF level detector on (without resistor on pin DP (D+))	[1]	-	120	250	µA
I_{DDD}	digital supply current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$ = 3 V; RF level detector on		-	12	-	mA
I_{DDA}	analog supply current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$ = 3 V;					
		RF level detector on		-	3	6	mA
		RF level detector off		-	1.5	5	mA
$I_{DD(PVDD)}$	PVDD supply current		[2]	-	-	30	mA
$I_{DD(SVDD)}$	SVDD supply current	sam_switch_en set to 1	[3]	-	-	30	mA
$I_{DD(TVDD)}$	TVDD supply current	continuous wave; $V_{DD(TVDD)}$ = 3 V	[4][5]	-	60	100	mA

[1] I_{pd} is the total currents over all supplies.

[2] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[3] $I_{DD(SVDD)}$ depends on the overall load on $V_{DD(SVDD)}$ pad.

[4] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuitry connected to TX1 and TX2.

[5] During operation with a typical circuitry the overall current is below 100 mA.

10.1.2 Voltage regulator characteristics

Table 8. Voltage regulator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BUS}	bus supply voltage	USB mode; V_{SS} = 0 V	4.02	5	5.25	V
V_{DDD}	digital supply voltage	after inrush current limitation (USB mode); from I_{VDDD} = 0 mA to I_{VDDD} = 150 mA	2.95	3.3	3.6	V
I_{BUS}	bus supply current	USB mode; measure on V_{BUS}	-	-	150	mA

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Table 8. Voltage regulator characteristics[1] …continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{inrush(lim)}$	inrush current limit	at power-up (curlimofff = 0)	-	-	100	mA
$V_{th(rst)reg}$	regulator reset threshold voltage	regulator reset	1.90	2.15	2.40	V
$V_{th(rst)reg(hys)}$	regulator reset threshold voltage hysteresis		35	60	85	mV
	V_{DDD} decoupling capacitor		8	10	-	µF

[1] The internal regulator is only enabled when the USB interface is selected by I0 and I1.

10.2 Antenna presence self test thresholds

The values in Table 9 are guaranteed by design. Only functional is done in production for cases andet_ithl[1:0]=10b and for andet_ithh[2:0]=011b.

Table 9. Antenna presence detection

Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDD} lower current threshold for antenna presence detection					
andet_ithl[1:0]	00b	-	5	-	mA
	01b	-	15	-	mA
	10b	-	25	-	mA
	11b	-	35	-	mA
I_{VDDD} upper current threshold for antenna presence detection					
andet_ithh[2:0]	000b	-	45	-	mA
	001b	-	60	-	mA
	010b	-	75	-	mA
	011b	-	90	-	mA
	100b	-	105	-	mA
	101b	-	120	-	mA
	110b	-	135	-	mA
	111b	-	150	-	mA

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10.3 Typical 27.12 MHz Crystal requirements

Table 10. Crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency		27.107	27.12	27.133	MHz
ESR	equivalent series resistance		-	-	100	Ω
C_L	load capacitance		-	10	-	pF
P_{xtal}	crystal power dissipation		100	-	-	μW

10.4 Pin characteristics for 27.12 MHz XTAL Oscillator (OSCIN, OSCOUT)

Table 11. Pin characteristics for 27.12 MHz XTAL Oscillator (OSCIN, OSCOUT)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LI}	input leakage current	RSTPD_N = 0 V		−1	-	+1	mA
V_{IH}	HIGH-level input voltage			0.7 × V_{DDA}	-	V_{DDA}	V
V_{IL}	LOW-level input voltage			0	-	0.3 × V_{DDA}	V
V_{OH}	HIGH-level output voltage			-	1.1	-	V
V_{OL}	LOW-level output voltage			-	0.2	-	V
f_{clk}	clock frequency			−0.05 %	27.12	+0.05 %	MHz
δ	duty cycle			40	50	60	%
$\varphi_{n(th)}$	phase noise threshold		[1]	-	-	−140	dBc/Hz
$f_{\varphi n(th)}$	phase noise threshold frequency	$\varphi_{n(th)}$ = −140dBc/Hz; −20dB/decade slope	[1]	-	-	50	kHz
OSCIN							
V_i	input voltage	DC		-	0.65	-	V
C_i	input capacitance	V_{DDA} = 2.8 V; V_i (DC) = 0.65 V; V_i (AC) = 1 V p-p		-	2	-	pF
OSCOUT							
C_i	input capacitance			-	2	-	pF

[1] $\varphi_{n(th)}$ and $f_{\varphi n(th)}$ define the mask for maximum acceptable phase noise of the clock signal at the OSCIN, OSCOUT inputs. See Figure 3 "27.12 MHz input clock phase noise spectrum mask".

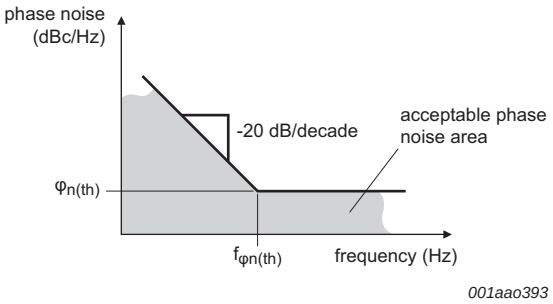

Fig 3. 27.12 MHz input clock phase noise spectrum mask

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10.5 RSTPD_N input pin characteristics

Table 12. RSTPD_N input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$V_{DD(PVDD)}$ −0.4	-	$V_{DD(PVDD)}$	V
V_{IL}	LOW-level input voltage		0	-	0.4	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(PVDD)}$	−1	-	1	μA
I_{IL}	LOW-level input current	V_I = 0 V	−1	-	1	μA
C_i	input capacitance		-	2.5	-	pF

10.6 Input pin characteristics for I0, I1 and TESTEN

Table 13. Input pin characteristics for I0, I1 and TESTEN

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	0.7 × V_{DDD}	-	V_{DDD}	V
V_{IL}	LOW-level input voltage		[2]	0		0.3 × V_{DDD}	V
I_{IH}	HIGH-level input current	I0 and I1; V_I = V_{DDD}	[3]	−1	-	1	μA
I_{IL}	LOW-level input current	V_I = 0 V		−1	-	1	μA
C_i	input capacitance			-	2.5	-	pF

[1] To minimize power consumption when in soft power-down mode, the limit is V_{DDD} − 0.4 V.

[2] To minimize power consumption when in soft power-down mode, the limit is 0.4 V.

[3] TESTEN should never be set to high level in the application. It is used for production test purpose only. It is recommended to connect TESTEN to ground although there is a pull-down included.

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10.7 RSTOUT_N output pin characteristics

Table 14. RSTOUT_N output pin characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_{OH} = −4 mA		0.7 × $V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$	V
		$V_{DD(PVDD)}$ = 1.8 V; I_{OH} = −2 mA	[1]	0.7 × $V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_{OL} = 4 mA		0	-	0.3 × $V_{DD(PVDD)}$	V
		$V_{DD(PVDD)}$ = 1.8 V; I_{OL} = 2 mA	[1]	0	-	0.3 × $V_{DD(PVDD)}$	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V; V_{OH} = 0.8 × $V_{DD(PVDD)}$	[2]	−4	-	-	mA
		$V_{DD(PVDD)}$ = 1.8 V; V_{OH} = 0.7 × $V_{DD(PVDD)}$		−2	-	-	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V; V_{OL} = 0.2 × $V_{DD(PVDD)}$	[2]	4	-	-	mA
		$V_{DD(PVDD)}$ = 1.8 V; V_{OL} = 0.3 × $V_{DD(PVDD)}$		2	-	-	mA
C_L	load capacitance				-	30	pF
t_r	rise time	$V_{DD(PVDD)}$ = 3 V; V_{OH} = 0.8 × $V_{DD(PVDD)}$; C_L = 30 pF		-	-	13.5	ns
		V_{DDP} = 1.8 V; V_{OH} = 0.7 × $V_{DD(PVDD)}$; C_L = 30 pF		-	-	10.8	ns
t_f	fall time	$V_{DD(PVDD)}$ = 3 V; V_{OL} = 0.2 × $V_{DD(PVDD)}$; C_L = 30 pF		-	-	13.5	ns
		$V_{DD(PVDD)}$ = 1.8 V; V_{OL} = 0.3 × $V_{DD(PVDD)}$; C_L = 30 pF		-	-	10.8	ns

[1] Data at $V_{DD(PVDD)}$ = 1.8V are only given from characterization results.

[2] I_{OH} and I_{OL} give the output drive capability from which the rise and fall times may be calculated as a function of the load capacitance.

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10.8 Input/output characteristics for pin P70_IRQ

Table 15. Input/output pin characteristics for pin P70_IRQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	$0.7 \times V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$	V
V_{IL}	LOW-level input voltage		[2]	0	-	$0.3 \times V_{DD(PVDD)}$	V
V_{OH}	HIGH-level output voltage	push-pull mode; $V_{DD(PVDD)}$ = 3 V; I_{OH} = −4 mA		$0.7 \times V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$	V
		push-pull mode; $V_{DD(PVDD)}$ = 1.8 V; I_{OH} = -2 mA	[3]	$0.7 \times V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	push-pull mode; $V_{DD(PVDD)}$ = 3 V; I_{OL} = 4 mA		0	-	$0.3 \times V_{DD(PVDD)}$	V
		push-pull mode; $V_{DD(PVDD)}$ = 1.8 V; I_{OL} = 2 mA	[3]	0	-	$0.3 \times V_{DD(PVDD)}$	V
I_{IH}	HIGH-level input current	input mode; $V_I = V_{DDD}$		−1	-	1	µA
I_{IL}	LOW-level input current	input mode; V_I = 0 V		−1	-	1	µA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V; $V_{OH} = 0.8 \times V_{DD(PVDD)}$	[5]	−4	-	-	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V; $V_{OL} = 0.2 \times V_{DD(PVDD)}$	[5]	4	-	-	mA
I_{LI}	input leakage current	RSTPD_N = 0.4 V		−1	-	1	µA
C_i	input capacitance			-	2.5		pF
C_L	load capacitance			-	-	30	pF
t_r	rise time	$V_{DD(PVDD)}$ = 3 V; $V_{OH} = 0.8 \times V_{DD(PVDD)}$; C_L = 30 pF		-	-	13.5	ns
		$V_{DD(PVDD)}$ = 1.8 V; $V_{OH} = 0.7 \times V_{DD(PVDD)}$; C_L = 30 pF		-	-	10.8	ns
t_f	fall time	$V_{DD(PVDD)}$ = 3 V; $V_{OL} = 0.2 \times V_{DD(PVDD)}$; C_L= 30 pF		-	-	13.5	ns
		$V_{DD(PVDD)}$ = 1.8 V; $V_{OL} = 0.3 \times V_{DD(PVDD)}$; C_L = 30 pF		-	-	10.8	ns

[1] To minimize power consumption when in soft power-down mode, the limit is $V_{DD(PVDD)} - 0.4$ V.

[2] To minimize power consumption when in soft power-down mode, the limit is 0.4 V.

[3] Data at $V_{DD(PVDD)}$ = 1.8 V are only given from characterization results.

[4] The I_{OH} and I_{OL} give the output driving capability and allow to calculate directly the rise and fall time as function of the load capacitance.

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10.9 Input/output pin characteristics for P30 / UART_RX, P31 / UART_TX, P32_INT0, P33_INT1

Table 16. Input/output pin characteristics for P30 / UART_RX, P31 / UART_TX, P32_INT0, P33_INT1

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	$0.7 \times V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$	V
V_{IL}	LOW-level input voltage		[2]	0	-	$0.3 \times V_{DD(PVDD)}$	V
V_{OH}	HIGH-level output voltage	push-pull mode; $V_{DD(PVDD)}$ = 3 V; I_{OH} = −4 mA		$V_{DD(PVDD)}$ −0.4	-	$V_{DD(PVDD)}$	V
		$V_{DD(PVDD)}$ = 1.8 V; I_{OH} = −2 mA	[3]	$V_{DD(PVDD)}$ −0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	push-pull mode; $V_{DD(PVDD)}$ = 3 V; I_{OL} = 4 mA		0	-	0.4	V
		$V_{DD(PVDD)}$ = 1.8 V; I_{OL} = 2 mA	[3]	0	-	0.4	V
I_{IH}	HIGH-level input current	input mode; $V_I = V_{DD(PVDD)}$		−1	-	1	µA
I_{IL}	LOW-level input current	input mode; V_I = 0 V		−1	-	1	µA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V; $V_{OH} = 0.8 \times V_{DD(PVDD)}$	[4]	−4	-	-	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V; $V_{OL} = 0.2 \times V_{DD(PVDD)}$	[4]	4	-	-	mA
I_{LI}	input leakage current	RSTPD_N = 0.4 V		−1	-	1	µA
C_i	input capacitance			-	2.5	-	pF
C_L	load capacitance			-	-	30	pF
t_r	rise time	$V_{DD(PVDD)}$ = 3 V; $V_{OH} = 0.8 \times V_{DD(PVDD)}$; C_L = 30 pF		-	-	13.5	ns
		$V_{DD(PVDD)}$ = 1.8 V; $V_{OH} = 0.7 \times V_{DD(PVDD)}$; C_L = 30 pF		-	-	10.8	ns
t_f	fall time	$V_{DD(PVDD)}$ = 3 V; $V_{OL} = 0.2 \times V_{DD(PVDD)}$; C_L= 30 pF		-	-	13.5	ns
		$V_{DD(PVDD)}$ = 1.8 V; $V_{OL} = 0.3 \times V_{DD(PVDD)}$; C_L = 30 pF		-	-	10.8	ns

[1] To minimize power consumption when in soft power-down mode, the limit is $V_{DD(PVDD)}$ − 0.4 V.

[2] To minimize power consumption when in soft power-down mode, the limit is 0.4 V

[3] Data at $V_{DD(PVDD)}$ = 1.8 V are only given from characterization results.

[4] The I_{OH} and I_{OL} give the output driving capability and allow to calculate directly the rise and fall time as function of the load capacitance.

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10.10 Input/output pin characteristics for P35

Table 17. Input/output pin characteristics for P35

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	$0.7 \times V_{DDD}$	-	V_{DDD}	V
V_{IL}	LOW-level input voltage		[2]	0	-	$0.3 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage	V_{DDD} = 3 V; I_{OH} = −4 mA		$V_{DDD} - 0.4$	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_{OL} = 4 mA		0	-	0.4	V
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$		−1	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V		−1	-	1	µA
I_{OH}	HIGH-level output current	V_{DDD} = 3 V; $V_{OH} = 0.8 \times V_{DD(PVDD)}$	[3]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{DDD} = 3 V; $V_{OL} = 0.2 \times V_{DD(PVDD)}$	[3]	4	-	-	mA
I_{LI}	input leakage current	RSTPD_N = 0.4 V		−1	-	1	µA
C_i	input capacitance			-	2.5	-	pF
C_L	load capacitance			-	-	30	pF
t_r	rise time	V_{DDD} = 3 V; $V_{OH} = 0.8 \times V_{DDD}$; C_L = 30 pF		-	-	13.5	ns
		V_{DDD} = 1.8 V; $V_{OH} = 0.7 \times V_{DDD}$; C_L = 30 pF		-	-	10.8	ns
t_f	fall time	V_{DDD} = 3 V; $V_{OL} = 0.2 \times V_{DDD}$; C_L= 30 pF		-	-	13.5	ns
		V_{DDD} = 1.8 V; $V_{OL} = 0.3 \times V_{DDD}$; C_L = 30 pF		-	-	10.8	ns

[1] To minimize power consumption when in soft power-down mode, the limit is $V_{DDD} - 0.4$ V.

[2] To minimize power consumption when in soft power-down mode, the limit is 0.4 V.

[3] The I_{OH} and I_{OL} give the output driving capability and allow to calculate directly the rise and fall time as function of the load capacitance.

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10.11 Input/output pin characteristics for DP and DM

Table 18. Input/output pin characteristics for DP and DM for USB interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(PVDD)}$ = 3.3 V		2	-	3.6	V
V_{IL}	LOW-level input voltage		[1]	0	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3.3 V; R_{PD} = 1.5 Ω to V_{SS}		2.8	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3.3 V; R_{PD} = 1.5 Ω to $V_{DD(PVDD)}$		0	-	0.3	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3.3 V; V_{OH} = 0.8 × $V_{DD(PVDD)}$	[2]	−4	-	-	mA
		$V_{DD(PVDD)}$ = 1.8 V; V_{OH} = 0.7 × $V_{DD(PVDD)}$		−2	-	-	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3.3 V; V_{OL} = 0.2 × $V_{DD(PVDD)}$	[2]	4	-	-	mA
		$V_{DD(PVDD)}$ = 1.8 V; V_{OL} = 0.3 × $V_{DD(PVDD)}$		2	-	-	mA
I_{IH}	HIGH-level input current	V_I = $V_{DD(PVDD)}$		-	-	1	μA
I_{IL}	LOW-level input current	V_I = 0 V		-	-	1	μA
I_{LI}	input leakage current	RSTPD_N = 0 V		−1	-	+1	μA
C_i	input capacitance			-	2.5	3.5	pF
Z_{INP}	input impedance exclusive of pull-up/pull-down (for low-/full speed)			300	-	-	kΩ
Z_{DRV}	driver output impedance for driver which is not high-speed capable			28	-	44	Ω
t_{FDRATE}	full-speed data rate for devices which are not high-speed capable			11.97	-	12.03	Mb/s
t_{DJ1}	source jitter total (including frequency tolerance) to next transition			−3.5	-	+3.5	ns
t_{DJ2}	source jitter total (including frequency tolerance) for paired transitions			−4	-	+4	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition			−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions			−9	-	+9	ns
t_{FEOPT}	source SE0 interval of EOP			160	-	175	ns
t_{FEOPR}	receiver SE0 interval of EOP			82	-	-	ns
t_{FST}	width of SE0 interval during differential transition			-	-	14	ns

[1] The value does not guarantee the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 V.

[2] The I_{OH} and I_{OL} give the output driving capability and allow to calculate directly the rise and fall time as function of the load capacitance.

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Table 19. USB DP/DM differential receiver input levels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DI}	differential input sensitivity voltage	-	0.2	-	-	V
V_{CM}	differential common mode voltage range	-	0.8	-	2.5	V

Table 20. USB DP/DM driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	C_L = 50 pF; 10 % to 90 % of (V_{OH} - V_{OL})	4	-	20	ns
t_f	fall time	C_L = 50 pF; 10 % to 90 % of (V_{OH} - V_{OL})	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	(t_{FR}/t_{FF}); excluding the first transition from Idle state	90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state	1.3	-	2.0	V

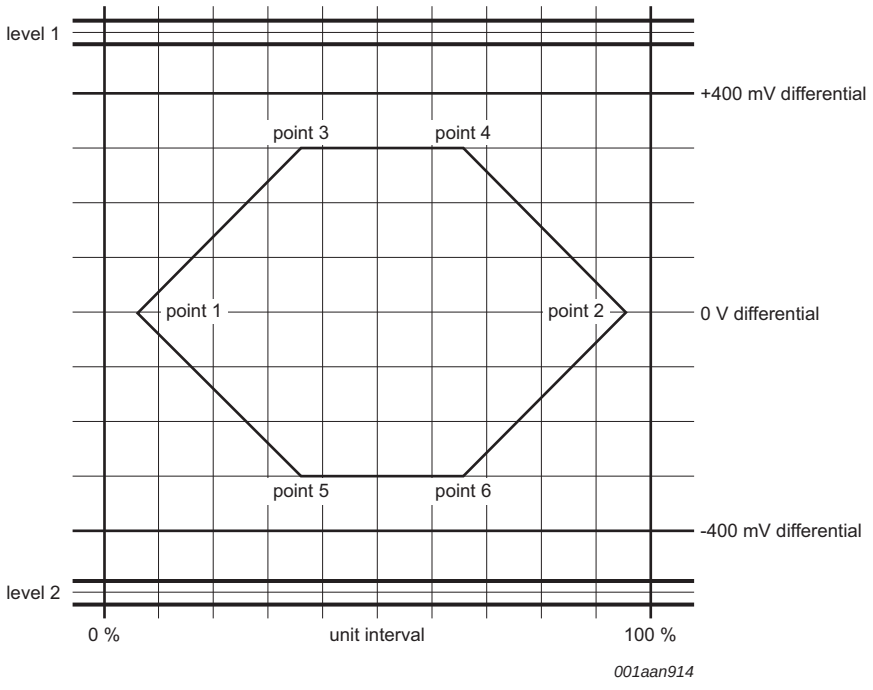

Fig 4. Transmit waveform at DP/DM

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Table 21. Input Pin characteristics for DP for HSU interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	$0.7 \times V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$	V
V_{IL}	LOW-level input voltage		[2]	0	-	$0.3 \times V_{DD(PVDD)}$	V
I_{IH}	HIGH-level input current	$V_i = V_{DD(PVDD)}$		-	-	1	mA
I_{IL}	LOW-level input current	$V_i = 0$ V		-	-	1	mA
I_{LI}	input leakage current	RSTPD_N = 0 V		–1		1	mA
C_i	input capacitance			-	2.5	3.5	pF

[1] The value does not guarantee the power-down consumptions. To reach the specified power-down consumptions, the limit is $V_{DD(PVDD)}$ –0.4 V.

[2] The value does not guarantee the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 V.

Table 22. Output Pin characteristics for DM for HSU interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)} = 3$ V; $I_{OH} = -4$ mA		$V_{DD(PVDD)} - 0.4$	-	$V_{DD(PVDD)}$	V
		$V_{DD(PVDD)} = 1.8$ V; $I_{OH} = -2$ mA		$V_{DD(PVDD)} - 0.4$	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)} = 3$ V; $I_{OL} = -4$ mA		0	-	0.4	V
		$V_{DD(PVDD)} = 1.8$ V; $I_{OL} = -2$ mA		0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)} = 3$ V; $V_{OH} = 0.8 \times V_{DD(PVDD)}$	[1]	–4	-	-	mA
		$V_{DD(PVDD)} = 1.8$ V; $V_{OH} = 0.7 \times V_{DD(PVDD)}$		–2	-	-	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)} = 3.3$ V; $V_{OL} = 0.2 \times V_{DD(PVDD)}$	[1]	4	-	-	mA
		$V_{DD(PVDD)} = 1.8$ V; $V_{OL} = 0.3 \times V_{DD(PVDD)}$		2	-	-	mA
I_{LI}	input leakage current	RSTPD_N = 0 V		–1	-	1	mA
C_L	load capacitance			-	-	30	pF
t_r	rise time	$V_{DDP} = 3$ V; $V_{OH} = 0.8 \times V_{DD(PVDD)}$; $C_L = 30$ pF		-	-	13.5	ns
		$V_{DD(PVDD)} = 1.8$ V; $V_{OH} = 0.7 \times V_{DD(PVDD)}$; $C_L = 30$ pF		-	-	10.8	ns
t_f	fall time	$V_{DD(PVDD)} = 3$ V; $V_{OL} = 0.2 \times V_{DD(PVDD)}$; $C_L = 30$ pF		-	-	13.5	ns
		$V_{DDP} = 1.8$ V; $V_{OL} = 0.3 \times V_{DD(PVDD)}$; $C_L = 30$ pF		-	-	10.8	ns

[1] The I_{OH} and I_{OL} give the output driving capability and allow to calculate directly the rise and fall time as function of the load capacitance

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10.12 Input pin characteristics for SDA/P50_SLC

Table 23. Input/output drain output pin characteristics for SDA/P50_SLC I²C interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	$0.7 \times V_{DD(PVDD)}$	-	V_{DDD}	V
V_{IL}	LOW-level input voltage		[2]	0	-	$0.3 \times V_{DDD}$	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_{OL} = −4 mA		0	-	0.3	V
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$		−1	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V		−1	-	1	µA
I_{LI}	input leakage current	RSTPD_N = 0.4 V		−1	-	1	µA
C_i	input capacitance			-	2.5		pF
C_L	load capacitance			-	-	30	pF
t_r	rise time of both SDA and SCL signals		[3]	20	-	300	ns
t_f	fall time of both SDA and SCL signals		[3]	20	-	300	ns

[1] To minimize power consumption when in soft power-down mode, the limit is V_{DDD} − 0.4 V.

[2] To minimize power consumption when in soft power-down mode, the limit is 0.4 V.

[3] The PR533 has a slope control according to the I²C-bus specification for the Fast mode. The slope control is always present and not dependent of the I²C-bus speed.

10.13 Output pin characteristics for DELATT

Table 24. Output pin characteristics for DELATT

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage		[1]	$0.7 \times V_{DD(SVDD)}$	-	$V_{DD(SVDD)}$	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(PVDD)}$	V
I_{IH}	HIGH-level input current	input mode; $V_I = V_{DD(SVDD)}$		−1	-	1	µA
I_{IL}	LOW-level input current	input mode; V_I = 0 V		−1	-	1	µA
I_{LI}	input leakage current	RSTPD_N = 0.4 V		−1	-	1	µA
C_i	input capacitance			-	2.5	-	pF

[1] To minimize power consumption when in soft power-down mode, the limit is $V_{DD(PVDD)}$ − 0.4 V.

10.14 Input pin characteristics for SIGIN

Table 25. Input/output pin characteristics for SIGIN

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	$0.7 \times V_{DD(SVDD)}$	-	$V_{DD(SVDD)}$	V
V_{IL}	LOW-level input voltage		[2]	0	-	$0.3 \times V_{DD(SVDD)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(SVDD)}$		−1	-	+1	µA
I_{IL}	LOW-level input current	V_I = 0 V		−1	-	+1	µA
I_{LI}	input leakage current	RSTPD_N = 0.4 V		−1	-	+1	µA
C_i	input capacitance			-	2.5	-	pF

[1] To minimize power consumption when in soft power-down mode, the limit is $V_{DD(SVDD)}$ − 0.4 V.

[2] To minimize power consumption when in soft power-down mode, the limit is 0.4 V.

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10.15 Output pin characteristics for SIGOUT

Table 26. Output pin characteristics for SIGOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OH} = -4$ mA	$V_{DD(SVDD)} - 0.4$	-	$V_{DD(SVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OL} = +4$ mA	0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OH} = -4$ mA	−0.4	-	-	mA
I_{OL}	LOW-level output current	$V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OL} = +4$ mA	4	-	-	mA
I_{LI}	input leakage current	RSTPD_N = 0.4 V	−1	-	+1	µA
C_i	input capacitance		-	2.5		pF
C_L	load capacitance		-	-	30	pF
t_r	rise time	$V_{DD(SVDD)} = 3$ V; $V_{OH} = 0.8 \times V_{DD(SVDD)}$; $C_{out} = 30$ pF	-	-	9	ns
t_f	fall time	$V_{DD(SVDD)} = 3$ V; $V_{OL} = 0.2 \times V_{DD(SVDD)}$; $C_{out} = 30$ pF	-	-	9	ns

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10.16 Input/output pin characteristics for P34

Table 27. Input/output pin characteristics for P34

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		[1]	$0.7 \times V_{DD(SVDD)}$	-	$V_{DD(SVDD)}$	V
V_{IL}	LOW-level input voltage		[2]	0	-	$0.3 \times V_{DD(SVDD)}$	V
V_{OH}	HIGH-level output voltage	push-pull; $V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OH} = -4$ mA		$V_{DD(SVDD)} - 0.4$	-	$V_{DD(SVDD)}$	V
V_{OL}	LOW-level output voltage	push-pull; $V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OH} = +4$ mA		0	-	0.4	V
I_{IH}	HIGH-level input current	input mode; $V_I = V_{DD(SVDD)}$		–1	-	+1	µA
I_{IL}	LOW-level input current	input mode; $V_I = 0$ V		–1	-	+1	µA
V_{OH}	HIGH-level output voltage	$V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OH} = -4$ mA		–0.4	-	-	V
V_{OL}	LOW-level output voltage	$V_{DDD} - 0.1 < V_{DD(SVDD)} < V_{DDD}$ $I_{OL} = +4$ mA		4	-	-	V
I_{LI}	input leakage current	RSTPD_N = 0.4 V		–1	-	+1	µA
C_i	input capacitance			-	2.5		pF
C_L	load capacitance			-		30	pF
t_r	rise time	$V_{DDD} = 0.1 < V_{DDD}$ $V_{OH} = 0.8 \times V_{DD(SVDD)}$; $C_{out} = 30$ pF	[3]	-	13.5	-	ns
t_f	fall time	$V_{DDD} = 0.1 < V_{DDD}$ $V_{OL} = 0.2 \times V_{DD(SVDD)}$; $C_{out} = 30$ pF	[3]	-	13.5	-	ns

[1] To minimize power consumption when in soft power-down mode, the limit is $V_{DD(SVDD)} - 0.4$ V.

[2] To minimize power consumption when in soft power-down mode, the limit is 0.4 V.

[3] I_{OH} and I_{OL} specify the output drive capability from which the rise and fall times may be calculated as a function of the load capacitance.

10.17 Output pin characteristics for LOADMOD

Table 28. Output pin characteristics for LOADMOD

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DDD} = 3$ V; $I_{OH} = -4$ mA	$V_{DDD} - 0.4$	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	$V_{DDD} = 3$ V; $I_{OL} = 4$ mA	0	-	0.4	V
C_L	load capacitance		-	-	10	pF
t_r	rise time	$V_{DDD} = 3$ V; $V_{OH} = 0.8 \times V_{DDD}$; $C_{out} = 10$ pF	-	-	4.5	ns
t_f	fall time	$V_{DDD} = 3$ V; $V_{OL} \times = 0.2 \times V_{DDD}$; $C_{out} = 10$ pF	-	-	4.5	ns

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10.18 Input pin characteristics for RX

Table 29. Input pin characteristics for RX

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_i	input voltage	dynamic; signal frequency at 13.56 MHz	–0.7		V_{DDA} +1	V
C_i	input capacitance		6	10	14	pF
R_s	series resistance	RX input; V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V DC offset	315	350	385	Ω
Minimum dynamic input voltage						
$V_{RX(p-p)}$	peak-to-peak receiver voltage	Miller coded; 106 kbit/s	-	150	500	mV
		Manchester coded; 212 kbit/s and 424 kbit/s	-	100	200	mV
Maximum dynamic input voltage						
$V_{RX(p-p)}$	peak-to-peak receiver voltage	Miller coded; 106 kbit/s	V_{DDA}	-	-	V
		Manchester coded; 212 and 424 kbit/s	V_{DDA}	-	-	V
Minimum modulation voltage						
V_{mod}	modulation voltage	RxGain = 6 and 7 [1]	-	-	6	mV
		RxGain = 4 and 5 [1]	-	-	18	mV
		RxGain = 0 to 3 [1]	-	-	120	mV
Minimum modulation index						
m	modulation index	Miller coded; 106 kbit/s $V_{RX(p-p)}$= 1.5 V; SensMiller = 3	-	33	-	%

[1] The minimum modulation voltage is valid for all modulation schemes except Miller coded signals.

10.19 Output pin characteristics for AUX1/AUX2

Table 30. Output pin characteristics for AUX1/AUX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	V_{DDD} = 3 V; I_{OH} = –4 mA	V_{DDD} – 0.4	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_{OL} = 4 mA	V_{SSD}	-	V_{SSD} +0.4	V
I_{OH}	HIGH-level output current	V_{DDD}= 3 V; V_{OH} = V_{DDD} –0.3	–4	-	-	mA
I_{OL}	LOW-level output current	V_{DDD}= 3 V; V_{OL} = V_{DDD} -0.3	4	-	-	mA

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Table 30. Output pin characteristics for AUX1/AUX2 *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current	RSTPD_N = 0 V	–1	-	+1	µA
C_i	input capacitance		-	2.5	-	pF
C_L	load capacitance		-	-	15	pF

10.20 Output pin characteristics for TX1/TX2

Table 31. Output pin characteristics for TX1/TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(TVDD)}$ = 3 V; I_O = 32 mA; CWGsN = Fh	-	-	150	mV
		$V_{DD(TVDD)}$ = 3 V; I_O = 80 mA; CWGsN = Fh	-	-	400	mV
V_{OL}	LOW-level output voltage	$V_{DD(TVDD)}$ = 2.5 V; I_O = 32 mA; CWGsN = Fh	-	-	240	mV
		$V_{DD(TVDD)}$ = 2.5 V; I_O = 80 mA; CWGsN = Fh	-	-	640	mV

Table 32. Output resistance for TX1/TX2

Symbol	Parameter	Conditions1	CWGsP	Min	Typ	Max	Unit
R_{OH}	HIGH-level output resistance	$V_{DD(TVDD)}$ = 3 V; V_O = $V_{DD(TVDD)}$ − 100 mV	01h	133	180	251	Ω
			02h	67	90	125	Ω
			04h	34	46	62	Ω
			08h	17	23	31	Ω
			10h	8.5	12	15.5	Ω
			20h	4.7	6	7.8	Ω
			3Fh	2.3	3	4.4	Ω
R_{OL}	LOW-level output resistance		10h	34	46	62	Ω
			20h	17	23	31	Ω
			40h	8.5	12	15.5	Ω
			80h	4.7	6	7.8	Ω
			F0h	2.3	3	4.4	Ω

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10.21 System reset timing

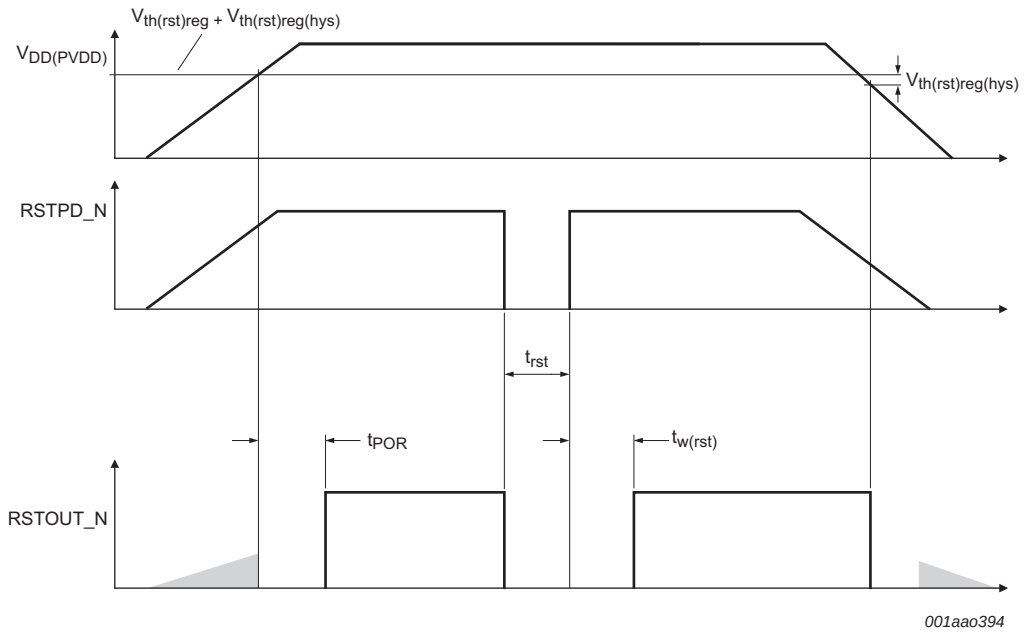

Fig 5. System reset overview

Table 33. Reset duration time

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{POR}	power-on reset time		[1]	0.1	0.4	2	ms
t_{rst}	reset time	hard power-down time; user dependent	[2]	20	-	-	ns
$t_{w(rst)}$	reset pulse width	reset time when RSTPD_N is released	[1]	0.1	0.4	2	ms

[1] Dependent on the 27.12 MHz crystal oscillator startup time.

[2] If the t_{rst} pulse is shorter than 20 ns, the device may be only partially reset.

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10.22 Timing for the I²C-bus interface

Table 34. I²C-bus timing specification

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			0	-	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	after this period, the first clock pulse is generated		600	-	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition			600	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			600	-	-	ns
t_{LOW}	LOW period of the SCL clock	P50_SCL		1300	-	-	ns
t_{HIGH}	HIGH period of the SCL clock	P50_SCL		600	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	900	ns
$t_{SU;DAT}$	data set-up time			100	-	-	ns
t_r	rise time of both SDA and SCL signals	P50_SCL	[1]	20	-	300	ns
t_f	fall time of both SDA and SCL signals	P50_SCL	[1]	20	-	300	ns
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	ms
$t_{stretch}$	stretch time	stretching time on P50_SCL when woken-up on its own address	[2]	-	-	1	ms
t_h	hold time	internal for SDA		330	-	590	ns
		internal for SDA in SPD mode	[3]	-	270	-	ns

[1] The PR533 has a slope control according to the I²C-bus specification for the Fast mode. The slope control is always present and not dependent of the I²C-bus speed.

[2] 27.12 MHz quartz starts in less than 800 µs. For example, quartz like TAS-3225A, TAS-7 or KSS2F with appropriate layout.

[3] The PR533 has an internal hold time of around 270ns for the SDA signal to bridge the undefined region of the falling edge of P50_SCL.

10.23 Temperature sensor

Table 35. Temperature sensor characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{th(act)otp}$	overtemperature protection activation threshold temperature	CIU	[1]	100	125	140	°C

[1] The temperature sensor embedded in the PR533 is not intended to monitor the temperature. Its purpose is to prevent destruction of the IC due to excessive heat. The external application should include circuitry to ensure that the ambient temperature does not exceed 85 °C as specified in Table 5 “Operating conditions”.

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11. Application information

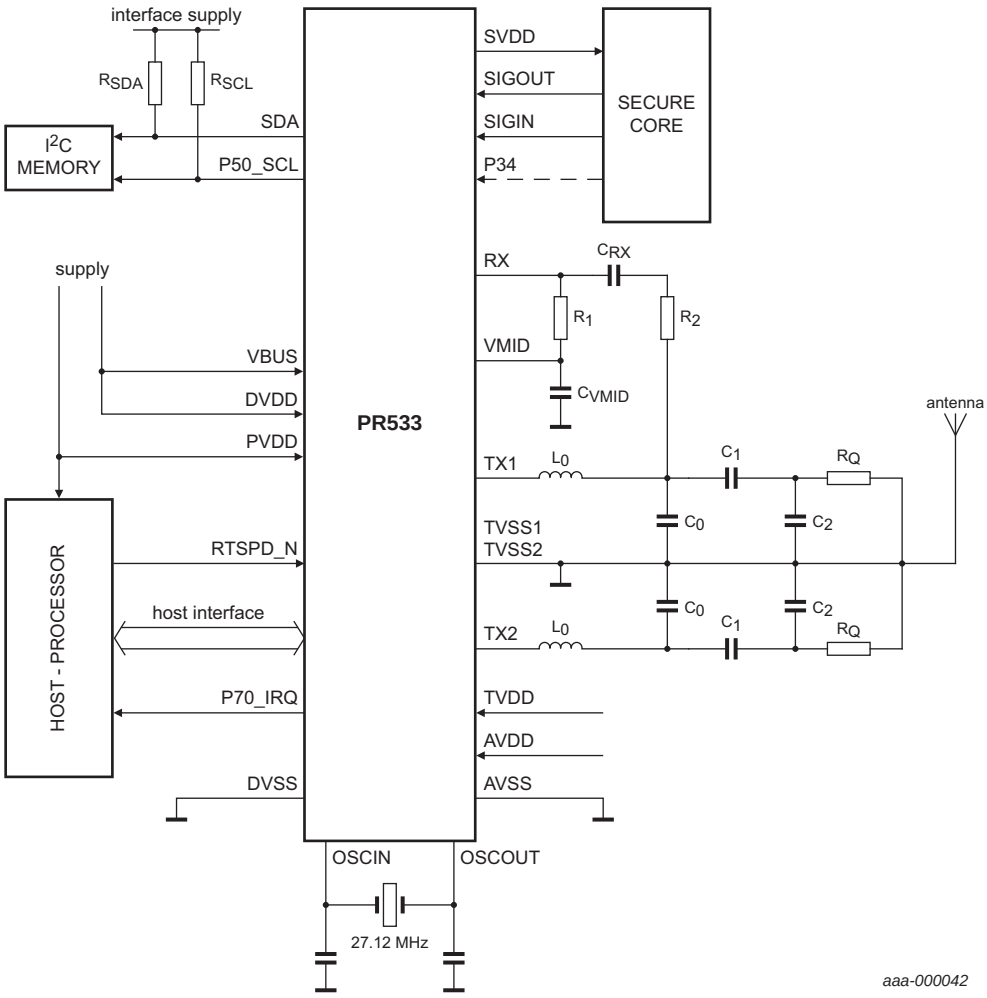

Fig 6. Application diagram of PR533

12. Abbreviations

Table 36. Abbreviations

Acronym	Description
CDM	Charge device Body Model
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read-Only Memory
HBM	Human Body Model
HPD	Hard Power Down
MM	Machine Model
NFC	Near Field Communication
SPD	Soft Power Down mode

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13. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PR5331C3HN_SDS v.3.0	20110803	Product short data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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