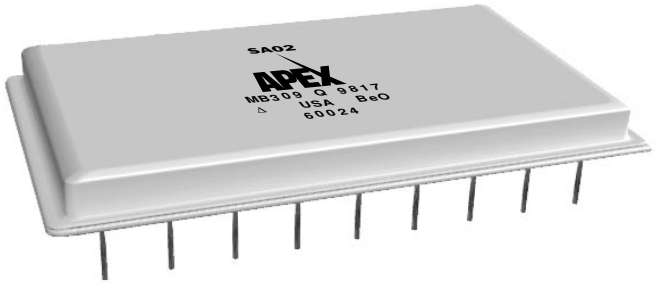
SA02

FEATURES

- 250kHz SWITCHING
- FULL BRIDGE OUTPUT 16-80V (160V P-P)
- 10A OUTPUT
- FAULT PROTECTION
- SHUTDOWN CONTROL
- SYNCHRONIZABLE CLOCK
- HERMETIC PACKAGE



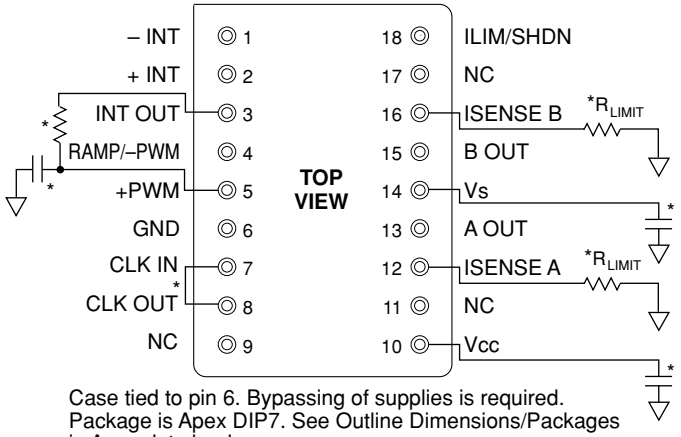
APPLICATIONS

- AIRCRAFT AUDIO AMPLIFIER
- BRUSH TYPE MOTOR CONTROL
- VIBRATION CANCELLING AMPLIFIER

DESCRIPTION

The SA02 amplifier is an 80 volt, 250kHz PWM amplifier. The full bridge output circuit provides 10 amps of continuous drive current for applications as diverse as aircraft audio and brush type motors. Clock output and input pins can be used for synchronization with other amplifiers or an externally generated clock. A separate integrator amplifier is also accessible and the integration may be varied for the application. Direct access to the pwm input is provided for connection to digital motion control circuits. Protection circuits guard against thermal overloads as well as shorts to supply or ground. The current limit is programmable with one or two external resistors depending on the application. A shutdown input disables all output bridge drivers. The 18 pin DIP7 steel package is hermetically sealed.

EXTERNAL CONNECTIONS

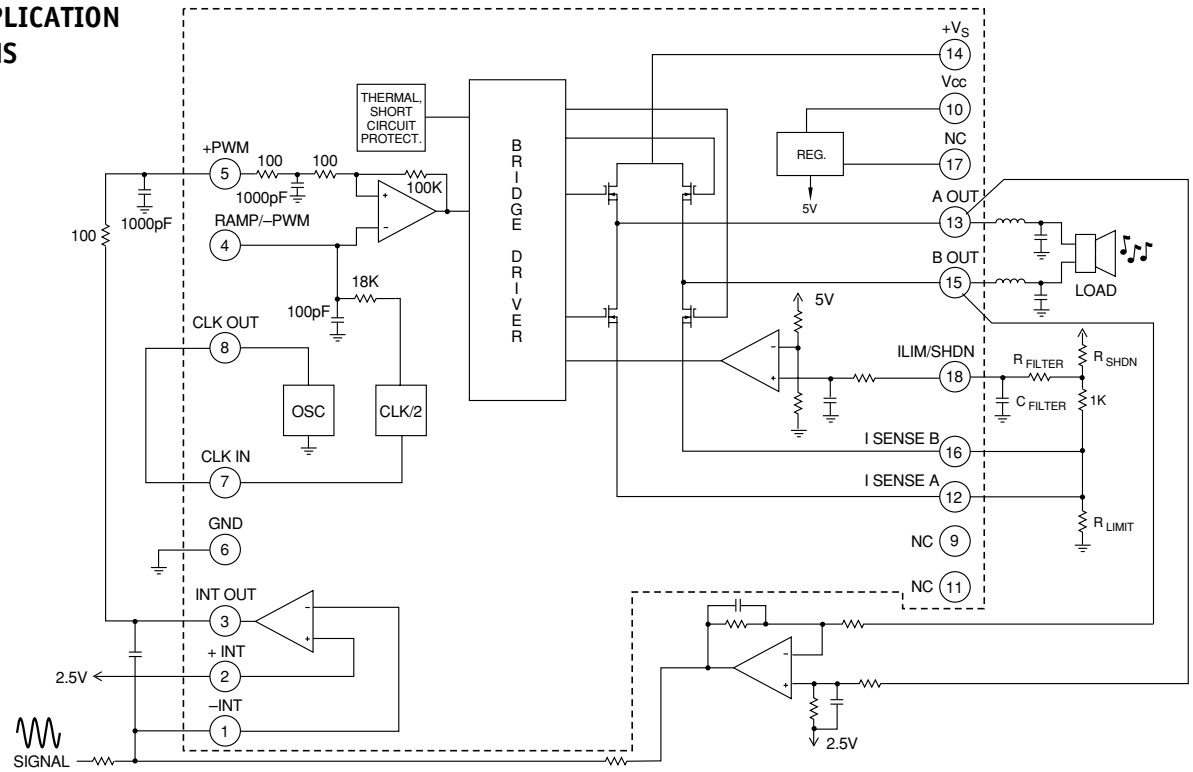


Case tied to pin 6. Bypassing of supplies is required. Package is Apex DIP7. See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/–PWM then A OUT > B OUT and ISENSE B > ISENSE A.

* See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION CONNECTIONS AIRCRAFT AUDIO



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, Vcc to GND	15V
SUPPLY VOLTAGE, $+V_S$ to GND	80V
OUTPUT CURRENT, peak	15A
±PWM	0 TO Vcc
CLK IN, ±INT V_{IN}, ILIM/SHDN V_{IN}	0 to +6V
POWER DISSIPATION, internal	156W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INTEGRATOR, CLOCK[3]					
OFFSET VOLTAGE				2	mV
BIAS CURRENT				150	nA
OFFSET CURRENT				30	nA
COMMON MODE VOLTAGE RANGE		0		+3	V
COMMON MODE REJECTION, DC		80			dB
SLEW RATE			15		V/µS
OPEN LOOP GAIN	R_L = 10KΩ	94			dB
GAIN BANDWIDTH PRODUCT			4.5		MHz
CLOCK OUT	$R_L \geq$ 10KΩ		500		kHz
CLOCK OUT, high level		4.7		5.3	V
CLOCK OUT, low level		0		.2	V
CLOCK IN, low level		0		.3	V
CLOCK IN, high level		2		5.6	V
OUTPUT					
EFFICIENCY, 10A output	V_S = 80V		94		%
SWITCHING FREQUENCY			250		kHz
CURRENT, continuous		10			A
CURRENT, peak[3]		15			A
$R_{DS(ON)}$[3]				.42	Ω
POWER SUPPLY					
VOLTAGE, V_{CC}	Full temperature range	10	12	15	V
VOLTAGE, V_S	Full temperature range	16		80	V
CURRENT, V_{CC}	V_{CC} = 12V		36	50	mA
CURRENT, V_S	Switching, No Load, V_S = 60V		70	90	mA
INPUTS[3]					
I_{LIM}/SHDN, trip point		90		110	mV
±PWM COMMON MODE VOLTAGE		1		Vcc – 1.5	V
THERMAL[4]					
RESISTANCE, junction to case	Full temperature range			1.6	°C/W
RESISTANCE, junction to air	Full temperature range		15		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	°C

NOTES:
1. 80W in each of the two active output transistors on at any one time.
2. Unless otherwise noted: T_C = 25°C.
3. Min max values guaranteed but not tested.
4. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

CAUTION

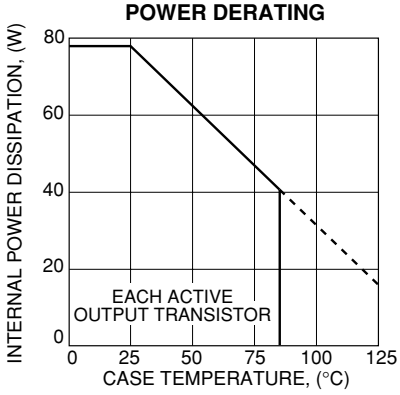
The SA02 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

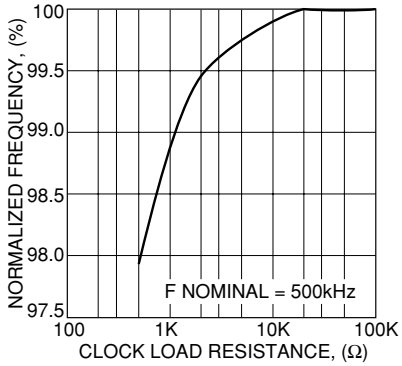
TYPICAL PERFORMANCE GRAPHS

SA02

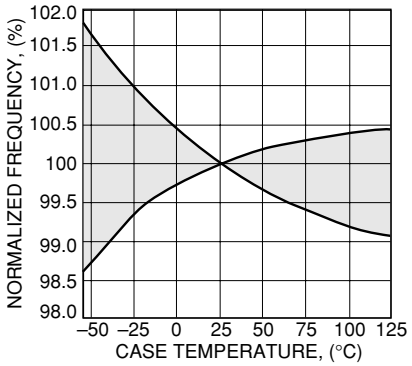
POWER DERATING



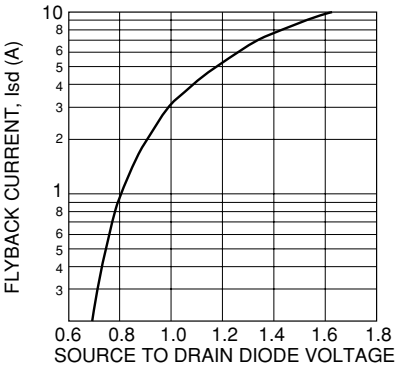
CLOCK LOADING



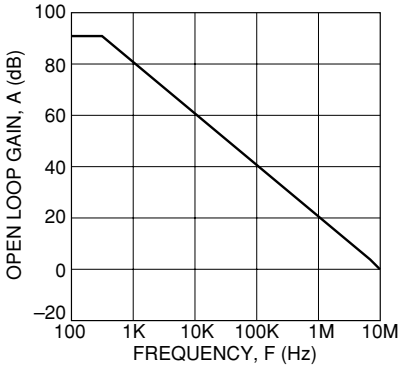
CLOCK FREQUENCY OVER TEMP



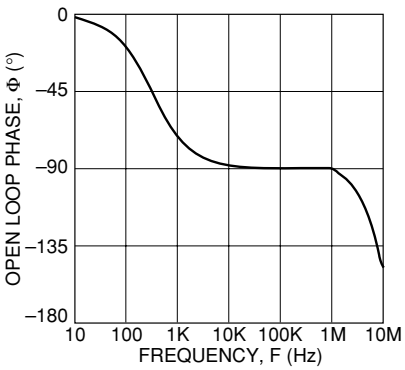
REVERSE DIODE



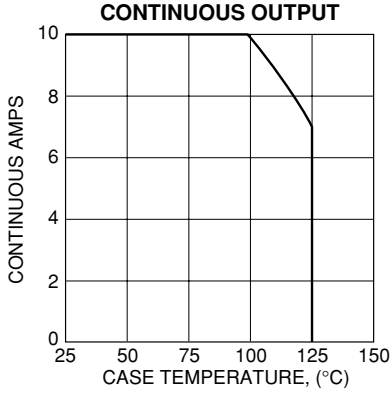
INTEGRATOR GAIN



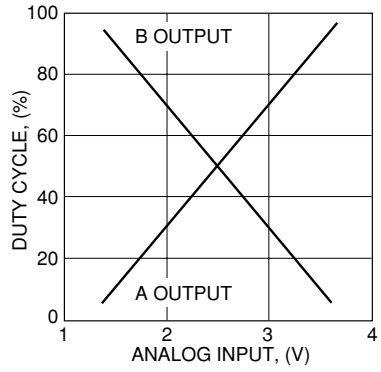
INTEGRATOR PHASE



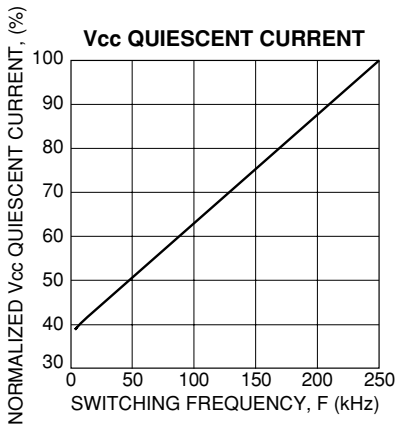
CONTINUOUS OUTPUT



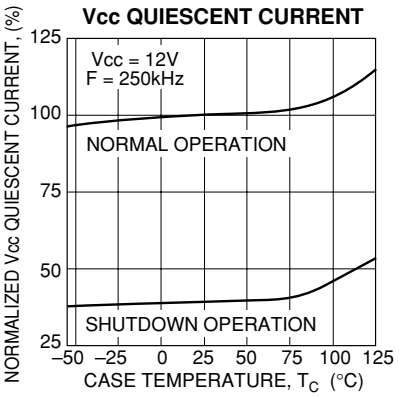
DUTY CYCLE VS ANALOG INPUT



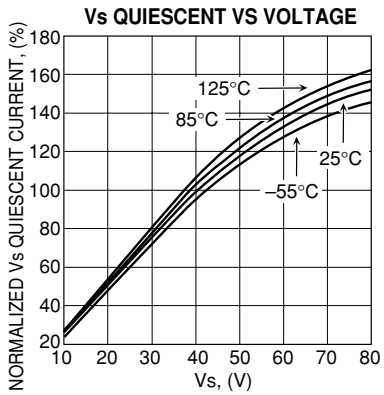
Vcc QUIESCENT CURRENT



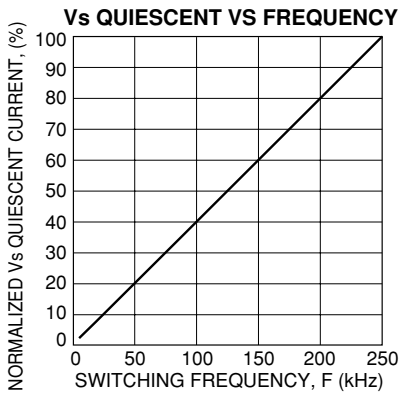
Vcc QUIESCENT CURRENT



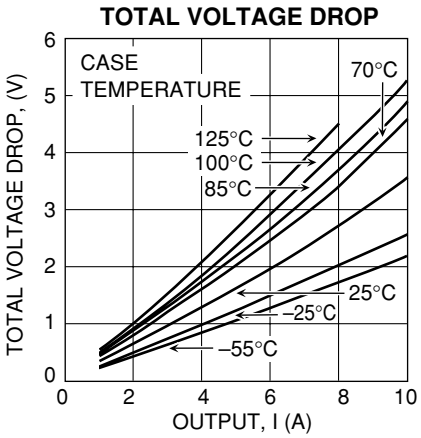
Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



C



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 500 kHZ. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 500kHZ is chosen an external capacitor must be tied to the RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 2.5 volts p-p with the lower peak 1.25 volts above ground.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1μF ceramic capacitor in parallel with another low ESR capacitor of at least 10μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1μF to .47μF ceramic capacitor connected directly to the Vcc pin will suffice.

NOISE FILTERING

Switching noise can enter the SA02 through the INT OUT to +PWM connection. A wise precaution is to low pass filter this connection. Adjust the pass band of the filter to 10 times the bandwidth required by the application. Keep the resistor value to 100 ohms or less since this resistor becomes part of the hysteresis circuit on the pwm comparator.

PCB LAYOUT

The designer needs to appreciate that the SA02 combines in one circuit both high speed high power switching and low level analog signals. Certain layout rules of thumb must be considered when a circuit board layout is designed using the SA02:

1. Bypassing of the power supplies is critical. Capacitors must be connected directly to the power supply pins with very short lead lengths (well under 1 inch). Ceramic chip capacitors are best.
2. Make all ground connections with a star pattern at pin 6.
3. Beware of capacitive coupling between output connections and signal inputs through the parasitic capacitance between layers in multilayer PCB designs.
4. Do not run small signal traces between the pins of the output section (pins 11-17).
5. Do not allow high currents to flow into the ground plane.
6. Separate switching and analog grounds and connect the two only at pin 6 as part of the star pattern.

INTEGRATOR

The integrator provides the inverted signal for negative feedback and also the open loop gain for the overall application circuit accuracy. Recommended value of C_{INT} is 10 pF for stability. However, poles and zeroes can be added to the circuit for overall loop stability as required.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100

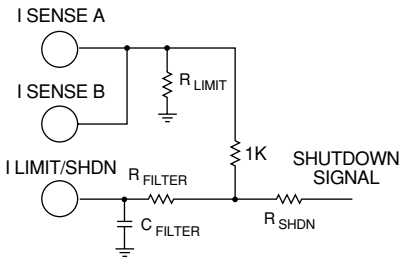


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

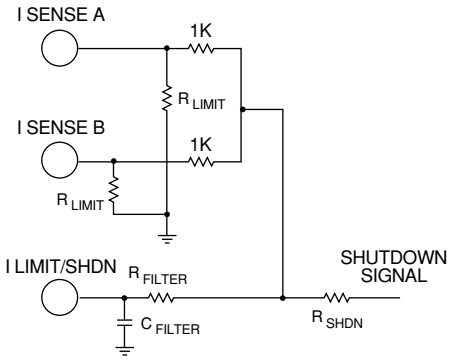


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .001uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

SHUTDOWN

The shutdown circuitry makes use of the internal current limiting circuitry. The two functions may be externally combined in voltage and current modes as shown below in Figures A and B. The R_{LIMIT} resistors will normally be very low values and can be considered zero for this application. In Figure A, R_{SHDN} and 1K form a voltage divider for the shutdown signal. After a suitable noise filter is designed for the current limit, adjust the value of R_{SHDN} to give a minimum 110 mV of shutdown signal at the I LIMIT/SHDN pin when the shutdown signal is high. Note that C_{FILTER} will filter both the current limit noise spikes and the shutdown signal. Shutdown and current limit operate on each cycle of the internal switching rate. As long as the shutdown signal is high the output will be disabled.

PROTECTION CIRCUITS

Circuits monitor the temperature and load on each of the bridge output transistors. On each cycle should any fault condition be detected all output transistors in the bridge are shut off. Faults protected against are: shorts across the outputs, shorts to ground, and over temperature conditions. Should any of these faults be detected, the output transistors will be latched off. The fault must be removed and V_{CC} power recycled to restart the SA02. In addition there is a built in dead time during which all the output transistors are off. The dead time removes the possibility of a momentary conduction path through the upper and lower transistors of each half bridge during the switching interval. Noise or flyback may be observed at the outputs during this time due to the high impedance of the outputs in the off state. This will vary with the nature of the load.

C

