



5N50K

Power MOSFET

5A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

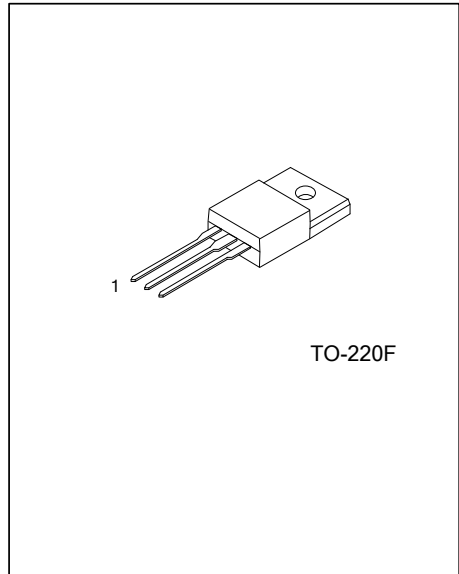
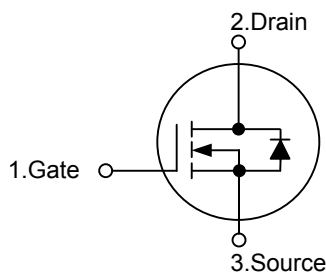
The UTC **5N50K** is a n-channel power MOSFET adopting UTC's advanced technology to provide customers with DMOS, planar stripe technology. This technology is designed to meet the requirements of the minimum on-state resistance and perfect switching performance. It also can withstand high energy pulse in the avalanche and communication mode.

The UTC **5N50K** can be used in applications, such as active power factor correction, high efficiency switched mode power supplies, electronic lamp ballasts based on half bridge topology.

FEATURES

- * $R_{DS(ON)} = 1.4\Omega @ V_{GS} = 10V$
- * 100% avalanche tested
- * High switching speed

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5N50KL-TF3-T	5N50KG-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

5N50KL-TF3-R	(1) Packing Type	(1) T: Tube
	(2) Package Type	(2) TF3: TO-220F
	(3) Lead Free	(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER SYMBOL		RATINGS	UNIT
Drain-Source Voltage		V_{DSS} 500	V
Gate-Source Voltage		V_{GSS} ± 30	V
Drain Current	Continuous I	I_D 5	A
	Pulsed (Note 2)	I_{DM} 20	A
Avalanche Current (Note 2)		I_{AR} 5	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS} 270	mJ
	Repetitive (Note 2)	E_{AR} 7.3	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt 4.5	V/ns
Power Dissipation		P_D 38	W
Junction Temperature		T_J + 150	$^{\circ}\text{C}$
Storage Temperature		T_{STG} -55 ~ +150	$^{\circ}\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 21.5\text{mH}$, $I_{AS} = 5.2\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER SYMBOL		RATINGS	UNIT
Junction to Ambient		θ_{JA} 62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case		θ_{JC} 3.25	$^{\circ}\text{C}/\text{W}$

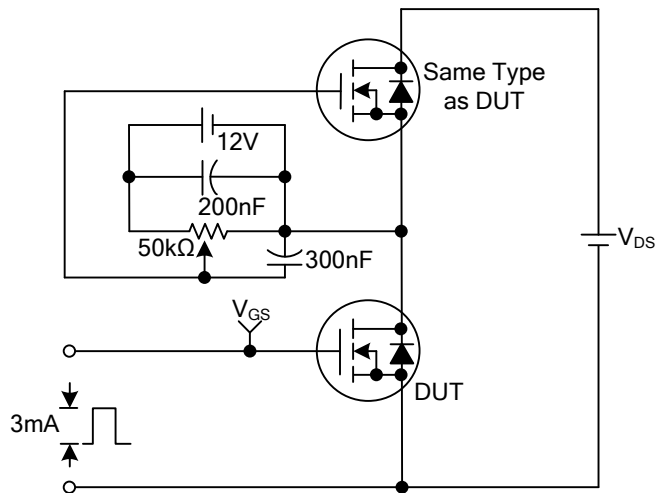
■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V 500				V
Breakdown Voltage Temperature Coefficient		ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =250μA		0.5		V/°C
Drain-Source Leakage Current		I _{DSS}	V _{DS} =500V, V _{GS} =0V			1	μA
			V _{DS} =400V, T _C =125°C			10	
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V, V _{DS} =0V			100	nA
	Reverse V		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2.5A		1.2	1.4	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		480	625	pF
Output Capacitance		C _{OSS}			80	105	pF
Reverse Transfer Capacitance		C _{RSS}			15	20	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{GS} =10V, V _{DS} =400V, I _D =5A (Note 1, 2)	18		24	nC
Gate to Source Charge		Q _{GS}			2.2		nC
Gate to Drain Charge		Q _{GD}			9.7		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =250V, I _D =5A, R _G =25Ω (Note 1, 2)		12	35	ns
Rise Time		t _R			46	100	ns
Turn-OFF Delay Time		t _{D(OFF)}			50	110	ns
Fall-Time t		F			48	105	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				5	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				20	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =5A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =5A, V _{GS} =0V,		263		ns
Reverse Recovery Charge		Q _{RR}	dl _F /dt=100A/μs (Note 1)		1.9		μC

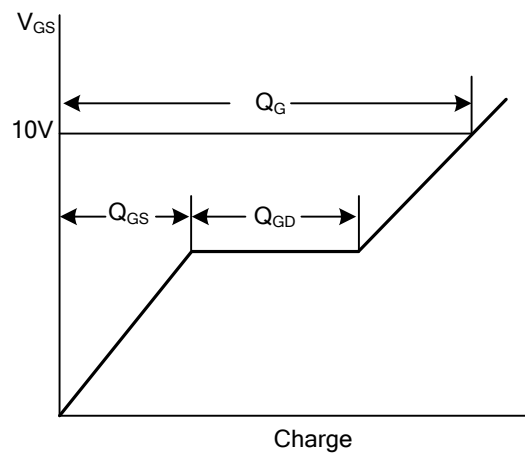
Note: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

2. Essentially independent of operating temperature

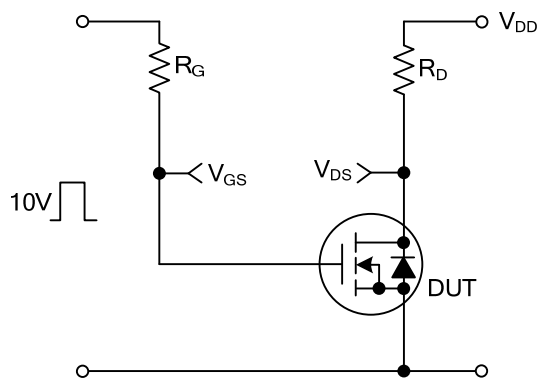
■ TEST CIRCUITS AND WAVEFORMS



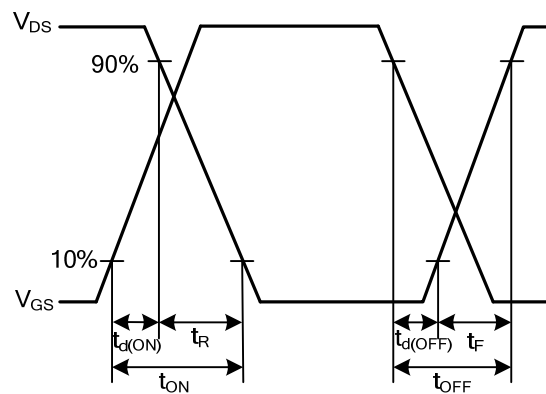
Gate Charge Test Circuit



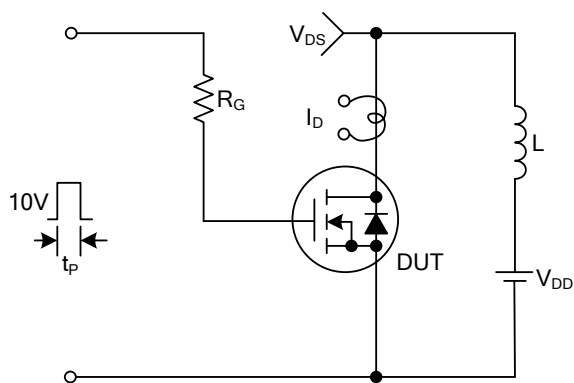
Gate Charge Waveforms



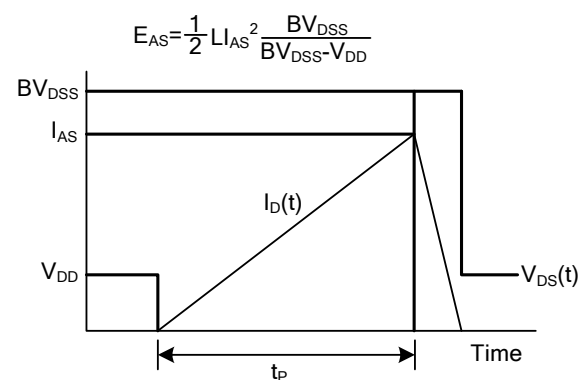
Resistive Switching Test Circuit



Resistive Switching Waveforms

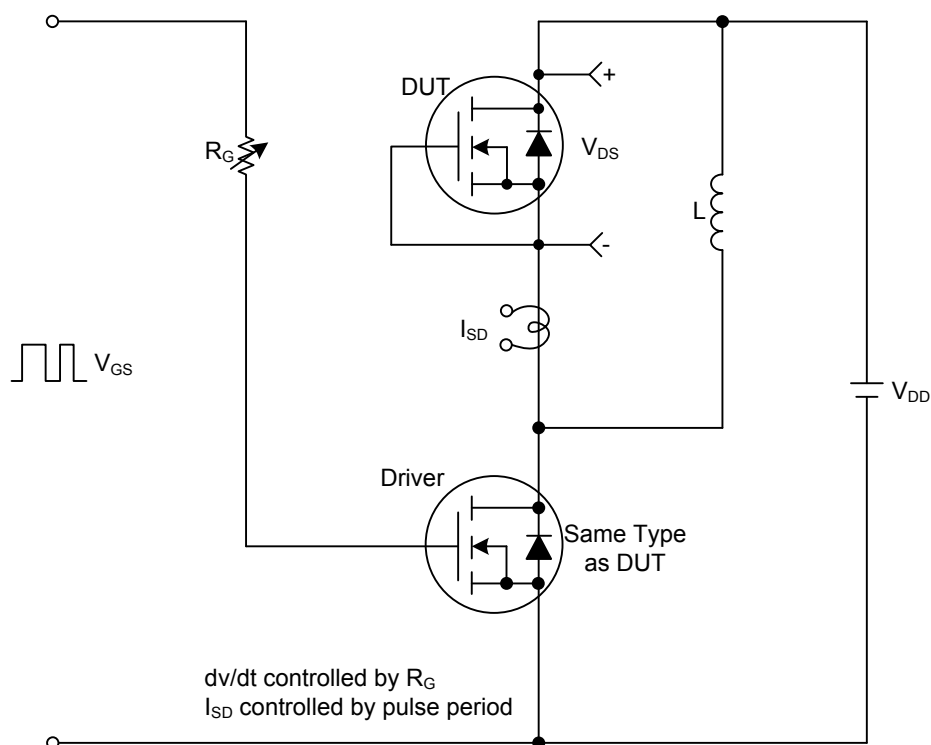


Unclamped Inductive Switching Test Circuit

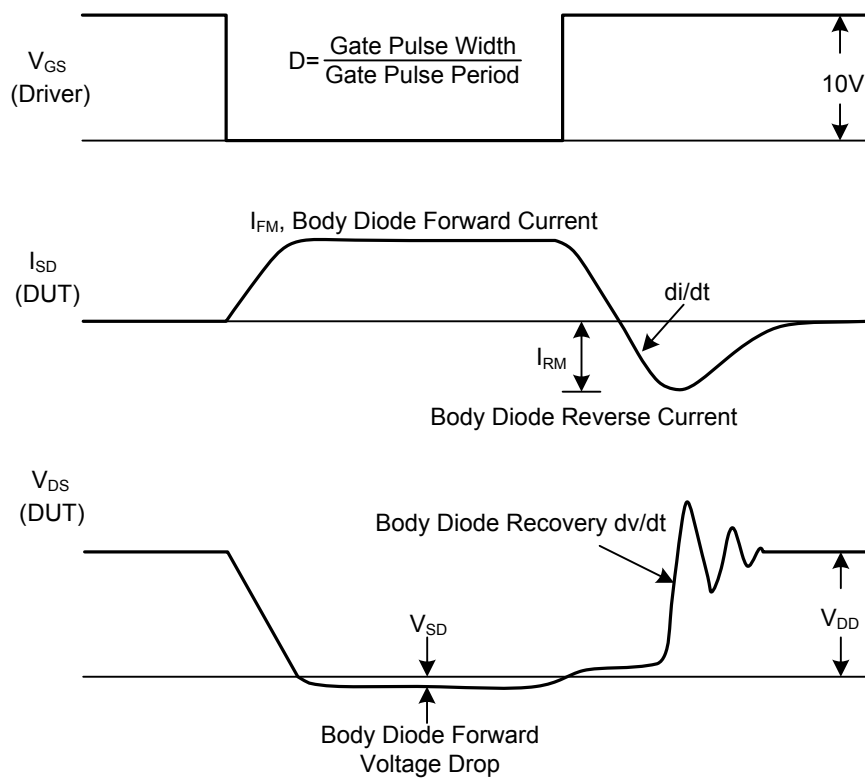


Unclamped Inductive Switching Waveforms

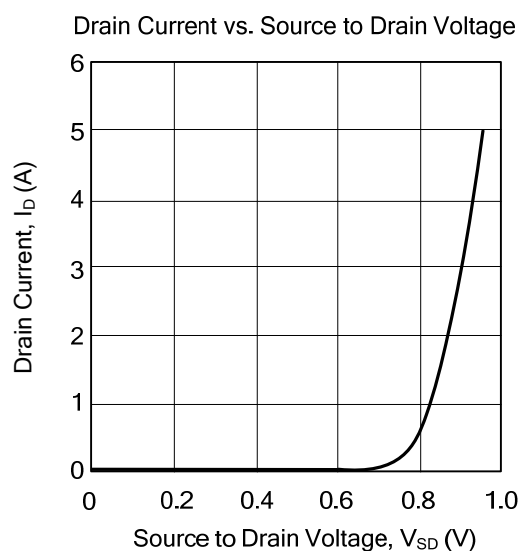
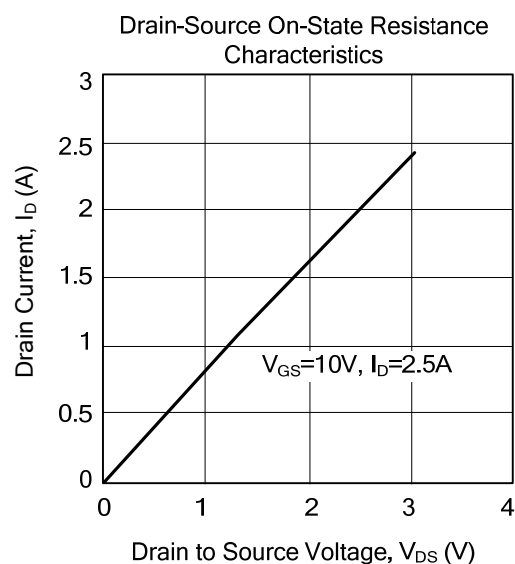
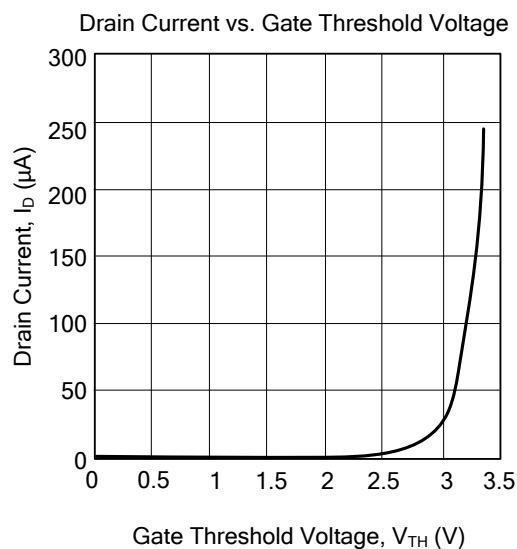
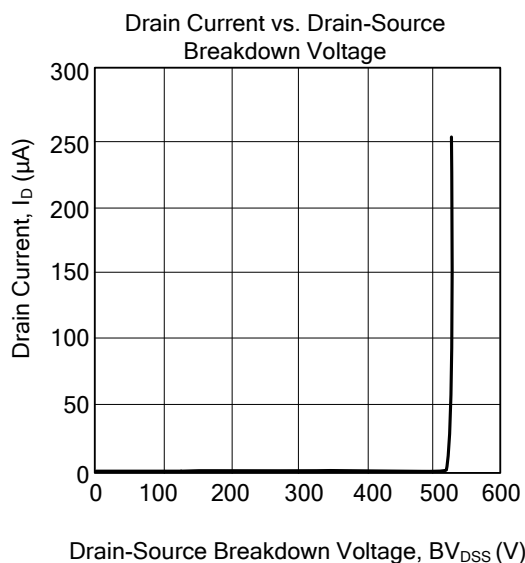
■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms



■ TYPICAL CHARACTERISTICS



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