HEWLETT PACKARD

MGA-66100 2-6 GHz Cascadable GaAs MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Broadband Performance: 2-6 GHz**
  12.5 dB Typical Gain
  ±1.0 dB Gain Flatness
  13.0 dBm P_{1dB}
- **Single Supply Bias**
- **Unconditionally Stable**

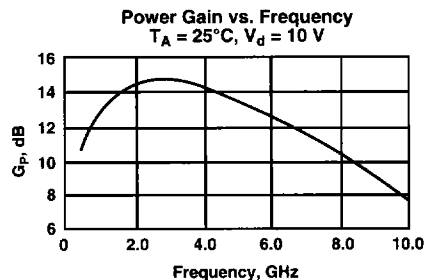
Description

The MGA-66100 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip. This device is designed for use as a general purpose 50 Ω gain block in the 2 to 6 GHz frequency range. Typical applications include narrow and broadband IF and RF amplifiers for commercial, industrial, and military requirements.

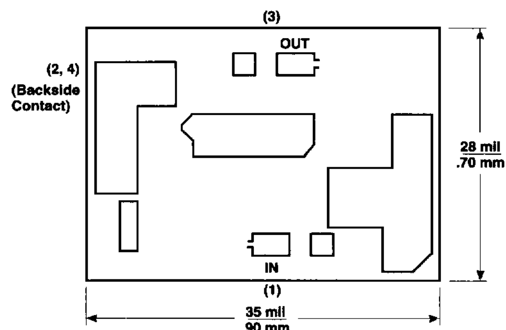
This MMIC is a cascade of two stages, each utilizing shunt feedback to establish a broadband impedance match. The source of each stage is AC grounded to allow biasing from a single positive power supply. The interstage blocking capacitor as well as a resistive "self-bias" network are included on chip.

The die is fabricated using HP's nominal .5 micron recessed Schottky-barrier-gate, gold metallization and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

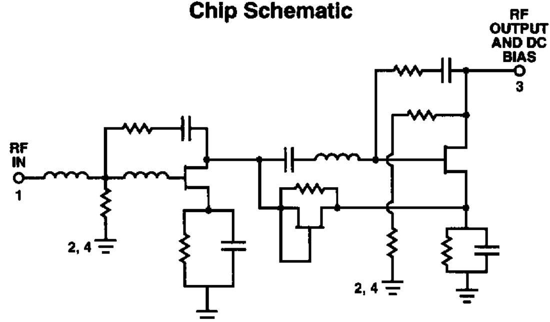
Power Gain vs. Frequency
$T_A = 25°C, V_d = 10$ V



Chip Outline



Chip Schematic



Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions: $V_d = 10$ V, $Z_O = 50$ Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\lvert S_{21}\rvert^2$)	f = 2 to 6 GHz	dB	10.0	12.5	
ΔG_P	Gain Flatness	f = 2 to 6 GHz	dB		±1.0	
—	Gain Variation vs. Temperature $T_{CASE} = -25°C$ to $+85°C$	f = 2 to 6 GHz	dB		±0.5	
VSWR	Input VSWR	f = 2 to 6 GHz			1.4:1	2.0:1
	Output VSWR	f = 2 to 6 GHz			1.4:1	2.0:1
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 2 to 6 GHz	dBm	10.0	13.0	
NF	50 Ω Noise Figure	f = 2 to 6 GHz	dB		7.5	
—	Reverse Isolation ($\lvert S_{12}\rvert^2$)	f = 2 to 6 GHz	dB		35	
I_d	Device Current		mA	35	50	65

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	12 V
Total Power Dissipation[2, 3]	800 mW
CW RF Input Power	+13 dBm
Channel Temperature	175°C
Storage Temperature	-65 to 175°C

Thermal Resistance: θ_{jc} = 40°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1µm spot size[4]

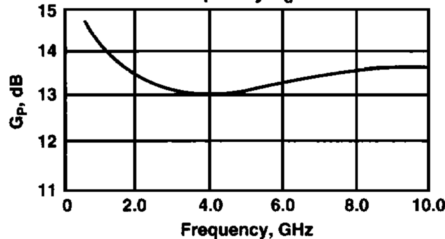
Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate linearly at 25 mW/°C for $T_{MOUNTING\ SURFACE}$ > 143°C.
4. The small spot size of the technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See Primer IIIA for more information.

Part Number Ordering Information

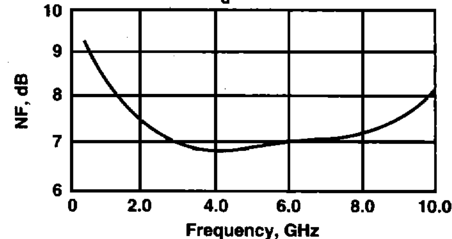
Part Number	Devices Per Tray
MGA-66100-GP1	5
MGA-66100-GP3	50
MGA-66100-GP6	Up to 300

Typical Performance, T_A = 25°C
(Unless otherwise noted)

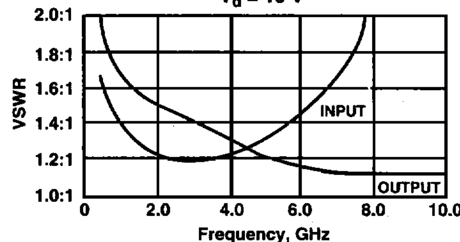
Output Power @ 1 dB Gain Compression vs. Frequency V_d = 10 V



Noise Figure vs. Frequency V_d = 10 V



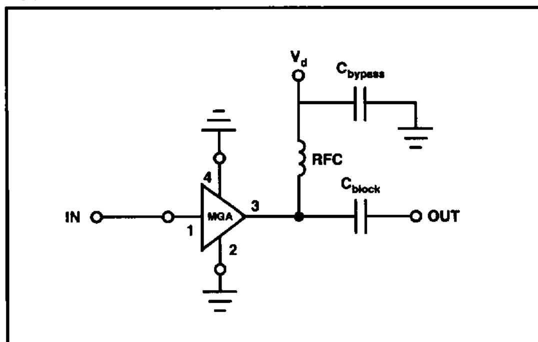
VSWR vs. Frequency V_d = 10 V



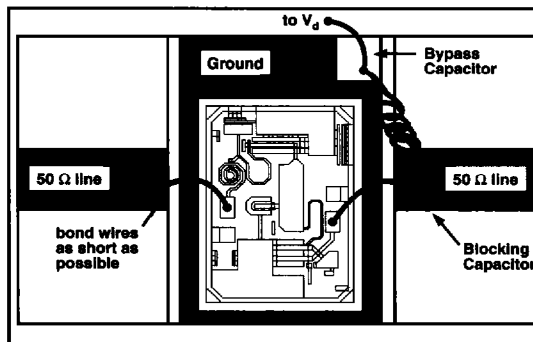
Typical Scattering Parameters: Z_O = 50 Ω T_A = 25°C, V_d = 10 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.25	39	10.2	3.23	14	-29.8	.032	-8	.36	-41
1.0	.16	36	12.3	4.12	-2	-32.0	.025	-17	.25	-45
2.0	.10	-22	14.1	5.06	-40	-34.2	.019	-14	.19	-46
3.0	.08	-37	14.5	5.28	-74	-35.9	.016	-11	.16	-54
4.0	.09	-105	14.2	5.15	-109	-38.0	.013	-9	.12	-65
5.0	.14	-152	13.5	4.71	-142	-40.9	.009	2	.09	-77
6.0	.20	176	12.4	4.19	-172	-44.3	.006	18	.07	-69
7.0	.27	141	11.3	3.67	160	-45.5	.005	54	.07	-48
8.0	.37	114	10.1	3.21	135	-45.0	.006	67	.07	-28
9.0	.50	96	8.7	2.73	111	-46.5	.005	90	.05	-10
10.0	.59	86	7.4	2.34	90	-46.8	.005	100	.03	7

Typical Biasing Configuration



Substrate Bonding Diagram



External Elements Required:
- Output DC Blocking Capacitor: 45 pF typical
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF typical
- Input and Output RF Transmission Lines: 50 Ω typical

Recommended Die Attach Procedure

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300° ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5-15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pick up the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

Recommended Wedge Bonding Procedure

1. Set heater block temperature to 260° ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads if the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.