



STD18N55M5 STF18N55M5, STP18N55M5

N-channel 550 V, 0.18 Ω, 14 A, MDmesh™ V Power MOSFET
in DPAK, TO-220FP and TO-220

Preliminary data

Features

Type	V _{DSS} @T _{Jmax}	R _{DS(on)} max	I _D
STD18N55M5			
STF18N55M5	600 V	< 0.21 Ω	14 A
STP18N55M5			

- DPAK worldwide best R_{DS(on)}
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

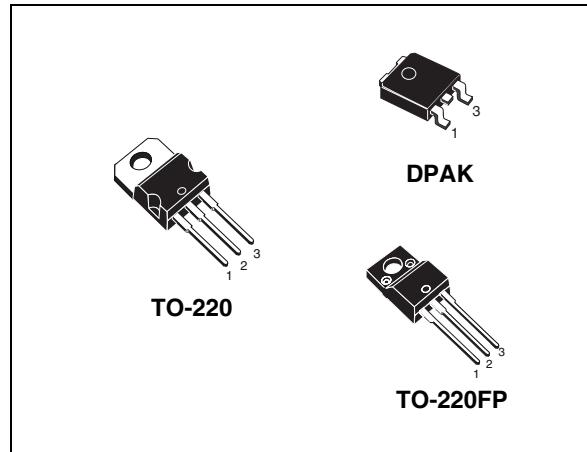
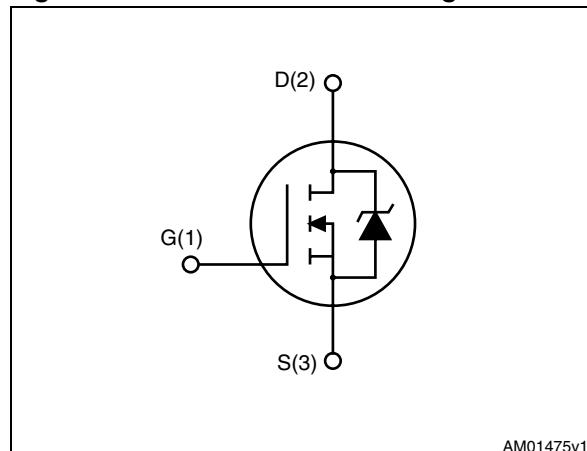


Figure 1. Internal schematic diagram



Application

- Switching applications

Description

MDmesh™ V is a revolutionary Power MOSFET technology based on an innovative proprietary vertical process, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD18N55M5	18N55M5	DPAK	Tape and reel
STF18N55M5		TO-220FP	
STP18N55M5		TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK	TO-220FP	
V_{GS}	Gate-source voltage	25		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	14	14 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	9	9 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	56	56 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	90	25	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_j max)	TBD		A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50$ V)	TBD		mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	14		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1$ s; $T_c = 25^\circ\text{C}$)		2500	V
T_{stg}	Storage temperature	- 55 to 50		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 14$ A, $di/dt \leq 100$ A/ μs , $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.39	5	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	62.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50			°C/W
T_I	Maximum lead temperature for soldering purpose	300			°C

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	550			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$		0.18	0.21	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			TBD		pF
C_{oss}	Output capacitance		-	TBD	-	pF
C_{rss}	Reverse transfer capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	TBD	-	pF
$C_{o(\text{tr})}^{(1)}$	Equivalent capacitance time related		-	TBD	-	pF
$C_{o(\text{er})}^{(2)}$	Equivalent capacitance energy related	$V_{DS} = 0, V_{GS} = 0$	-	TBD	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	TBD	-	Ω
Q_g	Total gate charge	$V_{DD} = 440 \text{ V}, I_D = 7 \text{ A}, V_{GS} = 10 \text{ V}$		TBD		nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge	(see Figure 3)		TBD	-	nC

1. $C_{oss\text{ eq}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\text{ eq}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 225 \text{ V}$, $I_D = 3.5 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 2 , Figure 7)	-	TBD	-	ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off-delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current		-		14	A
	Source-drain current (pulsed)				56	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 14 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time	$I_{SD} = 14 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ (see Figure 4)	-	TBD		ns
	Reverse recovery charge			TBD		nC
	Reverse recovery current			TBD		A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time	$I_{SD} = 14 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$, $T_j = 150^\circ\text{C}$ (see Figure 4)	-	TBD		ns
	Reverse recovery charge			TBD		nC
	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

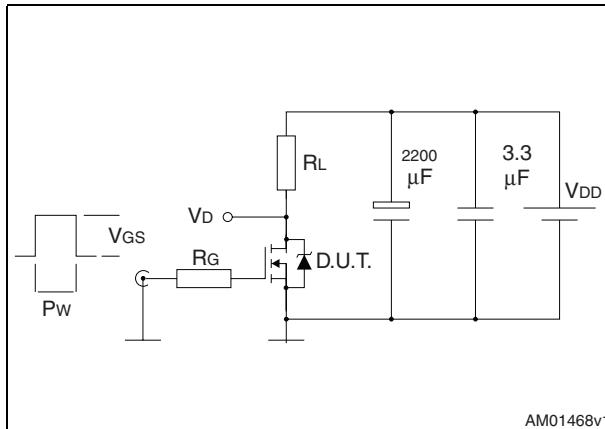


Figure 3. Gate charge test circuit

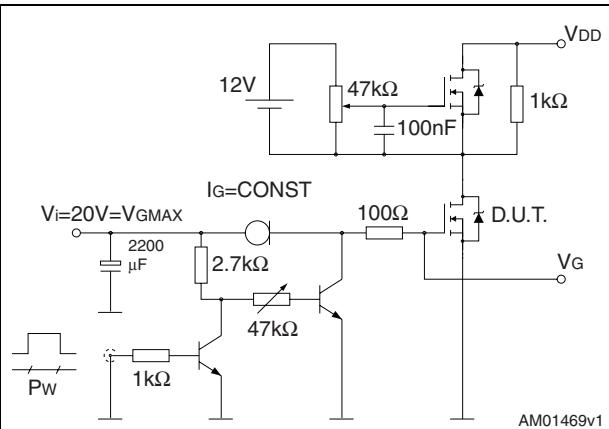


Figure 4. Test circuit for inductive load switching and diode recovery times

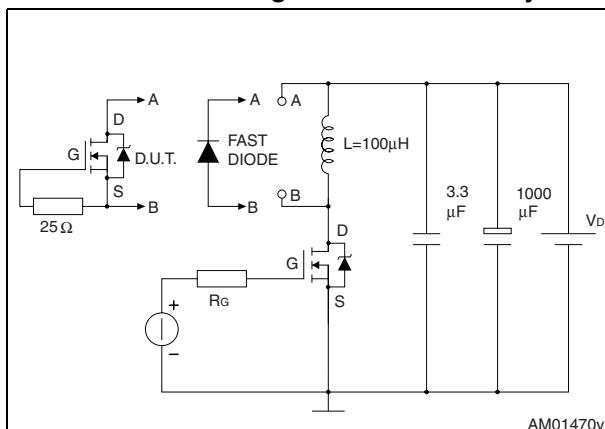


Figure 5. Unclamped inductive load test circuit

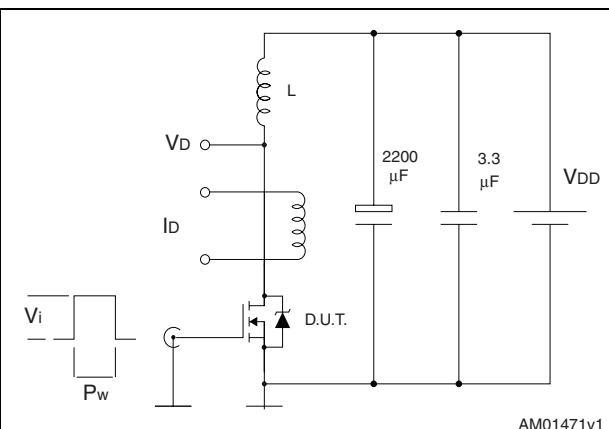


Figure 6. Unclamped inductive waveform

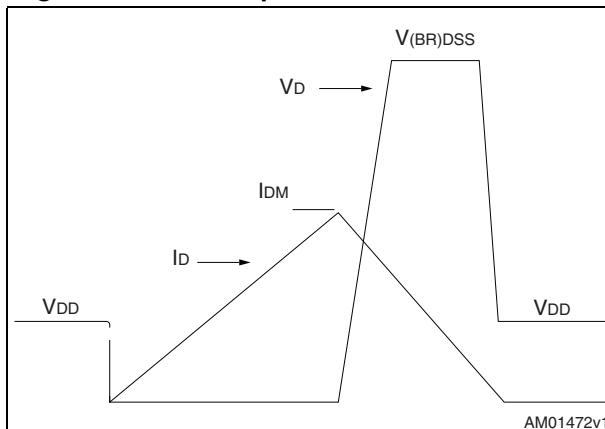
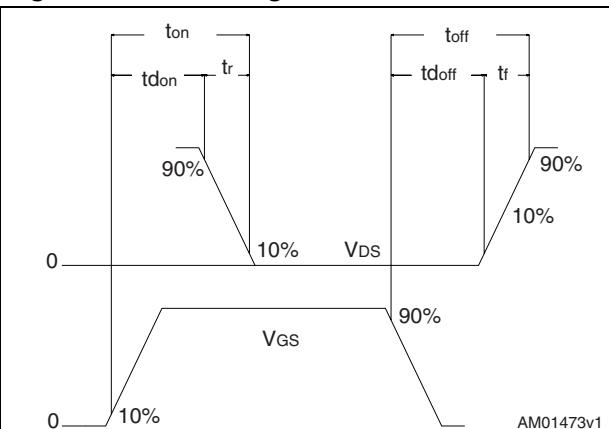


Figure 7. Switching time waveform

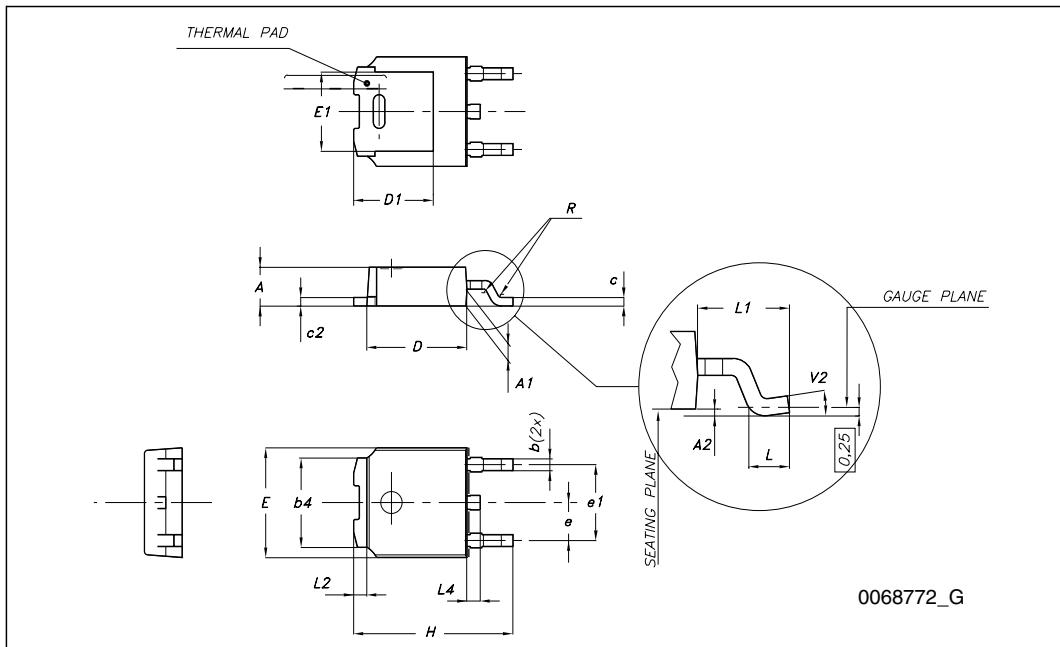


4 Package mechanical data

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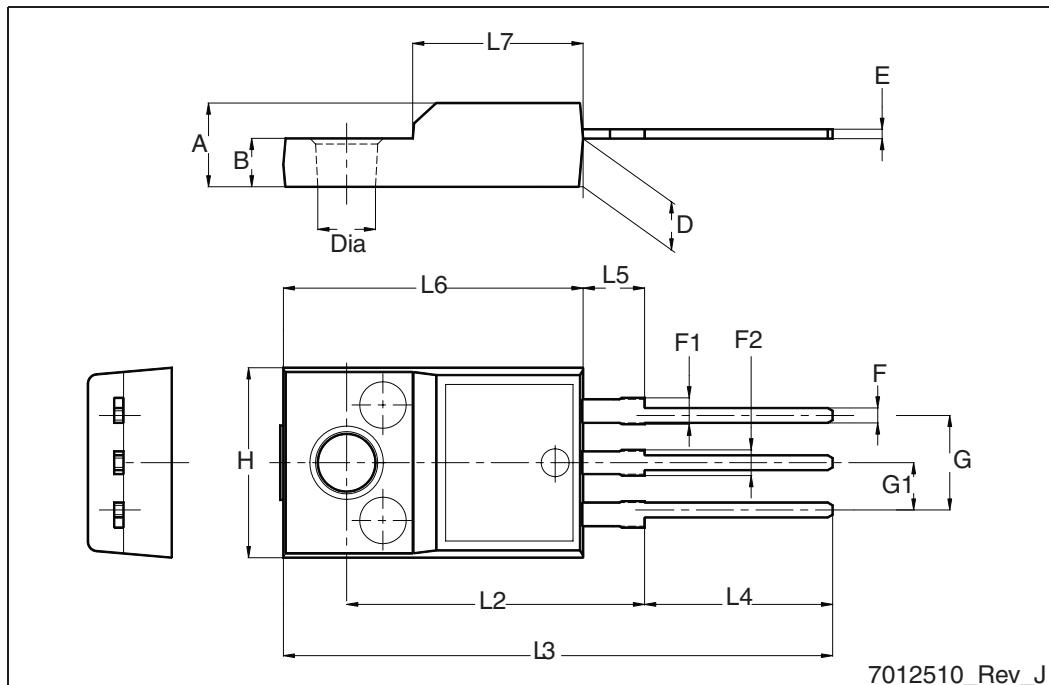
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



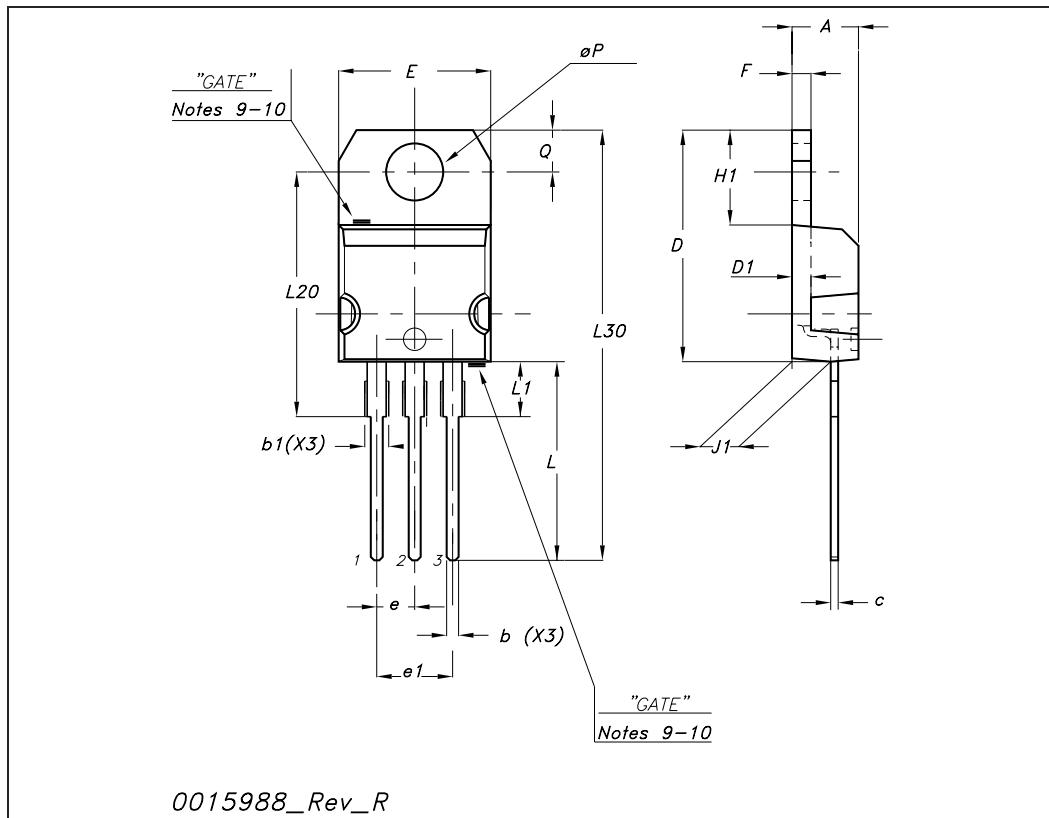
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



TO-220 mechanical data

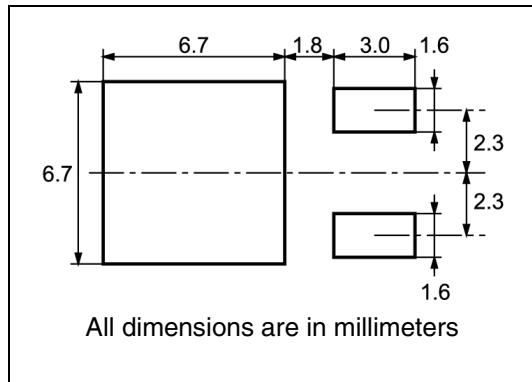
Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
$\emptyset P$	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



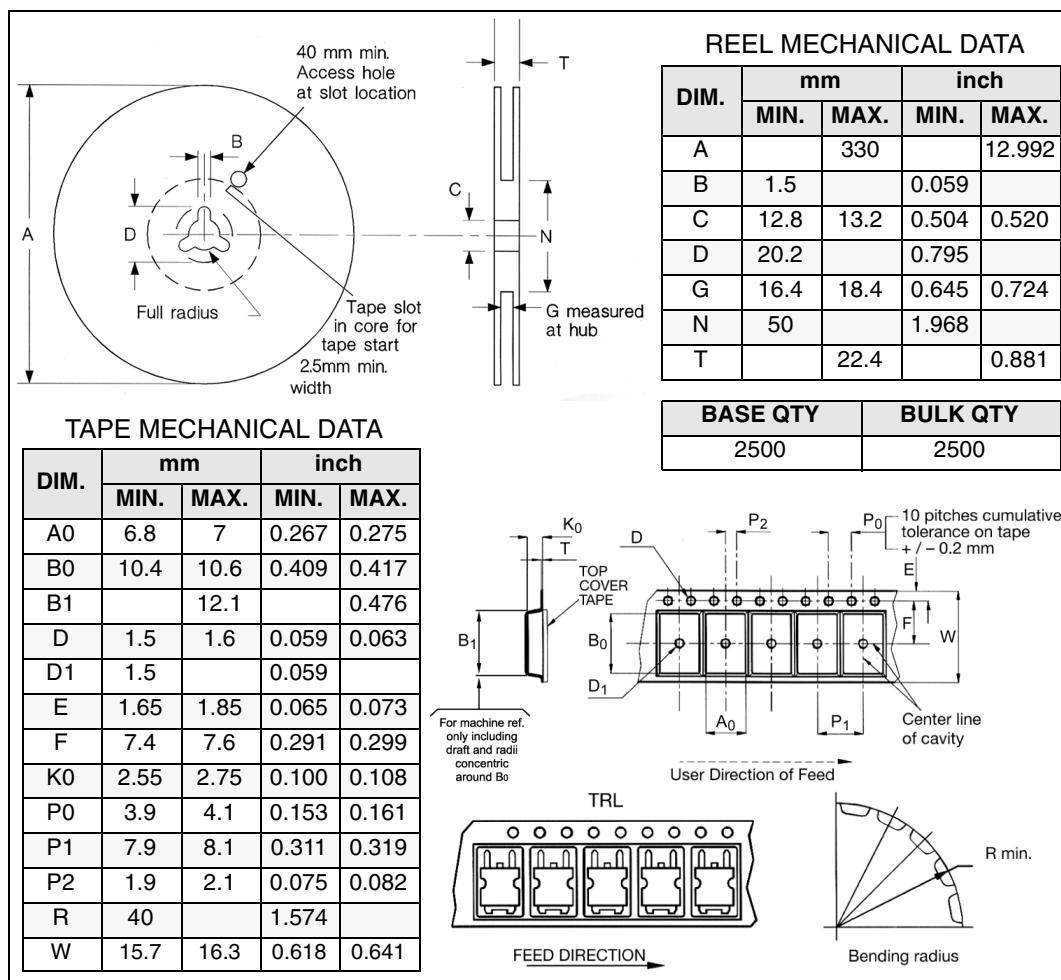
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5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
09-Feb-2010	1	First release

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