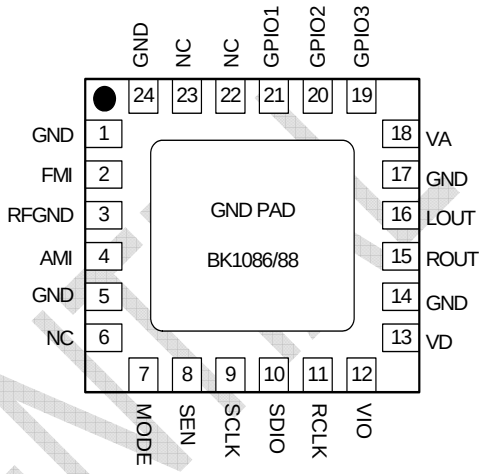
BK1086/88

BROADCAST AM/FM/SW/LW RADIO RECEIVER

Features

- Worldwide 64~108 MHz FM band support
- Worldwide 520~1710kHz AM band support
- SW band support(2.3-21.85MHz, BK1088 only)
- LW band support(153-279kHz,BK1088 only)
- Automatic gain control(AGC)
- Automatic frequency control(AFC)
- Digital FM stereo decoder
- Automatic FM stereo/mono blend
- Automatic noise suppression
- 50us/75us de-emphasis
- RDS/RBDS decoder
- 2.4 ~ 5.5 V supply voltage
- Wide range reference clock support
- 32.768KHz crystal oscillator
- 4x4 mm 24-pin QFN package



QFN 24 Pin Assignments (Top View)

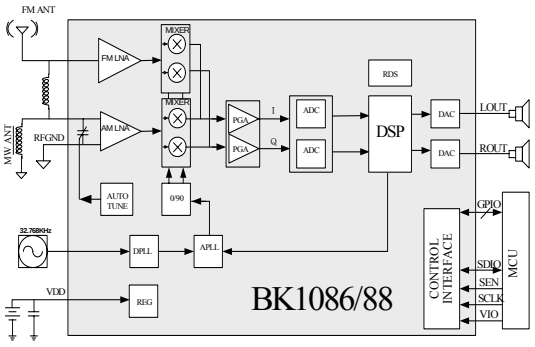
Applications

- Table and portable radios
- CD/DVD players
- Modules

General Description

The BK1086/88 AM/FM receiver employs a low-IF architecture, mixed signal image rejection and all digital demodulation technology. The station scan of BK1086/88 searches radio stations based on both the channel RSSI estimation and signal quality assessment, increases the number of receivable stations while avoids false stops. BK1086/88 enables FM/AM/SW/LW radio reception with low power, small board space and minimum number of external component.

Functional Block Diagram



1 Table of Contents

2 Functional Description

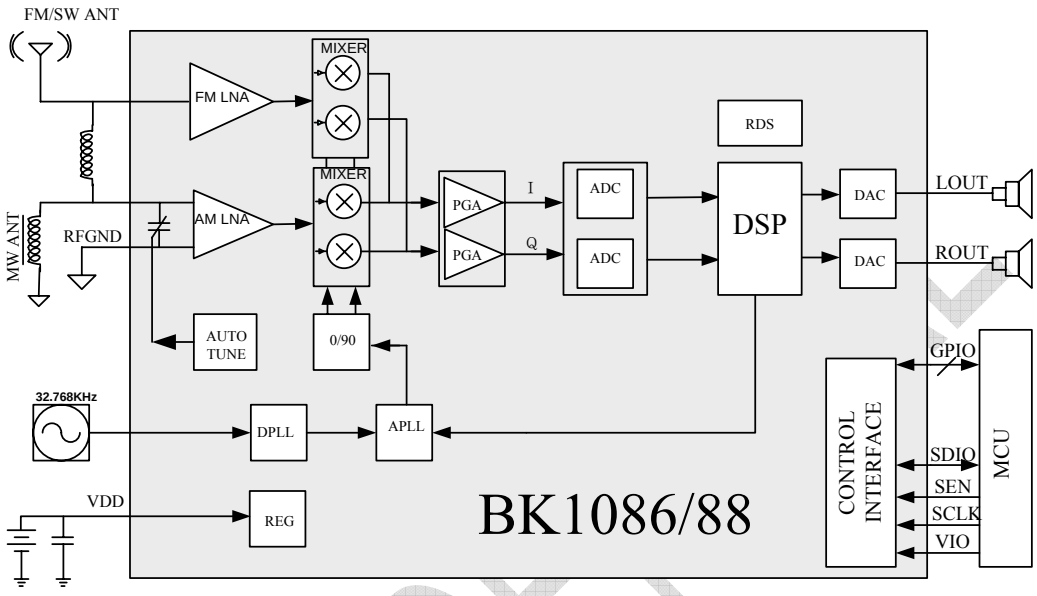


Figure1. Functional Block Diagram

2.1 FM Receiver

The receiver employs a digital low-IF architecture that reduces external components, and integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (64 to 108MHz), an automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers, an image-reject mixer down converts the RF signal to low-IF, The mixer output is amplified by a programmable gain control (PGA), and digitized by a high resolution analog-to-digital converters (ADCs). An audio DSP finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

2.2 AM Receiver

BK1086/88 supports worldwide AM band reception by a digital low-IF architecture with minimum number of external components. This architecture allows for high-precision filtering, offering excellent selectivity and noise suppression. Similar to the FM receiver, the integrated LNA and AGC optimize sensitivity and rejection of strong interferers allowing better reception of weak stations. The BK1086/88 provides highly accurate digital AM tuning without factory adjustments. To offer maximum flexibility, the receiver supports a wide range of ferrite loop sticks from 180–600 µH for MW band..

2.3 Interface Bus

The BK1086/88 supports 3-wire and I^{2}C control interface, with up to 2.5 MHz clock speed. User could select either of them by setting the state of MODE pin. BK1086/88 will use I2C interface for MODE=0 or 3-wire interface for MODE =1.

BK1086/88 always latches data at the SCLK rising edge and outputs its data at SCLK falling edge. For MCU, data should be always written at the falling edge of SCLK, and read out at the rising edge of SCLK.

2.3.1 3-wire bus mode

When selecting 3-wire mode, user must set MODE = 1. 3-wire bus mode uses SCLK, SDIO and SEN pins. A transaction begins when user drives SEN Low. Next, user drives an 8-bit command serially on SDIO, which is captured by BK1086/88 on rising edges of SCLK. The command consists of a 7-bit start register address, followed by a read/write bit (read = 1, write = 0).

2.3.2 I2C bus mode

When selecting I2C mode, user must set MODE = 0.

I2C bus mode only uses SCLK and SDIO pins. A transaction begins with the start condition, which occurs when SDIO falls while SCLK is high. Next, user drivers an 8-bit device ID serially on SDIO, which is captured by BK1086/88 at the rising edge of SCLK. The device ID of BK1086/88 is 0x80.

After driving the device ID, user drives an 8-bit control word on SDIO. The control word consists of a 7-bit start register address, followed by a read/write bit (read = 1, write = 0).

For I2C host reading, the host must give an ACK to BK1086/88 after each byte access, and should give a NACK to BK1086/88 after last byte read out. For stable communication, the rising edge time of SCLK should be less than 200ns.

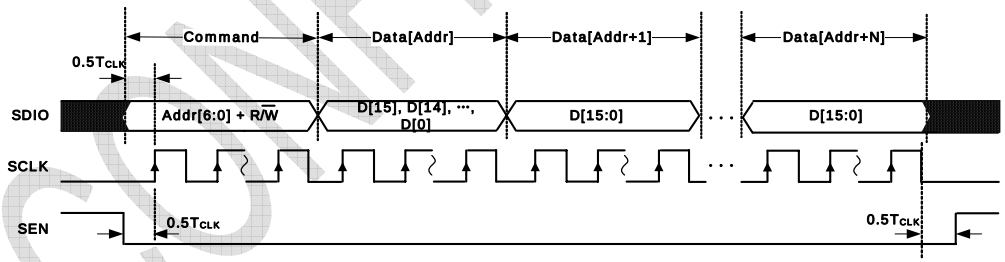


Figure 2. 3-Wire Interface Diagram

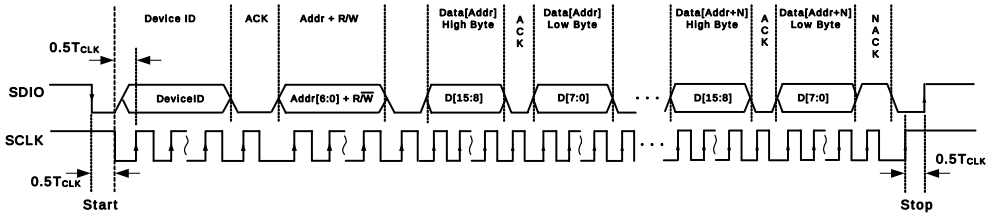


Figure 3. I2C Interface Diagram

2.4 Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS data.

The BK1086/88 has integrated stereo decoder automatically decodes the MPX signal. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L-R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L-R) signal. Separate left and right channels are obtained by adding and subtracting the (L+R) and (L-R) signals, respectively. Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. The signal level range over which the stereo to mono blending occurs can be adjusted by setting the BLNDADJ [1:0] register. Stereo/mono status can be monitored with the ST register bit and mono operation can be forced with the MONO register bit and stereo operation can be forced with the STEREO register bit.

BK1086/88 uses pre-emphasis and de-emphasis to improve the signal-to-noise ratio of FM receivers by reducing the effects of high frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants, 50 or 75μs, are used in various regions. The de-emphasis time constant is programmable with the DE bit. High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted with the DMUTE bit. Volume can be adjusted digitally with the VOLUME [4:0] bits. The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The soft mute attack and decay rate can be adjusted with the SMUTER [1:0] bits where 00 is the fastest setting. The soft mute attenuation level can be adjusted with the SMUTEA [1:0] bits where 00 is the most attenuated. The soft mute disable (DSMUTE) bit may be set high to disable this feature.

2.5 Seek/Tune System

In FM mode, channel spacing of 10， 50, 100 or 200 kHz is selected with bits SPACE [1:0]. The channel is selected with bits CHAN [14:0]. The bottom of the band is set to 64 MHz, 76 MHz or 87 MHz with the bits BAND [1:0]. The tuning operation begins by setting the TUNE bit. After tuning completes, the seek/tune complete (STC) bit will be set and the RSSI level is available by reading bits RSSI [6:0]. The TUNE bit must be set low after the STC bit is set high in order to prepare for the next tune operation and clear the STC bit. Seek tuning searches up or down for a channel with RSSI greater than the seek threshold set with the SEEKTH [6:0] bits and SNR greater than the SNR threshold set with the SKSNR [6:0] bits.

In addition, an optional AFCRL and/or impulse noise detector may be used to qualify valid stations. The AFCRL detector is set by SKAFCRL and the SKCNT [3:0] bits set the impulse noise threshold. Using the extra seek qualifiers can reduce false stops and, in combination with lowering the RSSI seek threshold, increase the number of found stations. Two seek modes are available. If the seek mode (SKMODE) bit is low when seeking process is initiated, the device seeks through the band, wraps from one band edge to the other, and continues seeking. If the seek operation was unable to find a channel, the seek failure/band limit (SF/BL) bit will be set high and the device will return to the channel selected before the seek operation began. If the SKMODE bit is high when seeking process is initiated, the device seeks through the band until the band limit is reached and the SF/BL bit will be set high. A seek operation is initiated by setting the SEEKUP and SEEK bits. After the seek operation completes, the STC bit will be set, and the RSSI level as well as the tuned channel number are available by reading bits RSSI [7:0] and bits READCHAN [14:0]. During a seek operation READCHAN [14:0] is also updated and may be read to supervise the seeking progress. The STC bit is set after the seek operation completes. The channel is valid if the seek operation completes and the SF/BL bit is set low. Note that if the AFCRL bit is set or the SNR and RSSI are lower than the thresholds, the audio output is muted as in the soft mute case discussed in stereo audio processing section. The SEEK bit should be set low after the STC bit is set high in order to prepare for the next seek operation as well as clearing the STC and SF/BL bits. The seek operation may be aborted by setting the SEEK bit low at any time. The device can be configured to generate an interrupt on GPIO2 when a tune or seek operation completes. Setting the seek/tune complete (STCIEN) bit and GPIO2 [1:0] = 01 will configure GPIO2 for a 5 ms low interrupt when the STC bit is set by the device.

The AM mode tuning system algorithm is same as FM mod

2.6 GPIO output

The BK1086/88 has three GPIO pins. The function of GPIO pins could be programmed with bits GPIO1 [1:0], GPIO2 [1:0], GPIO3 [1:0], GPIO2/3 pins can be used as interrupt request pins for the seek/tune or RDS ready functions and as a stereo/mono indicator respectively.

GPIO functionality is available regardless of the state of the VA and VD supplies, or the ENABLE and DISABLE bits.

2.7 RDS Processor

The BK1086/88 implements an RDS processor for symbol decoding, block synchronization, error detection, and error correction. Set the RDSEN=1 will enable RDS reception, and set RDSDEC=1 will enable automatic error correction. After error check and processing, if a correct RDS frame is received, the received block will be placed at RDSA, RDSB, RDSC and RDSD registers and RDS ready bit RDSR will be set. When RDSIEN is enabled, a 5 ms active low interrupt will be issued on GPIO2.

2.8 Reference Clock

The BK1086/88 accepts wide range, from 32.768 kHz to 38.4 MHz, reference clock input to the RCLK pin. For frequency less than 4 MHz, it must be multiplier of 32.768 KHz. The BK1086/88 also support 32.768KHz crystal oscillator. Low quality reference clock with 200ppm is acceptable.

2.9 Initialization Sequence

To initialize BK1086/88:

1. Supply VIO.
2. Supply VA and VD. Note that VA and VD could be supplied at the same time of VIO supplied.
3. Provide RCLK.
4. Set the ENABLE bit high and the DISABLE bit low to power up BK1086/88.

To power down BK1086/88:

1. Set the ENABLE bit high and the DISABLE bit high to place BK1086/88 in power down mode. Note that all register states are maintained as long as VIO is supplied.
2. (Optional) Remove RCLK.
3. Remove VA and VD as needed.

To power up BK1086/88 (after power down):

1. Note that VIO is still supplied in this scenario. If VIO is not supplied, refer to BK1086/88 initialization procedure above.
2. Supply VA and VD.
3. Provide RCLK.
4. Set the ENABLE bit high and the DISABLE bit low to power up BK1086/88.
5.

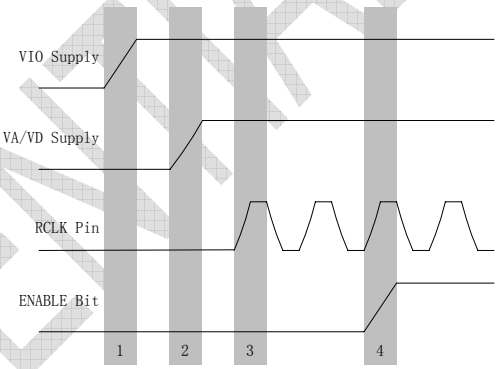


Figure 4 Initialization Sequence

3 Design Specification

3.1 Recommended Operating Conditions

Table 1 Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage	V_D		2.4	—	5.5	V
Analog Supply Voltage	V_A		2.4	—	5.5	V
Interface Supply Voltage	V_{IO}		1.6	—	3.6	V
Ambient Temperature	T_A		–20	25	85	°C
Notes: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_D = V_A = 3.3$ V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.						

3.2 Power Consumption Specification

Table 2 Power Consumption Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current (FM Mode)	I_S	ENABLE = 1 DISABLE = 0	—	25	27	mA
Supply Current (AM Mode)	I_S	ENABLE = 1 DISABLE = 0	—	24	26	mA
Power down Current	I_{PD}	ENABLE = 0 DISABLE = 1	—	10	20	µA
Interface Power down Current	Ip_{IO}	SCLK, RCLK inactive ENABLE = 0	—	1.9	5	µA

3.3 Receiver Characteristics

Table 3 FM Receiver Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Input Frequency		64	—	108	MHz
Sensitivity[2,3,4,5,6]	(S+N)/N = 26 dB	—	1.7	2.2	µV EMF
LNA Input Resistance[7]		2.5	3	3.5	kΩ
Input IP3[8]		—	92	—	dBµV EMF
AM Suppression[2, 3, 4, 5, 7]	m = 0.3	40	45	—	dB
Adjacent Channel Selectivity	±200 kHz	35	45	—	dB
Alternate Channel Selectivity	±400 kHz	50	60	—	dB
Audio Output Voltage[2, 3, 4, 7]		—	100	—	mV RMS
Audio Stereo Separation[2, 4, 5, 7]		30	—	—	dB
Audio S/N[2, 3, 4, 5, 7,]			55	—	dB
Audio THD[2, 3, 5, 7, 10]		—	0.1	0.3	%
De-emphasis Time Constant [11]			50	75	µs
Audio Common Mode Voltage[12]	ENABLE = 1	0.8	0.9	1.0	V
Audio Output Load Resistance	Single-ended	—	32	—	Ω
Seek/Tune Time		—	—	60	ms/channel
RSSI Offset	Input levels of 8 and 50 dBµV at RF input	–3	—	3	dB

Notes:

1. Volume = maximum for all tests
2. F_{MOD} = 1 kHz, 75 µs de-emphasis
3. MONO = 1, and L = R unless noted otherwise
4. Δf = 22.5 kHz
5. B_{AF} = 300 Hz to 15 kHz, A-weighted
6. Sensitivity without matching network
7. Measured at V_{EMF} = 1 mV, f_{RF} = 64 to 108 MHz
8. |f2 – f1| > 2 MHz, f0 = 2 x f1 – f2. AGC is disabled by setting AGCD = 1
9. The channel spacing is selected with the SPACE [1:0] bits
10. Δf = 75 kHz
11. The de-emphasis time constant is selected with the DE bit
12. At LOUT and ROUT pins

Table 4 AM Receiver Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency	Long Wave(AM)	153	—	279	kHz
	Medium Wave(AM)	520	—	1710	kHz
	Short Wave(SW)	2.3	—	21.85	MHz
Sensitivity[1,2,3]	(S+N)/N = 26 dB	—	20		μV EMF
Large Signal Voltage Handling			300		mV_{RMS}
Power Supply Rejection Ratio			40	—	dB
Audio Output Voltage		—	100	—	mV_{RMS}
Audio S/N[1,2,3,5]			55	—	dB
Audio THD[1,2,3,5]		—	0.1		%
Antenna Inductance	Medium Wave(AM)	180		600	uH
	Long Wave(LW)		2800		
Power Up Time	From power down		—	150	ms

Notes:

1. FMOD = 1kHz , 30%modulation , A-weighted , 2 kHz channel filter
2. B_{AF} = 300 Hz to 15 kHz, A-weighted
3. f_{RF} = 1000kHz
4. Guaranteed by characterization
5. V_{IN} = 5 mV_{RMS}

3.4 I2C Control Interface Characteristics

Table 4 I2C Control Interface Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		—	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6			µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold	$t_{HD:DAT}$		—	—	900	ns
SCLK Input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		—	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		—	—	200	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	60	pF
Input Filter Pulse Suppression	t_{SP}		—	—	40	ns

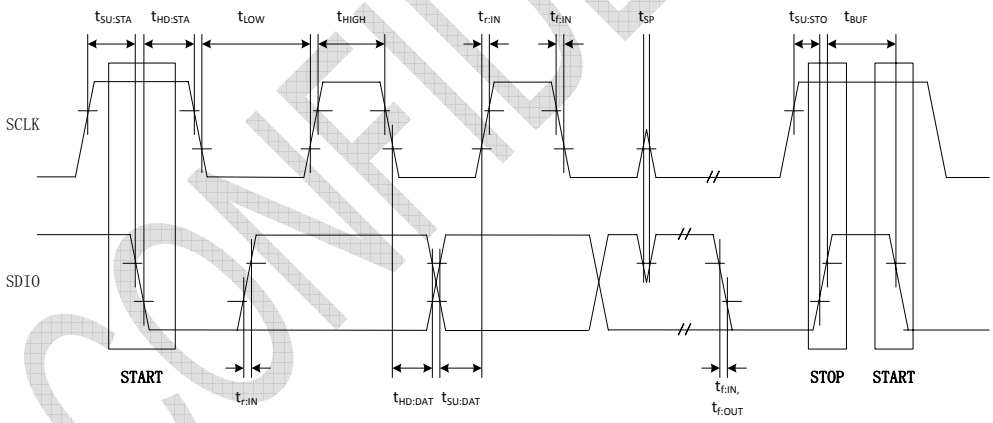


Figure 5 I2C Control Interface Read and Write Timing Diagram

3.5 3-Wire Control Interface Characteristics

Table 5 3-Wire Control Interface Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, SEN to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
SEN Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, SEN, SDIO, Rise/Fall Time	t_R , t_F		—	—	10	ns

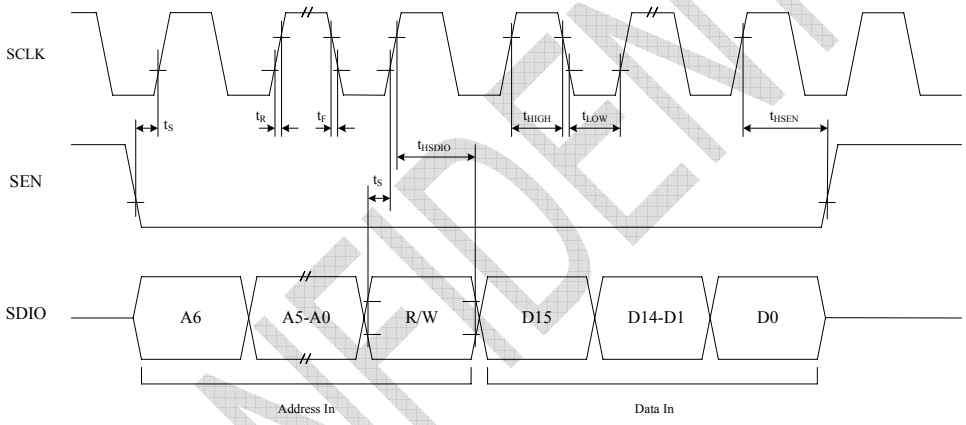


Figure 6 3-Wire Control Interface Write Timing Diagram

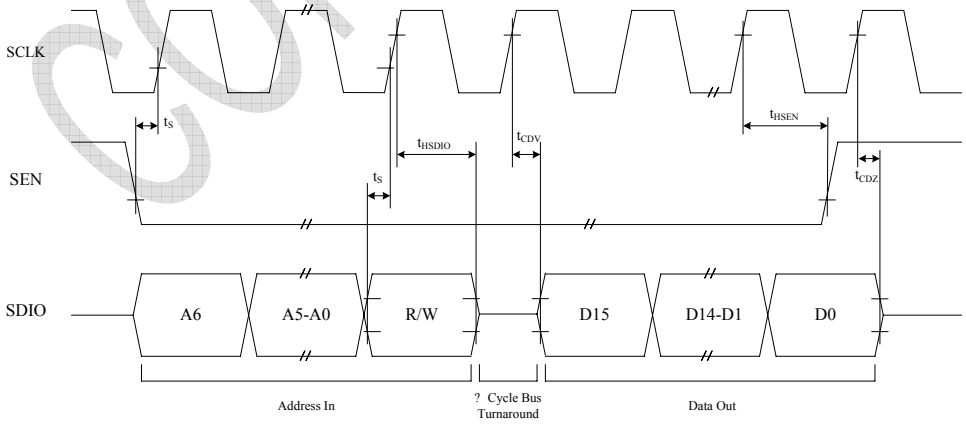


Figure 7 3-Wire Control Interface Read Timing Diagram

4 Register Definition

Register 00h. Device ID (0x8040)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	DEVID[15:0]	16'h8040	Device ID

Register 01h. Chip ID (0x1080)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	CHIPID[15:0]	16h'1080	Chip ID

Register 02h. Power Configuration (0x0280)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	DSMUTE	1'h0	Soft mute Disable. 0 = Soft mute enable. 1 = Soft mute disable.
[14]	MUTEL	1'h0	Mute L channel. 0 = L channel normal operation. 1 = L channel mute.
[13]	MUTER	1'h0	Mute L channel. 0 = R channel normal operation. 1 = R channel mute.
[12]	MONO	1'h0	Mono. 0 = Normal operation. 1 = Force mono.
[11]	STEREO	1'h0	Stereo 0 = Normal operation. 1 = Force stereo. MONO and STEREO cannot be set to 1 simultaneously.
[10]	SKMODE	1'h0	Seek Mode 0 = Wrap 1 = Stop at the upper or higher band limit
[9]	SEEKUP	1'h1	Seek Direction. 0 = Seek down.

			1 = Seek up.
[8]	SEEK	1'h0	Seek 0 = Disable 1 = Enable seek A pos edge can start the seek process and during it SEEK should be 1
[7]	SKAFCRL	1'h1	Seek with AFC Rail 0 = During seeking, the channel is valid no matter whether AFCRL is high or low. 1 = During seeking, the channel is invalid if AFCRL is high.
[6]	DISABLE	1'h0	Power up Disable 0 = Normal operation 1 = Power down
[5:1]	SNR_REF[4:0]	5'h0	Output SNR adjustment. Read SNR = SNR (calculated) – SNR_REF
[0]	ENABLE	1'h0	Power up Enable 0 = Power down 1 = Normal operation Note: Only DISABLE=0 and ENABLE=1 can power on the device

Register 03h. Channel (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	TUNE	1'h0	Tune 0 = Disable 1 = enable Note: a pos edge can start the tune process and during it TUNE must be 1 and SEEK must be 0
[14:0]	CHAN[14:0]	15'h0	Channel Select The tuned Frequency = Band + CHAN * SPACE

Register 04h. System Configuration1 (0x1180)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	RDSIEN	1'h0	RDS Interrupt Enable 0 = disable. 1 = enable. When register GPIO2[1:0]=2'b01 and new RDS come, a 5ms low pulse will appear at GPIO2
[14]	STCIEN	1'h0	Seek/Tune Complete Interrupt Enable 0 = disable. 1 = enable. When register GPIO2[1:0]=2'b01 and seek or tune finish, a 5ms low pulse will appear at GPIO2 .Both RDSIEN and STCIEN can be high

[13]	AFCINV	1'h0	AFC Invert 0 = Normal AFC into mixer 1 = Reverse AFC into mixer
[12]	RDSEN	1'h1	RDS Enable 0 = Disable RDS. 1 = Enable RDS
[11]	DE	1'h0	De-emphesisi 0 = 75us 1 = 50us
[10:9]	TCPILOT	2'h0	The Time Used to Cal The Strength of Pilot 00:4ms 01:8ms 10:16ms 11:32ms
[8:6]	BLNDADJ [2:0]	3'h3	Stereo/Mono Blend Level Adjustment. 000 = 31–49 RSSI (0 dBuV) 001 = 34–52 RSSI (+3 dBuV) 010 = 37–55 RSSI (+6 dBuV) 011 = 40–58 RSSI (+9 dBuV) 100 = 31–49 RSSI (0 dBuV) 101 = 28–46 RSSI (-3 dBuV) 110 = 25–43 RSSI (-6 dBuV) 111 = 22–40 RSSI (-9 dBuV)
[5:4]	GPIO3[1:0]	2'h0	General Purpose I/O 3. 00 = High impedance 01 = Mono/Stereo indicator (ST) 10 = Low 11 = High
[3:2]	GPIO2[1:0]	2'h0	General Purpose I/O 3. 00 = High impedance 01 = STC/RDS interrupt. 10 = Low 11 = High
[1:0]	GPIO1[1:0]	2'h0	General Purpose I/O 3. 00 = High impedance 01 = CLK38MHz 10 = Low 11 = High

Register 05h. System Configuration2 (0x3ddf)

BIT	NAME	DEFAULT	DESCRIPTION
[15:9]	SEEKTH [6:0]	7'h1e	RSSI Seek Threshold
[8:7]	BAND[1:0]	2'h3	Band Select AM: 00: LW 153~279e3 FM:00: FULL 64~108e6 10: MW 520~1710e3 01: East Europe 64~76e6 10: SW 2.3~21.85e6 10: Japan 76~91e6 11: MW 522~1710e3 11: Europe 87~108e6 (LW and SW Band are only defined at BK1088)
[6:5]	SPACE[1:0]	2'h2	Channel Spacing

			AM: 0: 1e3 FM: 0: 10e3 1: 5e3 1: 50e3 2: 9e3 2: 100e3 3: 10e3 3: 200e3
[4:0]	VOLUME [4:0]	5'h1f	Volume 0x00 is the lowest and 0x1F is highest (0dBFS). 2dB each

Register 06h. System Configuration3 (0x01ef)

BIT	NAME	DEFAULT	DESCRIPTION
[15:14]	SMUTER[1:0]	2'h0	Soft mute Attack/Recover Rate 00 = fastest 01 = fast 10 = slow 11= slowest
[13:12]	SMUTEA[1:0]	2'h0	Soft mute Attenuation. 00 = 16db. 01 = 14db 10 = 12db, 11 = 10db
[11]	CLKSEL	1'h0	Clock Select 0 = External clock input, 1= Internal oscillator input.
[10:4]	SKSNR[6:0]	7'h1e	Seek SNR Threshold. Required channel SNR for a valid seek channel
[3:0]	SKCNT[3:0]	4'hf	Seek Impulse Detection Threshold Allowable number of impulse for a valid seek channel while setting all zeros means not use Impulse number to judge the channel's validity.

Register 07h. Test1 (0x0900)

BIT	NAME	DEFAULT	DESCRIPTION
[15:14]	Reserved	2'h0	Reserved
[13]	MODE	1'h0	Receiver Mode Select 0 = FM receiver 1 = AM receiver
[12]	SIQ	1'h0	IF I/Q Signal switch. 0 = Normal operation 1 = Reversed I/Q signal
[11]	IMPEN	1'h1	Impulse Remove Enable 0 = Disable 1 = Enable
[10]	BPDE	1'h0	De-emphasis Bypass 0 = Normal operation 1 = Bypass de-emphasis
[9:8]	IMPTH[1:0]	2'h1	Threshold of Impulse Detect. 00 = toughest

			11 = loosest
[7:3]	STGAIN [4:0]	5'h0	Stereo L/R Gain Adjustment, sighed value 00000 = 0 dB ⋯ 01111=15dB 10000= -16dB ⋯ 11111= -1dB For stereo separation optimization
[2:0]	FMGAIN [2:0]	3'h0	The gain of Frequency demodulated. 000 = 0dB ⋯ 011= +18dB 100= 0dB ⋯ 111= −18dB

Register 08h. Test2 (0x ac90)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	AFCEN	1'h1	AFC Enable 0 = Disable 1 = Enable
[14:13]	TCSEL[1:0]	2'h1	AFC/RSSI/SNR Calculate Rate 00 = fastest 11 = slowest. 4X times each
[12]	SEL25K	1'h0	AFCRL Threshold 0 = Channel space/2 1 = 25kHz
[11]	AVE	1'h1	AFC Average 0 = Use the instant AFC value 1 = Use the average AFC value
[10:9]	VAR[1:0]	2'h2	Variation Threshold for average AFC calculation 00 = Disable 01 = the toughest 11 = the loosest
[8:7]	RANGE [1:0]	2'h1	AFC Average Range 00 = the toughest 11 = the loosest
[6:0]	AFCRSSIT H[6:0]	7'h10	RSSI Threshold for Instant AFC updating

Register 09h. Status1 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:7]	AFC[8:0]	9'h000	The AFC value. unit AM 0.15k Hz, FM 0.6k Hz
[6:0]	SNR[6:0]	7'h00	The SNR Value.(in dB)

Register 0Ah. Status2 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	RDSR	1'h0	RDS Ready Indicator 0 = Not Ready 1 = Ready Keep high for 40ms after new RDS is received
[14]	STC	1'h0	Seek/Tune Complete 0 = Not Complete 1 = Complete
[13]	SF/BL	1'h0	Seek Fail/Band Limit 0 = Seek successful. 1 = Seek fail/Band limit reached
[12]	AFCRL	1'h0	AFC Rail 0 = AFC not railed 1 = AFC railed
[11:8]	CNTIMP	4'h0	Impulse Number
[7]	ST	1'h0	Stereo Indicator
[6:0]	RSSI[6:0]	7'h00	RSSI value

Register 0Bh. Read Channel (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	Reserved	1'h0	Reserved
[14:0]	READCHAN[14:0]	15'h0000	Read Channel Provides the current working channel

Register 0Ch. RDS1 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	RDSA[15:0]	16'h0000	The First Register of RDS Received

Register 0Dh. RDS2 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	RDSB[15:0]	16'h0000	The second register of RDS received

Register 0Eh. RDS3 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	RDSC[15:0]	16'h0000	The third register of RDS received

Register 0Fh. RDS4 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	RDSD[15:0]	16'h0000	The fourth register of RDS received when read

Register 10h. Boot Configuration1 (0x7b11)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h7b11	Reserved.

Register 11h. Boot Configuration2 (0x0080)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h0080	Reserved.

Register 12h. Boot Configuration3 (0x4000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h4000	Reserved.

Register 13h. Boot Configuration4 (0x3e00)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h3e00	Reserved.

Register 14h. Boot Configuration5 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	SKMUTE	1'h0	0: disable soft mute when seeking 1: enable soft mute when seeking
[14]	AFCMUTE	1'h0	0: disable soft mute when AFCRL is high 1: enable soft mute when AFCRL is high
[13:7]	SNRMTH[6:0]	7'h00	The Mute Threshold Based on SNR
[6:0]]	RSSIMTH[6:0	7'h00	The Mute Threshold Based on RSSI

Register 15h. Boot Configuration6 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h8000	Reserved.

Register 16h. Boot Configuration7 (0x0400)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h0400	Reserved.

Register 17h. Boot Configuration8 (0x0001)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h0001	Reserved.

Register 18h. Boot Configuration9 (0x143c)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h143c	Reserved.

Register 19h. Boot Configuration10 (0x4351)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	Reserved	16'h4351	Reserved. Do not write anytime.

Register 1Ah. Boot Configuration11 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15:9]	Reserved	7'h00	Reserved.
[8:0]	ANT_SEL[8:0]	9'h000	Antenna varactor tune

Register 1Bh. Analog Configuration1 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	FREQ_SEL[0]	1'h0	Reference clock divider control ,Refer to Reg1D Default 0 for 32.768kHz reference input.
[14:0]	Reserved	15'h0000	Reserved.

Register 1Ch. Analog Configuration2 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	FREQ_SEL[1]	1'h0	Reference clock divider control ,Refer to Reg1D Default 0 for 32.768kHz reference input.
[14:0]	Reserved	15'h0000	Reserved.

Register 1Dh. Analog Configuration2 (0x0000)

BIT	NAME	DEFAULT	DESCRIPTION
[15]	FREQ_SEL[17:2]	16'h0000	Reference clock divider control , FREQ_SEL[17:0] = HEX |Ref Frequency/512+0.5| Default 16 for 32.768kHz reference.

Register 1Eh - Register 28h.

Internal test registers are not accessible for user. Initial value and procedure will be provided separately by BEKEN.

5 Pin Assignment

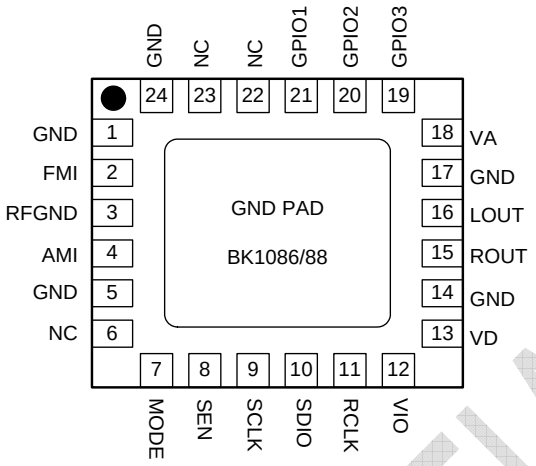


Figure 8 Pin assignment for BK1086/88 QFN24 4x4 mm package

Pin Number(s)	Name	Description
1,5,14,17,24, GND PAD	GND	Ground. Connect to ground plane on PCB
2	FMI	FM RF input.
3	RFGND	RF ground.
4	AMI	MW/SW/LW RF input.
7	MODE	Control interface selection MODE pin is low , I^2C mode MODE pin is high , SPI mode
8	SEN	Serial communications enable. (active low)
9	SCLK	Clock for Serial communications.
10	SDIO	Serial data input/output.
11	RCLK	32.768kHz - 38.4MHz external reference clock input/32.768KHz Oscillator input.
12	VIO	Power supply for I/O.
13	VD	Power supply for digital.
15	ROUT	Right audio output.
16	LOUT	Left audio output.
18	VA	Power supply for analog.
19,20,21	GPIO1,2,3	General purpose input/output.
6,22,23	NC	Not connect.

6 Typical Application Schematic

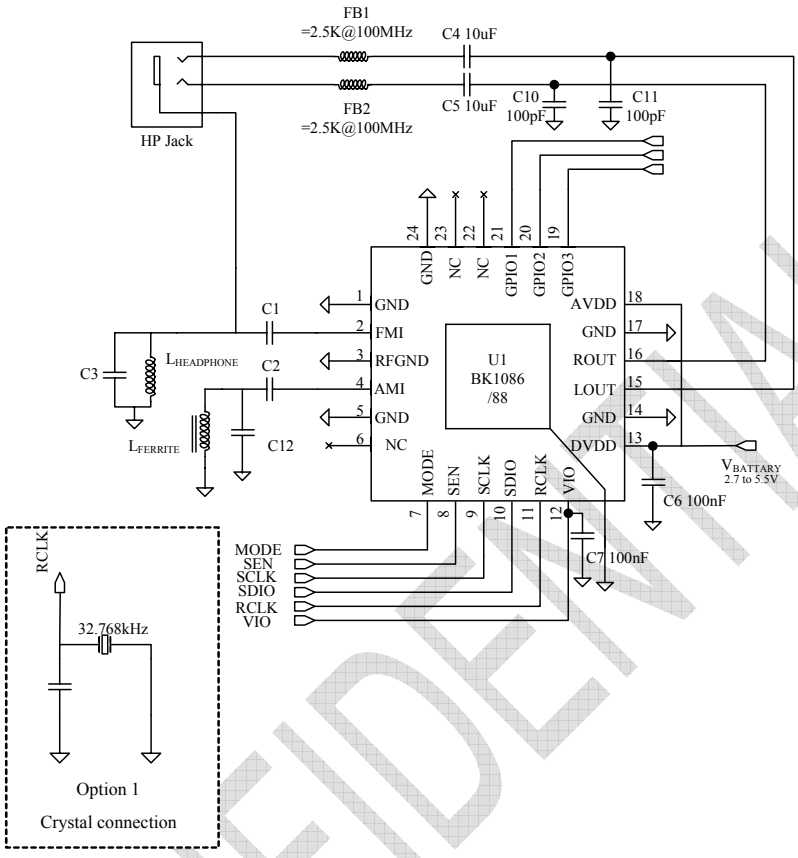


Figure 9. BK1086/88 with Headphone Antenna Application

Notes:

1. J1: Common 32Ω resistance headphone.
2. U1:BK1086/88 chip.
3. FM choke ($L_{headphone}$ and C3) for LNA input match with the headphone.
4. Pin NC (6, 22, and 23) should be leaved floating.
5. Place C6, C7 close to chip pin.
6. All grounds connect directly to GND plane on PCB.
7. Keep the FMI and AMI trace as short as possible.
8. Keep the wire from FMI to headphone as short as possible and must put it on the surface of the PCB.
9. When use crystal to generate the reference clock, please refer to the option 1(Crystal connection).

7 Package information

QFN 4x4 24pin packages are available for BK1086/88. Detail information of the package follows:

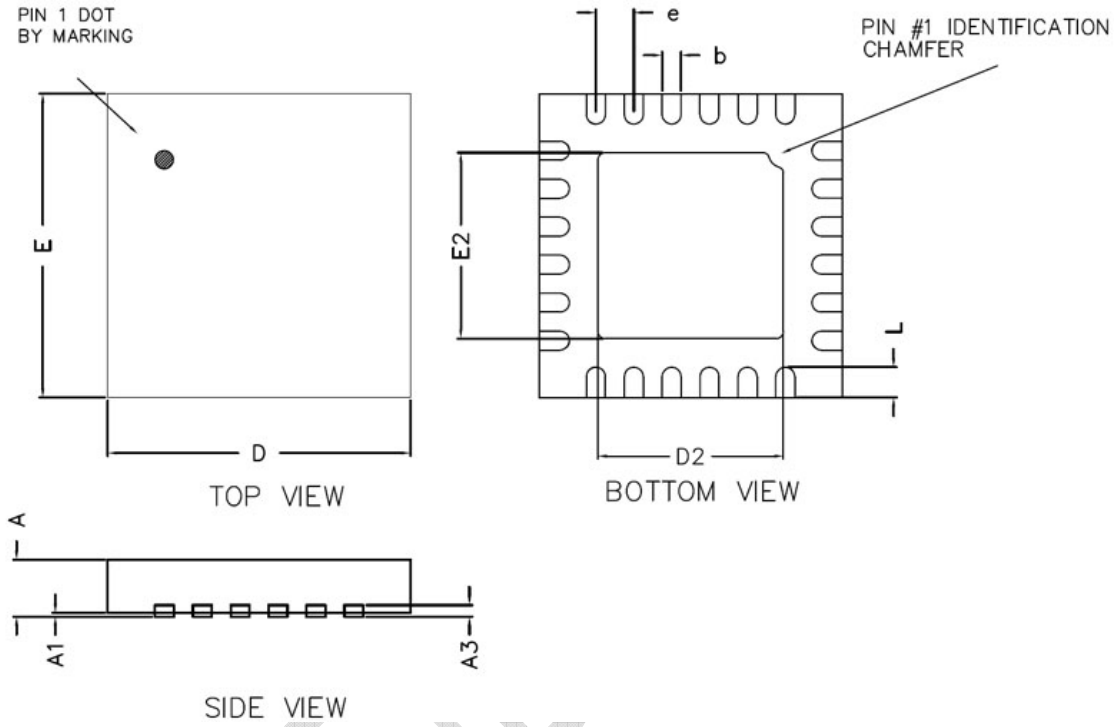


Figure 10 QFN 4x4 24 Pin Package diagram

Table 6 QFN 4x4 24 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0.00	-	0.05	mm
A3		0.20 REF		mm
D	3.95	4.00	4.05	mm
E	3.95	4.00	4.05	mm
b	0.20	0.25	0.30	mm
L	0.35	0.40	0.45	mm
D2	2.30	2.45	2.55	mm
E2	2.30	2.45	2.55	mm
e		0.50 REF		mm

Soldering layer content

Content	width	unit
Ni	0.5-2.0	um
Pd	0.02-0.15	um
Au	0.003-0.015	um

Storage Caution

1. Calculated shelf life in vacuum sealed bag 12 months at<40℃ and 90% relative humidity(RH).
2. Peak package body temperature 260℃.
3. After vacuum sealed bag is opened ,devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within 168 hours of factory conditions<40℃/60%.
   b) Stored at 10% RH.

8 Solder Reflow Profile

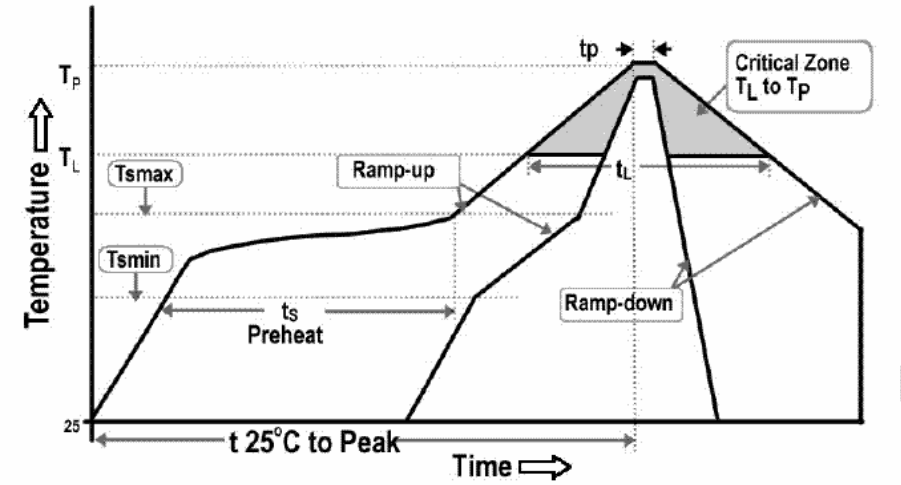


Figure 11 Classification Reflow Profile

Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3°C/second max.
Pre_heat	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (TL)	217°C
	Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual PeakTemperature (tp)		20-40 seconds
Ramp-Down Rate 6		6°C/second max.
Time 25°C to Peak Temperature 8		8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD Techniques should be used when handling these devices.

9 Order information

Part number	Package	Packing	MOQ (ea)
BK1086QB	QFN24	Tape Reel	3K
BK1088QB	QFN24	Tape Reel	3K

Remark:
MOQ: Minimum Order Quantity

10 Additional Reference Resource

- Universal application guide
- EVB quick-start guide

11 Revision History

Version	Change Summary	Data	Author
Rev.0.1	Initial draft	06-29-2009	JW
Rev.0.2		02-04-2010	JW
Rev.1.0	Formal release version	09-15-2010	JW