Comlinear Corporation

Fast Settling, High Current Wideband Op Amps

CLC203

APPLICATIONS:

- coaxial line driving
- DAC current to voltage amplifier
- flash A to D driving
- baseband and video communications
- radar and IF processors

FEATURES:

- 60MHz full-power bandwidth (20V_{pp}, 100Ω)
- 200mA output current
- 0.2% settling in 15ns
- 0.5mV input offset voltage, 5μV/°C drift
- 4ns rise and fall times (20V)

DESCRIPTION:

The CLC203 is a wideband, high-current operational amplifier which features a unique combination of high power and high precision. The amplifier's **output current of 200mA and a full-power bandwidth of 60MHz (20V_{pp}, 100Ω)** ensure a quick design solution for the most demanding loads and signals. The **solid 15ns settling time (to 0.2%)** is reinforced by the CLC203's excellent DC performance; typically, the input offset voltage is only 0.5mV and is guaranteed to be less than 1mV at +25°C. **The input offset voltage drift is typically only 5μV/°C.**

The CLC203 is well suited to a wide range of applications. Specifically, the wide bandwidth, fast settling, linear phase, and very low harmonic distortion provide the designer with the signal fidelity needed in applications such as driving flash A to Ds or coaxial lines. The 60MHz full-power bandwidth and 200mA output current of the CLC203 eliminate the need for power buffers in most applications. Engineers desiring to improve the DC performance or settling precision of systems using the original CLC103 may replace it with a CLC203—in most cases with no design changes (they are pin compatible, however the CLC203 does not have a bias control pin).

The dynamic performance of the CLC203 is based on Comlinear's proprietary op amp topology. This new design provides performance far beyond that available from conventional op amp designs; for example, **the —3dB bandwidth remains nearly constant over a wide range of gains.** (See the table below.) And since the amplifier is inherently stable, the user is saved the trouble and expense of designing external compensation networks. The result is shorter design time and the ability to accommodate design changes (in gain, for example) without loss of performance or a redesign of compensation circuits.
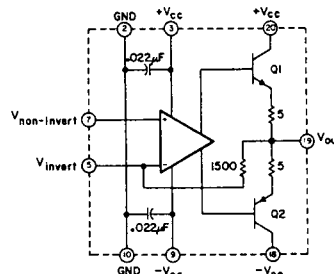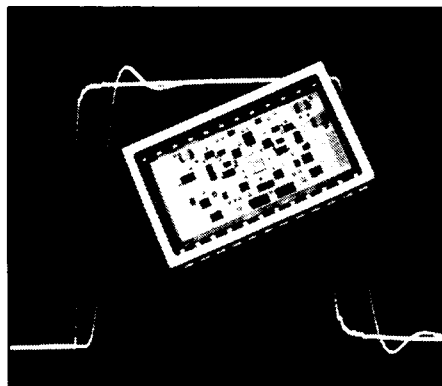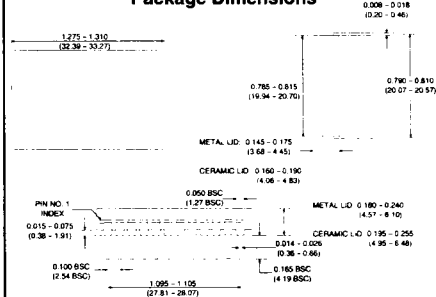
The CLC203 is constructed using thin film resistor/bipolar transistor technology. The CLC203AI is specified over a temperature range of −25°C to +85°C, while the CLC203AM is specified over a range of −55°C to +125°C and is screened to Comlinear's M Standard for high reliability applications. Both devices are packaged in 24-pin ceramic DIPs.

CLC203 Equivalent Circuit Diagram
(all undesignated pins are internally unconnected)

Package Dimensions

Typical Performance

parameter	gain setting						units
	+4	+20	+50	−4	−20	−50	
−3dB bandwidth	250	170	120	195	165	120	MHz
rise time (20V)	4	4	4	4	4	4	ns
slew rate	6	6	6	6	6	6	V/ns
settling time (0.2%)	15	15	18	15	15	18	ns

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC203AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC203AI	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
* −3dB bandwidth	$V_{out}<4V_{pp}$	160	>140	>140	>110	MHz	SSBW
	$V_{out}=20V_{pp}$	60	>50	>50	>40	MHz	FPBW
gain flatness at	$V_{out}<4V_{pp}$						
* peaking	0.1 to 40MHz	0.1	<0.7	<0.4	<0.3	dB	GFPL
* peaking	>40MHz	0.2	<1.5	<0.6	<0.6	dB	GFPH
* rolloff	at 75MHz	—	<0.4	<0.6	<1.0	dB	GFR
group delay	to 75MHz	3.3±0.3	—	—	—	ns	GD
linear phase deviation	to 75MHz	1	<3.5	<2.5	<2.5	°	LPD
reverse isolation	to 150MHz						
non-inverting		55	>45	>45	>45	dB	RINI
inverting		48	>40	>40	>40	dB	RII
TIME DOMAIN RESPONSE							
rise and fall time	5V step	2.5	<2.9	<2.9	<3.3	ns	TRS
	20V step	4.0	<5.0	<5.0	<5.0	ns	TRL
settling time to 0.2%	10V step	15	<25	<20	<25	ns	TSP
overshoot	5V step	7	<20	<15	<15	%	OS
slew rate (overdriven input)		6	>5	>5	>5	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		30	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
*2nd harmonic distortion	$2V_{pp}$, 20MHz	−55	<−45	<−45	<−45	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz	−55	<−45	<−45	<−45	dBc	HD3
equivalent noise input							
noise floor	>100kHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	28	<56	<56	<56	μV	INV
noise floor	>5MHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	28	<56	<56	<56	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		0.5	<2.2	<1.5	<2.5	mV	VIO
average temperature coefficient		5	<15	<15	<15	μV/°C	DVIO
*input bias current	non-inverting	5	<36	<20	<20	μA	IBN
average temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	5	<26	<15	<30	μA	IBI
average temperature coefficient		50	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		60	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 75MHz	2, 45	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±11	>±11	>±11	V	VO

Common Mode and Output Voltage Limits
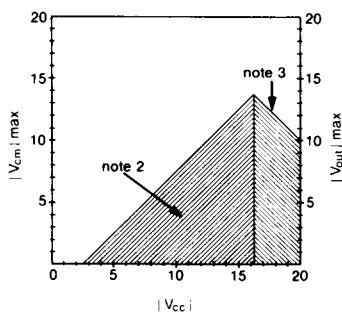
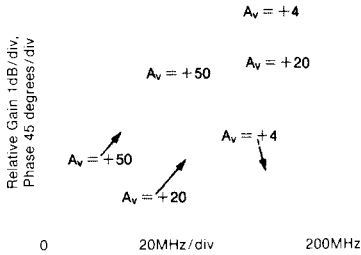|	
supply voltage (V_{cc})	±20V
output current	±200mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	AM: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

note 1: Parameters preceded by an * are the final electrical test parameters and are 100% tested. AM units are tested at −55°C, +25°C, and +125°C. AI units are tested only at +25°C although their performance is guaranteed at −25°C and +85°C as indicated above.
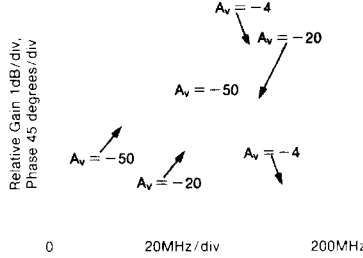
note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed V_{cc}. (V_{cm} is the voltage at the non-inverting input, pin 7.)

note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ±15V.
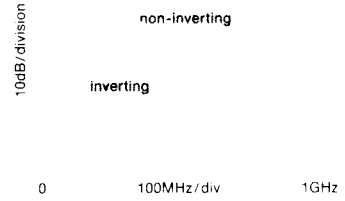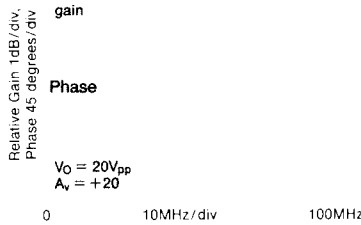
Non-Inverting Gain and Phase
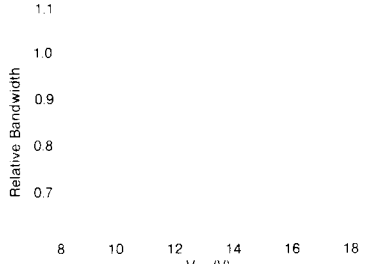
Relative Gain 1dB/div,
Phase 45 degrees/div

$A_v = +4$
$A_v = +50$ $A_v = +20$
$A_v = +50$ $A_v = +4$
$A_v = +20$

0   20MHz/div   200MHz

Inverting Gain and Phase

Relative Gain 1dB/div,
Phase 45 degrees/div

$A_v = -4$
$A_v = -20$
$A_v = -50$
$A_v = -50$ $A_v = -4$
$A_v = -20$

0   20MHz/div   200MHz

Broadband Inverting and Non-Inverting Gain

10dB/division

non-inverting

inverting

0   100MHz/div   1GHz

Large Signal Gain and Phase

Relative Gain 1dB/div,
Phase 45 degrees/div

gain

Phase

$V_O = 20V_{pp}$
$A_v = +20$

0   10MHz/div   100MHz

Relative Bandwidth vs. V_{cc}

Relative Bandwidth

1.1
1.0
0.9
0.8
0.7

8   10   12   14   16   18
V_{cc} (V)

Gain vs. Frequency for Various Loads

1dB/div

1kΩ
100Ω
200Ω
50Ω

0   20MHz/div   200MHz
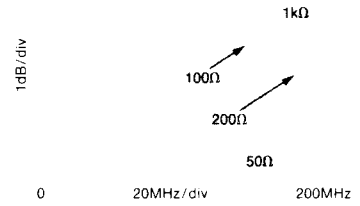
Small Signal Pulse Response (Inv, Non-Inv)

$A_v = +20$

1V/div

$A_v = -20$

5ns/div

Large Signal Pulse Response (Inv, Non-Inv)

$A_v = +20$

4V/div

$A_v = -20$

5ns/div

Settling Time

Settling Percentage

+0.5
+0.4
+0.3
+0.2
+0.1
0
-0.1
-0.2
-0.3
-0.4
-0.5

5ns/div

50ns/div
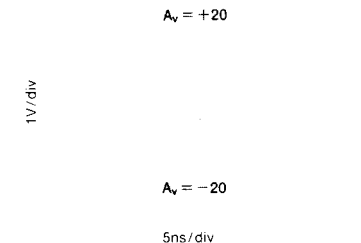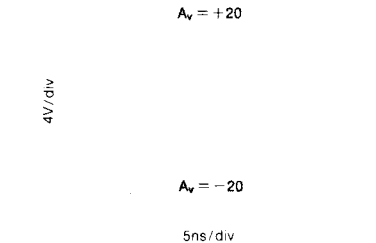
Time
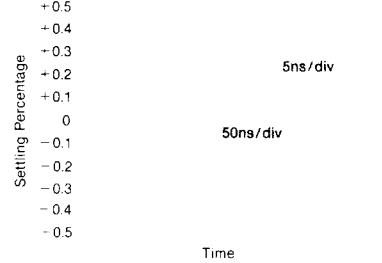
2nd and 3rd Harmonic Distortion Intercept

Intercept Point (- dBm)

100
85
70
55
40

2nd harmonic
intercept exceeds
90dBm below 100kHz I_2

3rd harmonic
intercept exceeds
65dBm below 100kHz I_3

10^5 10^6 10^7 10^8
Frequency (Hz)
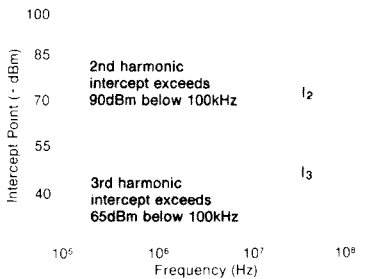
2-Tone 3rd Order Intermod. Intercept

Intercept Point (+ dBm)

55
50
45
40
35
30

0   20   40   60   80   100
Frequency (MHz)

CMRR and PSRR

dB

70
60
50
40
30

PSRR

CMRR

10^1 10^2 10^3 10^4 10^5 10^6 10^7
Frequency (Hz)

Equivalent Input Noise

Noise Voltage (nV/√Hz)
Noise Current (pA/√Hz)

100

10

1

Inverting Current
11.4pA/√Hz

Non-Inverting Current
2.5pA/√Hz

Voltage
2.2nV/√Hz

10^2 10^3 10^4 10^5 10^6 10^7 10^8
Frequency (Hz)

T_{case}

85°C/W   85°C/W   200°C/W   200°C/W

$T_{j(pnp)}$ $T_{j(npn)}$ $T_{j(cir1)}$ $T_{j(cir2)}$

P_{pnp} P_{npn} P_{cir1} P_{cir2} P_{cir3}

$\theta_{ca} = 23°C/W$ in still air without
a heatsink
(With heat sinking or air flow,
θ_{ca} will be lower.)

$T_{ambient}$

$P_{cir1} = 7mA [(+V_{cc}) - V_{out}]$
$P_{cir2} = 7mA [V_{out} - (-V_{cc})]$
$P_{cir3} = I_C [(+V_{cc}) - (-V_{cc})]$ where $I_C = 15mA$ at +15V
$P_{xxx} = I_{col}[(±V_{cc}) - V_{out} - I_{col}(R_{col} + 5)]$ where
$I_{col} = V_{out}/R_{load}$ or 8mA, whichever is
greater. (Include R_f in R_{load}.)

(For positive V_{out} and V_{cc}, P_{xxx} is the power in the
npn device. For negative V_{out} and V_{cc}, this power is
in the pnp device.)
R_{col} is an external resistor (22 ohms recommended)
between the xxx collector and +V_{cc}.
$T_{j(pnp)} = (P_{pnp}) 85°C/W + (P_{total}) \theta_{ca} + T_{ambient}$
similar for $T_{j(npn)}$.
$T_{j(cir1)} = (P_{cir1}) 200°C/W + (P_{total}) \theta_{ca} + T_{ambient}$
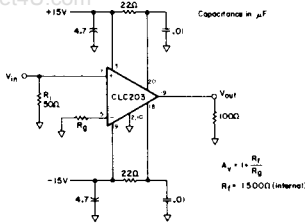similar for $T_{j(cir2)}$.

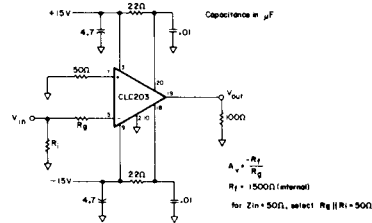Figure 1: recommended non-inverting gain circuit

Figure 2: recommended inverting circuit

Test fixture layout artwork is available upon request.

CLC203 Operation

The CLC203 is based on Comlinear's proprietary op amp topology, a unique design which uses current feedback instead of the usual voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (see the gain equations above). A complete discussion of current feedback is given in application note AN300-1.

Increasing Bandwidth at High Gains

At high gains ($|A_v| \geq 50$) the bandwidth of the CLC203 may be increased by lowering the value of feedback resistance. This is done by connecting an external resistor in parallel with the internal 1500Ω feedback resistor. The table below shows the recommended external resistor values for different gain settings.

Increasing Bandwidth at High Gains

$|A_v|$	external resistor	−3dB bandwidth
50	$3k\Omega$	140MHz
100	750Ω	110MHz

Layout Considerations

To obtain optimum performance from any circuit operating at high frequencies, good PC layout is essential. Fortunately, the stable, well-behaved response of the CLC203 makes operation at high frequencies less sensitive to layout than is the case with other wideband op amps, even though the CLC203 has a much wider bandwidth.

In general, a good layout is one which minimizes the unwanted coupling of a signal between nodes in a circuit. A continuous ground plane from the signal input to output on the circuit side of the board is helpful. Traces should be kept short to minimize inductance. If long traces are needed, use microstrip transmission lines which are terminated in their characteristic impedance. At some high-impedance nodes, or in sensitive areas such as near pin 5 of the CLC203, stray capacitance should be kept small by keeping nodes small and removing ground plane directly around the node.

The $\pm V_{cc}$ connections to the CLC203 are internally bypassed to ground with $0.022\mu F$ capacitors to provide good high-frequency decoupling. It is recommended that $1\mu F$ or larger tantalum capacitors be provided for low-frequency decoupling. The $0.01\mu F$ capacitors shown at pins 18 and 20 in figures 1 and 2 should be kept within 0.1" of those pins. A wide strip of ground plane should be provided for a signal return path between the load-resistor ground and these capacitors.

Since the layout of the PC board forms such an important part of the circuit, much time can be saved if prototype amplifier boards are tested early in the design stage. Encased/connectorized amplifiers are available from Comlinear.

Distortion and Noise

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC203. First, convert the output voltage (V_O) to $V_{rms} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{rms}^2))$ to get the output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$ dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$ dB below the level of P, as will the two-tone third order intermodulation products. These approximations are useful for $P < -1$dB compression levels.

Approximate noise figure can be determined for the CLC203 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \dfrac{i_n^2\, R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high-frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly-qualified applications engineers to provide technical and design assistance.