YAMAHA LSI

YVZ152B

(CDGD)
CD Graphics Decoder

■ OUTLINE

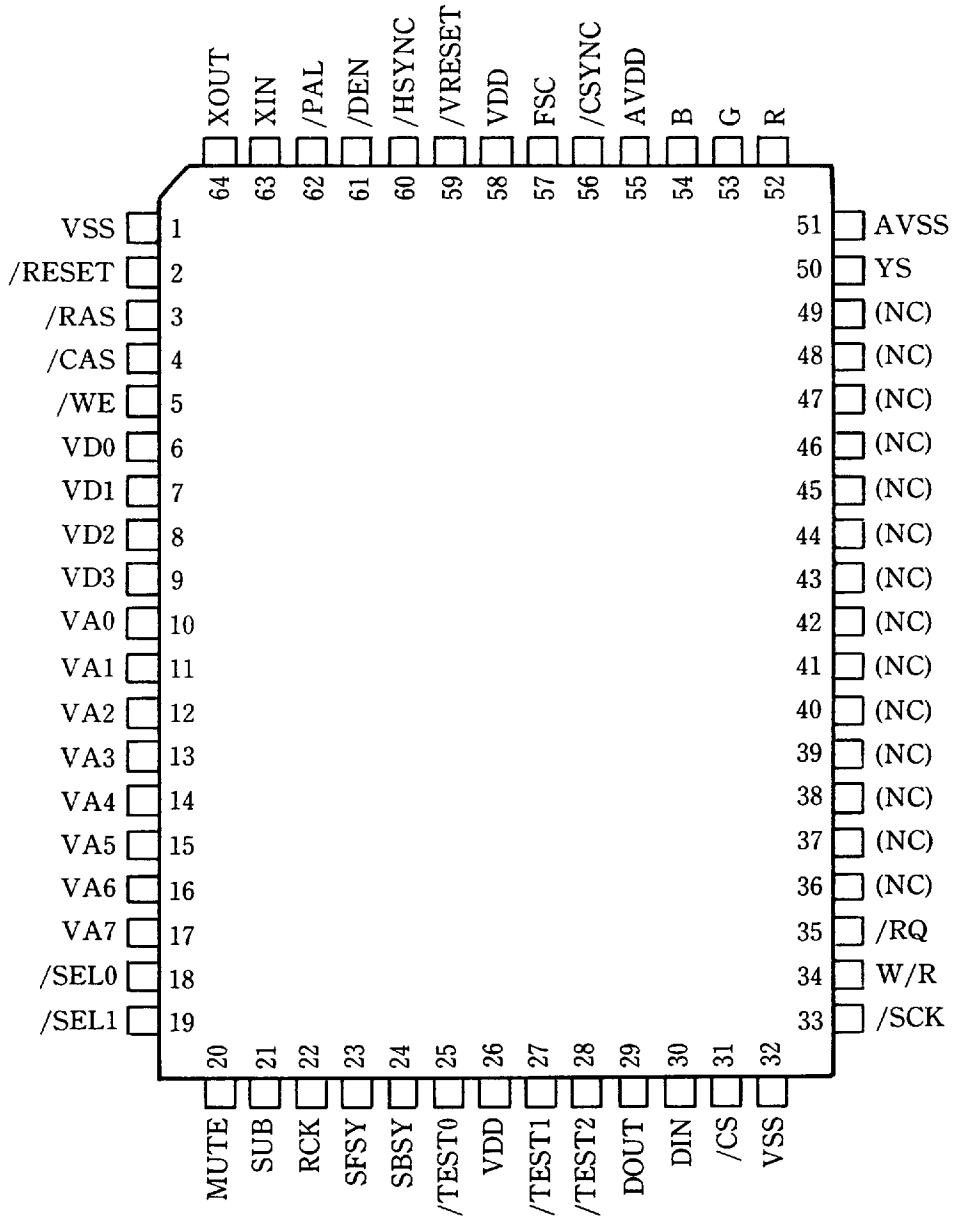
The YVZ152B (CDGD) is an LSI with the functions necessary for the CD graphics player incorporated in one chip. They are such functions as to deinterleave, detect and correct errors of subcodes R ~ W, and process the graphic command. By using the subcode output from the CD signal processing LSI such as YM7121C (SPC5), simple attachment of the 256K bit DRAM and composite video encoder will allow to decode the CD graphics. As the graphic command is read and written by the microprocessor, it can be used for the subcode system other than the CD graphics.

■ FEATURES

- Deinterleave, error detection and correction functions for the CD subcode R ~ W
- Interface with the subcode output comforming to EIAJ from the CD signal processing LSI
- Interface with the digital audio interface receiver of the YM3623B and YM3436D
- Control over the drawing process and display of the CD graphics
- Linear RGB output by the built-in DAC
- One unit of 256K bit DRAM is connected as a video RAM
- Superimposing with the other visual equipment is possible by the external synchronous function
- Useable for both NTSC and PAL
- Graphic commands can be read and written through the microprocessor serial interface
- The backdrop color setting and the screen display setting including the display position adjustment can be done through the microprocessor.
- Single 5V power supply, Si-gate CMOS process
- 64-pin plastic QFP (YVZ152B-F)

YVZ152 CATALOG
CATALOG No. : LSI-4VZ152
1994 04

■ PIN CONFIGURATION



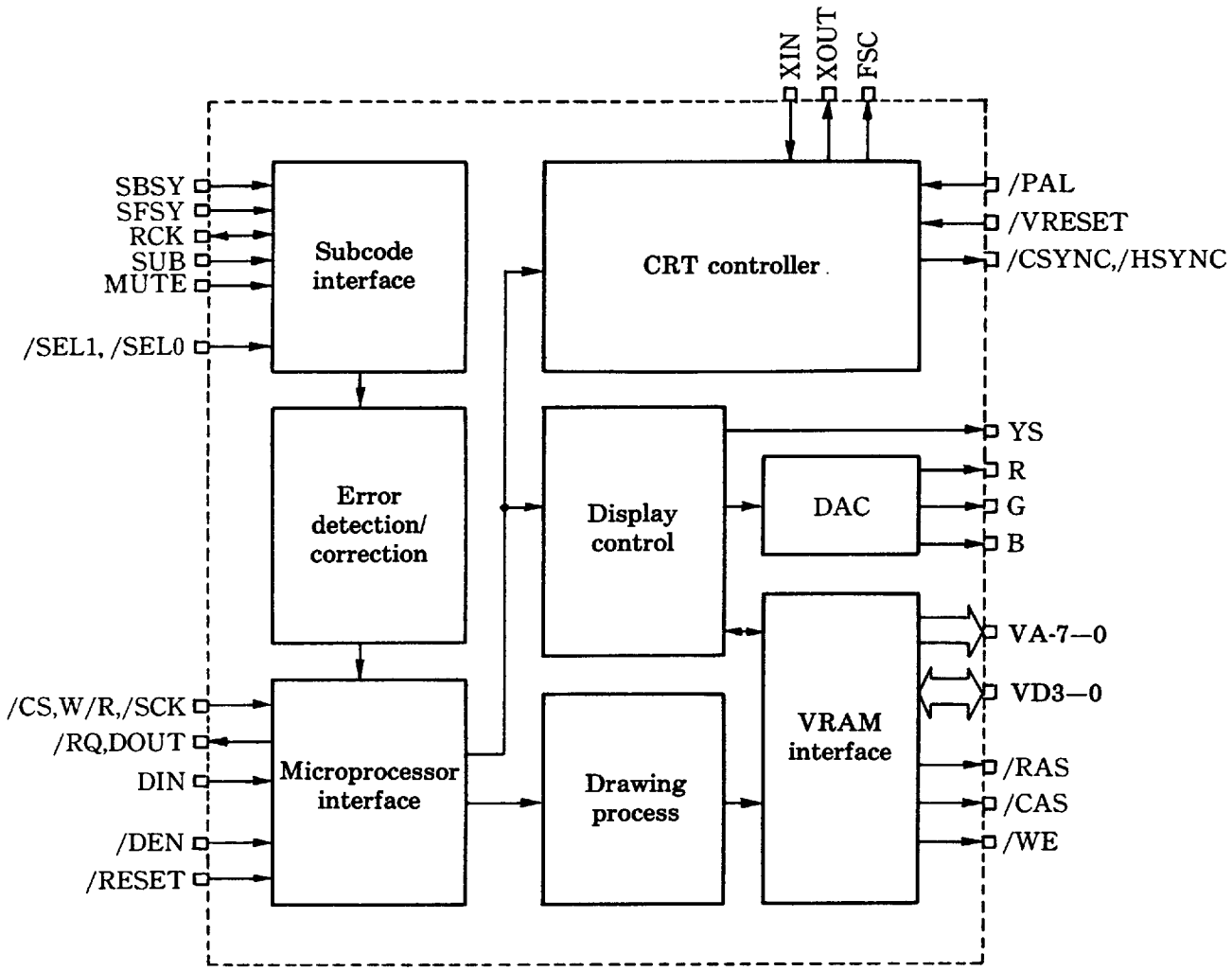
〈64QFP Top View〉

■ PIN DESCRIPTION

No.	Name	I/O	Function
1	VSS	—	Ground (for digital block)
2	/RESET	I	Reset input (low active)
3	/RAS	O	DRAM interface RAS
4	/CAS	O	DRAM interface CAS
5	/WE	O	DRAM interface WE
6	VD0	I/O	DRAM interface data (LSB)
7	VD1	I/O	DRAM interface data
8	VD2	I/O	DRAM interface data
9	VD3	I/O	DRAM interface data (MSB)
10	VA0	I	DRAM interface address (LSB)
11	VA1	I	DRAM interface address
12	VA2	I	DRAM interface address
13	VA3	I	DRAM interface address
14	VA4	I	DRAM interface address
15	VA5	I	DRAM interface address
16	VA6	I	DRAM interface address
17	VA7	I	DRAM interface address (MSB)
18	/SEL0	I+	Subcode interface, interface select
19	/SEL1	I+	Subcode interface, interface select
20	MUTE	I	Subcode interface, subcode data muting
21	SUB	I	Subcode interface, subcode data
22	RCK	I/O	Subcode interface, clock
23	SFSY	I	Subcode interface, frame synchronous signal
24	SBSY	I	Subcode interface, block synchronous signal
25	/TEST0	I+	LSI test terminal (normally unconnected)
26	VDD	—	+5V power supply (for digital block)
27	/TEST1	I+	LSI test terminal (normally unconnected)
28	/TEST2	I+	LSI test terminal (normally unconnected)
29	DOUT	OT	Microcomputer interface, serial data output
30	DIN	I	Microcomputer interface, serial data input
31	/CS	I	Microcomputer interface, chip select
32	VSS	—	Ground (for digital block)
33	/SCK	I	Microcomputer interface, serial clock input
34	W/R	I	Microcomputer interface, read/write select
35	/RQ	O	Microcomputer interface, subcode read request
36	(NC)		
⋮			
49	(NC)		
50	YS	O	Superimpose timing output
51	AVSS	—	Ground (for analog block)
52	R	O	RGB output (R)
53	G	O	RGB output (G)
54	B	O	RGB output (B)
55	AVDD	—	+5V power supply (for analog block)
56	/CSYNC	O	Composite synchronous signal output
57	FSC	O	NTSC sub-carrier clock output (3.579545 MHz)
58	VDD	—	+5V power supply (for digital block)
59	/VRESET	I+	Vertical timing reset input
60	/HSYNC	O	Horizontal synchronous signal output
61	/DEN	I+	Screen display enable ('L' : data display ON)
62	/PAL	I+	NTSC/PAL select ('H' : NTSC mode, 'L' : PAL mode)
63	XIN	I	Crystal oscillator connecting terminal or external clock input (14.31818 MHz)
64	XOUT	O	Crystal oscillator connecting terminal

Note) I+ : Input terminal with a pulled-up resistor
OT : Tri-state output terminal

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

1. Clocks XIN, XOUT

The crystal oscillator circuit is formed by using both XIN and XOUT terminals. The oscillation frequency is 4 fsc (14.31818 MHz) in the NTSC mode. Also it is possible to input the external clock through the XI terminal.

2. Subcode interface /SEL1, /SEL0, SBSY, SFSY, RCK, SUB, MUTE

This subcode interface conforms to EIAJ. Also, it is possible to take out the subcode from the user data output by connecting with the YM3623B (DIR) or YM3436D (DIR2). The format is determined by selecting 'H' or 'L' of /SEL1 and /SEL0 as shown below.

/SEL1	/SEL0	INTERFACE	SBSY	SFSY	RCK	SUB
H	H	EIAJ(1)	SBSY	SFSY(1)	RCK(1)	DATA
H	L	EIAJ(2)	–	SFSY(2)	RCK(2)	DATA
L	H	YM3623	L/R(15pin)	SSYNC(26pin)	SCK(25pin)	SDO(27pin)
L	L	YM3436	LR(38pin)	–	–	FS0(34pin)

Note) For the formats of EIAJ (1) and EIAJ (2), refer to the subcode input format.

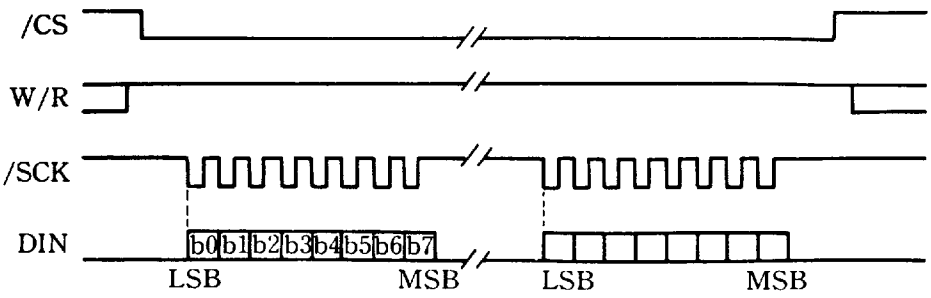
In EIAJ(1), YM3623 or YM3436 mode, when the sub-code block synchronous signals have occurred at discontinuous positions due to a scratch or some other reason, they are neglected. Also, when they have failed to occur at expected positions, they are interpolated for protection.

When MUTE='H' at using EIAJ input, MUTE disables the input of SBSY, SFSY and SUB, and stops the output of RCK.

3. Microprocessor interface /CS, /RQ, /SCK, W/R, DIN, DOUT

3-1 Command input

The data sent from the microprocessor in the following format is received as a command.



The data must be sent by the specified number of bytes (1 byte=8 bits) determined by the command. (2 bytes for the register write command and 19 bytes for the graphic command)

(1) Register write command (2 bytes)

This command sets the operation of each section by writing the data in the specified register.

	b7	b6	b5	b4	b3	b2	b1	b0	
1st byte	1	0	0	0	RN3	RN2	RN1	RN0	REGISTER NUMBER
2nd byte	1	1	D5	D4	D3	D2	D1	D0	REGISTER DATA

(2) Register map

CONTROL REGISTER(REGISTER NUMBER 0)

RN3, 2, 1, 0	D5	D4	D3	D2	D1	D0
(0, 0, 0, 0)	IRST	RQIH	STEN	CINH	GCEN	DISP

- DISP Screen display enable (The operation of the logical OR with NOT of the /DEN terminal is executed.)
  (DISP or DEN)=1 : displays the VRAM data and border color (display enable).
  0 : Colors of the BACKDROP COLOR REGISTER are displayed throughout the screen (display disable).
- GCEN Microprocessor graphic command control enable
  1 : The graphic command from the microprocessor is permitted. The subcode input is neglected and the /RQ is not output.
  0 : The subcode command is permitted. The graphic command from the microprocessor is neglected.
- CINH Graphic command invalid
  1 : The graphic command is not executed even when inputted.
  0 : The inputted graphic command is executed.
- STEN Selection of the microprocessor read data
  1 : The status data is read out. The /RQ is not output.
  0 : The subcode data after the error detection correction is read out. The /RQ is output.
- RQIH Control over the /RQ (read request) output to the microprocessor
  1 : The /RQ is output when a subcode other than MODE=0 and MODE=1 is inputted.
  0 : The /RQ is output when a subcode other than MODE=0 is inputted.
- IRST Initial reset signal
  1 : All registers other than CONTROL REGISTER and DISPLAY ADJUST REGISTER set "power ON reset" conditions.
  0 : Normal operation

DISPLAY ADJUST REGISTER(REGISTER NUMBER 1)

RN3, 2, 1, 0	D5	D4	D3	D2	D1	D0
(0, 0, 0, 1)	DAV2	DAV1	DAV0	DAH2	DAH1	DAH0

- DAH2-0 : The display position in the horizontal direction is shifted to the right or left by 2-dot units.
  A 2's complement with DAH2 as a sign bit is used. When in minus, a shift to the left occurs and when in plus, to the right.
- DAV2-0 : The display position in the vertical direction is shifted up or down by 2-line units.
  A 2's complement with DAV2 as a sign bit is used. When in minus, an upward shift occurs and when in plus, a downward shift.

BACKDROP COLOR REGISTER(REGISTER NUMBER 2, 3)

RN3, 2, 1, 0	D5	D4	D3	D2	D1	D0
(0, 0, 1, 0)	R3	R2	R1	R0	G3	G2
(0, 0, 1, 1)	G1	G0	B3	B2	B1	B0

- When in the display disable, this color is displayed throughout the screen. The transparent timing is always active when YSEN is '1'.

YS REGISTER(REGISTER NUMBER 4, 5, 6)

RN3, 2, 1, 0	D5	D4	D3	D2	D1	D0
(0, 1, 0, 0)	/YS5	/YS4	/YS3	/YS2	/YS1	/YS0
(0, 1, 0, 1)	/YS11	/YS10	/YS9	/YS8	/YS7	/YS6
(0, 1, 1, 0)	YSEN	YSAT	/YS15	/YS14	/YS13	/YS12

- From among /YS15 to 0, the timing at which the '1' bit applicable color code is displayed becomes transparent.
- YSAT YS signal automatic generation
  1 : becomes transparent when the color code is /YS15 to 0 and PRESET BORDER
  0 : conforms to /YS15 to 0 only
- YSEN YS signal output enable
  1 : Low level output at a transparent (not superimpose) timing through the YS terminal
  0 : High level (superimpose timing) output through the YS terminal at all times

CHANNEL SELECT REGISTER(REGISTER NUMBER 7, 8, 9)

RN3, 2, 1, 0	D5	D4	D3	D2	D1	D0
(0, 1, 1, 1)	CN5	CN4	CN3	CN2	CN1	CN0
(1, 0, 0, 0)	CN11	CN10	CN9	CN8	CN7	CN6
(1, 0, 0, 1)	LINE	TEST	CN15	CN14	CN13	CN12

- LINE =1 : the LINE GRAPHICS mode
  0 : the TV GRAPHICS mode
- TEST LSI test bit
  Inputting '1' in this bit should be avoided.
- From among CN15 to 0, the graphic command of the '1' bit applicable channel is executed.

Note) When the /RESET terminal is set to the 'L' level, all registers will be cleared to '0' (although CN0 and CN1 of the CHANNEL SELECT REGISTER and B3 of the BACKDROP COLOR REGISTER will be set to '1').

(3) Microprocessor graphic command (19 bytes)

Using the same format as the graphic command, it is possible to execute drawing process through the microprocessor.

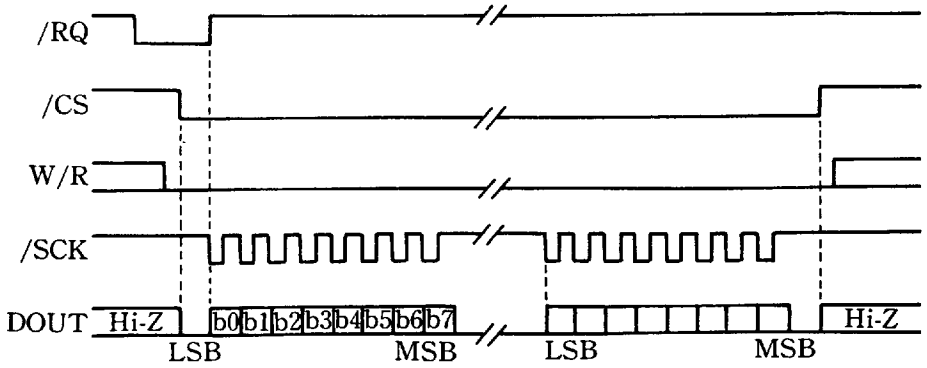
	b7	b6	b5	b4	b3	b2	b1	b0	
1st byte	0	0	0	0	0	0	0	0	Sync
2nd~19th byte	0	1	R	S	T	U	V	W	Symbol 0-19

The data is interpreted as shown below and executed in the same way as the subcode command.

	b5	b4	b3	b2	b1	b0	
1st byte	0	0	0	0	0	0	Sync
2nd byte	MODE			ITEM			Symbol 0
3rd byte	INSTRUCTION						Symbol 1
4th byte	DATA field						Symbol 4
19th byte							Symbol 19

3-2 Data output

The graphic command and the internal status are output to the microprocessor in the following format.



The data must be read by the specified number of bytes (1byte=8 bits). (19 bytes for the graphic command data and 1 byte for the internal status)

(1) Graphic command data (19 bytes)

When both GCEN and STEN of the CONTROL REGISTER are '0', it is possible to read the graphic command data whose error has been detected and corrected. When 1 pack data has been prepared internally, a read request signal is output from the /RQ terminal. Detecting this signal, the microprocessor read 19 bytes data continuously and provides the flag of the error detection/correction and symbol data . But the /RQ signal is not output by the subcode when the MODE is '0'.

As reception of the sub-code from the CD has a priority internally, the data is not secured unless the /RQ signal reading is completed within 3.3 msec. after it is output. The format of data to be read is as follows.

<Graphic command read data format>

	b7	b6	b5	b4	b3	b2	b1	b0	
1st byte	"0"	"0"	PKT	–	FQ1	FQ0	FP1	FP0	Flag word
2nd byte	"0"	"0"	R	S	T	U	V	W	Symbol 0
3rd byte	"0"	"0"	R	S	T	U	V	W	Symbol 1
4th byte	"0"	"0"	R	S	T	U	V	W	Symbol 4
5th byte					•				Symbol 5
					•				
					•				
					•				
					•				
					•				
					•				
					•				
					•				
					•				
					•				
					•				
19th byte	"0"	"0"	R	S	T	U	V	W	Symbol 19

- PKT : becomes '1' at the first pack of the packet
- FP1, FP0, FQ1, FQ0 : indicate the error detection/correction conditions as follows

PF1	PF0	Correction condition
0	0	No error in the data
0	1	Single correction executed and corrected
1	0	Double correction executed and corrected
1	1	Triple or more error detected and uncorrectable

QF1	QF0	Correction condition
0	0	No error in the data
0	1	Single correction executed and corrected
1	0	Double or more error detected and uncorrectable

(2) Internal status (1 byte)

The internal status can be read when the STEN of the CONTROL REGISTER is '1'.

	b7	b6	b5	b4	b3	b2	b1	b0	
1st byte	0	0	0	0	0	0	VB	CE	STATUS

- CE : become '1' during command execution
- VB : becomes'1' during vertical non-display period

4. DRAM interface VA7~0, VD3~0, /RAS, /CAS, /WE

This LSI requires a 256K bit DRAM as a video RAM.

Connect a DRAM which satisfies the conditions listed below. Refreshing is done by this LSI.

- 64K word × 4 bit configuration
- The access time from the /RAS is 120ns or less
- /CAS before /RAS refreshing is possible
- Following access modes are used.
  a) Read cycle
  b) Early write cycle
  c) Page mode read cycle (Cycle time : 120ns or less)
  d) Page mode write cycle (Cycle time : 120ns or less)

5. Drawing processing

The subcode, after being received, undergoes the deinterleave and error detection/correction operations and is transferred to the drawing processing block in packs. The command of an uncorrectable pack is not executed. Listed below are the commands that are interpreted and executed.

1) LINE GRAPHICS(MODE= 1, ITEM= 0)

- INSTRUCTION 4 ; Write FONT.
- INSTRUCTION12 ; Soft scroll SCREEN.

2) TV GRAPHICS(MODE= 1, ITEM= 1)

- INSTRUCTION 1 ; Preset MEMORY.
- INSTRUCTION 2 ; Preset BORDER.
- INSTRUCTION 6 ; Write FONT FORGROUND/BACKGROUND.
- INSTRUCTION20 ; Soft scroll SCREEN,with preset.
- INSTRUCTION24 ; Soft scroll SCREEN,with copy.
- INSTRUCTION30 ; Load the CLUT,colour− 0 ···colour− 7.
- INSTRUCTION31 ; Load the CLUT,colour− 8 ···colour−15.
- INSTRUCTION38 ; EXCLUSIVE−OR FONT with 2 colours.

6. CRT interface /DEN, R, G, B, FSC, /CSYNC, /HSYNC, /PAL, /VRESET, YS

The /DEN terminal is a display enable switch.

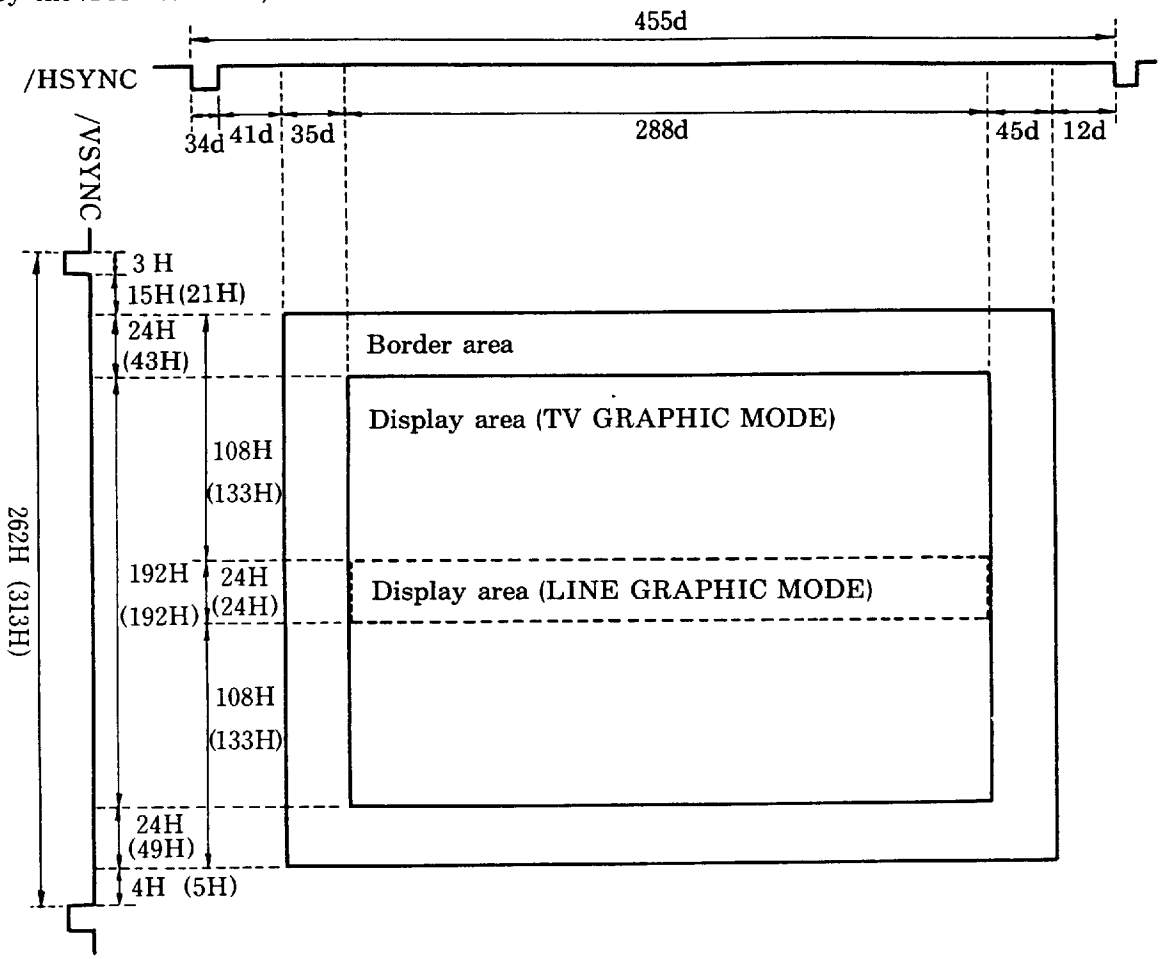
The image data is output regardless of the register setting when in 'L' and according to the DISP bit setting when in 'H'.

The image data is output by linear RGB through R, G and B terminals.

The fsc (3.579545 MHz) color sub-carrier clock is output through the FSC terminal.

The composite synchronous signal and horizontal synchronous signal are output through /CSYNC and /HSYNC terminals respectively.

Non-interlace scanning is executed at a cycle according to the NTSC or PAL specifications (set by the /PAL terminal).



Note : Unit dot clock (d) is 2 fsc. Numbers in the parentheses are for the PAL mode.

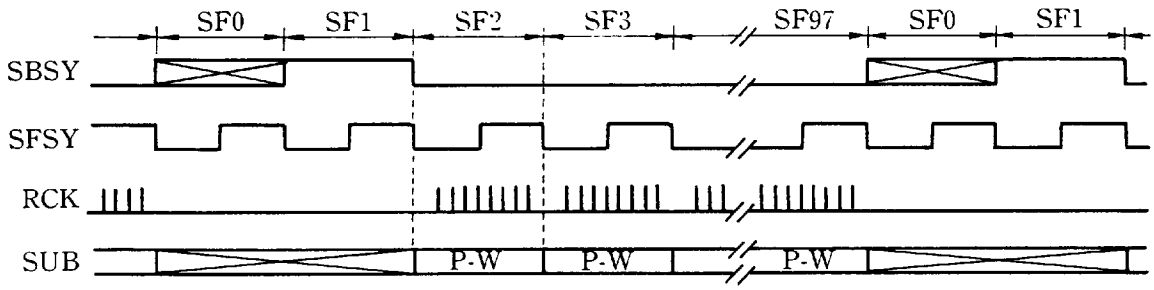
A superimpose timing is output through the YS terminal to execute superimpose. In this case, as synchronization to the external clock is necessary, the clock generated at the PLL is input to the XI terminal. Also, it is so designed that the internal vertical synchronous counter is reset at the fall of the /VRESET terminal so that the vertical synchronous timing is also externally synchronized.

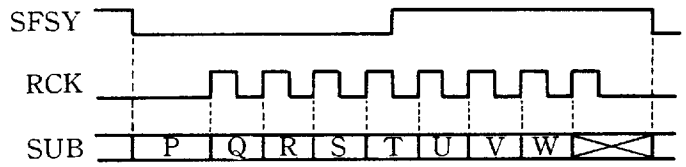
7. System reset /RESET

This LSI requires resetting when turning ON the power. Resetting is done by setting the /RESET terminal to 'L' for 10μs or more.

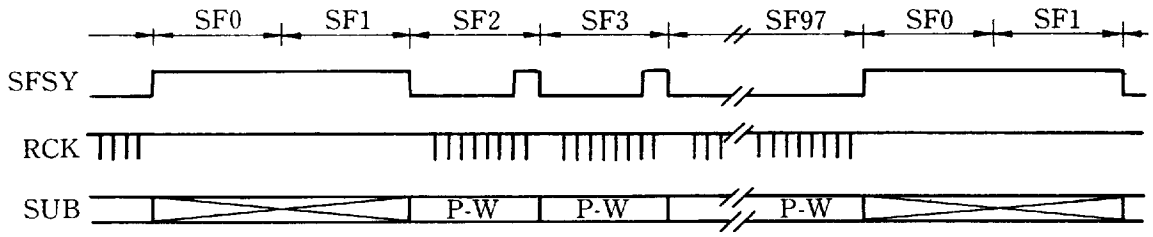
■ SUBCODE INPUT FORMAT

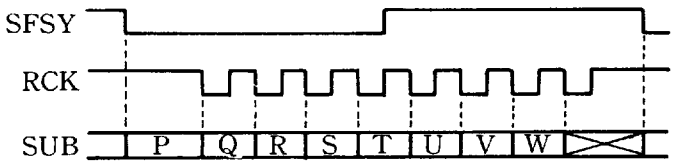
1. EIAJ(1) (/SEL1='H', /SEL0='H')





2. EIAJ(2) (/SEL1='H', /SEL0='L')





■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.5 ~ 7.0	V
Input voltage	V_I	−0.5 ~ V_{DD}+0.5	V
Output current	I_O	−20 ~ 20	mA
Storage temperature	Tstg	−50 ~ 125	°C

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Ta	0	25	70	°C
Clock frequency	f_{XI}	13.54	14.31818	15.03	MHz

3. DC Characteristics (Conditions; Ta=0 ~ 70°C, V_{DD}=5.0 ± 0.25V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	I_{DD}	V_{DD}=5.0V		60		mA
Input voltage, H level (1)	V_{IH1}	*1	2.0			V
Input voltage, H level (2)	V_{IH2}	*2	3.5			V
Input voltage, L level (1)	V_{IL1}	*1			0.8	V
Input voltage, L level (2)	V_{IL2}	*2			1.5	V
Input leak current	I_{LK}				10	μA
Output voltage, H level	V_{OH}	I_{OH}= −1.0mA	3.0			V
Output voltage, L level	V_{OL}	I_{OL}=1.6mA			0.4	V

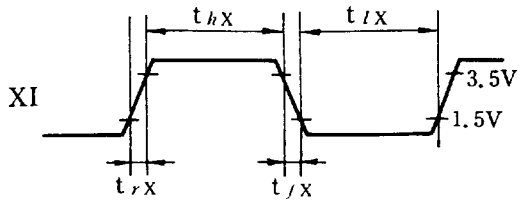
*1) Applicable to input terminals other than XI
*2) Applicable to XI terminal

4. AC Characteristics (Conditions; Ta=0 ~ 70°C, V_{DD}=5.0 ± 0.25V)

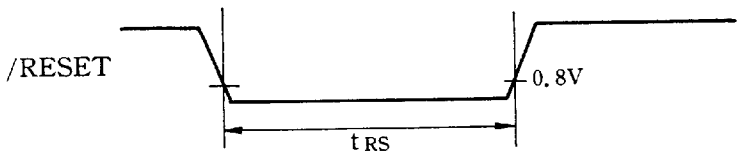
4-1. XI clock, /RESET timing

Parameter		Symbol	Min.	Typ.	Max.	Unit
XI clock	H level time	t_{hX}	18	28		ns
	L level time	t_{lX}	18	28		ns
	Rise time	t_{rX}			10	ns
	Fall time	t_{fX}			10	ns
/RESET pulse width		t_{RS}	10			μs

• XI clock timing



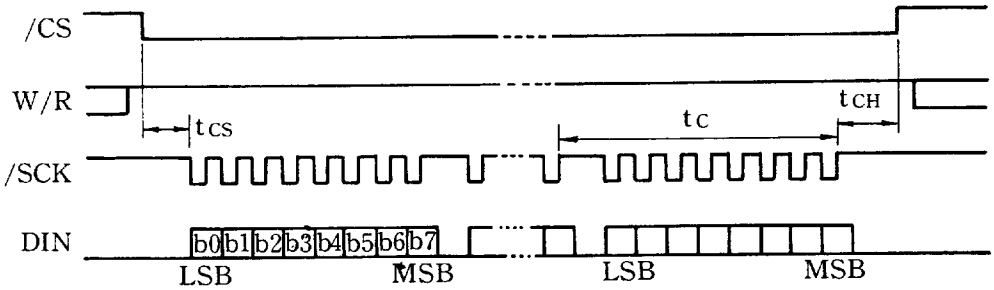
• /RESET timing

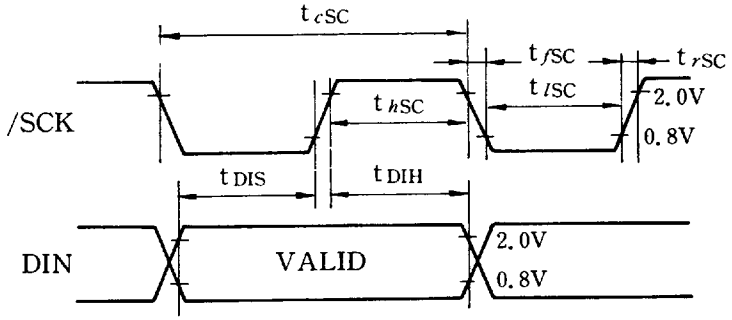


4-2 Microprocessor interface timing

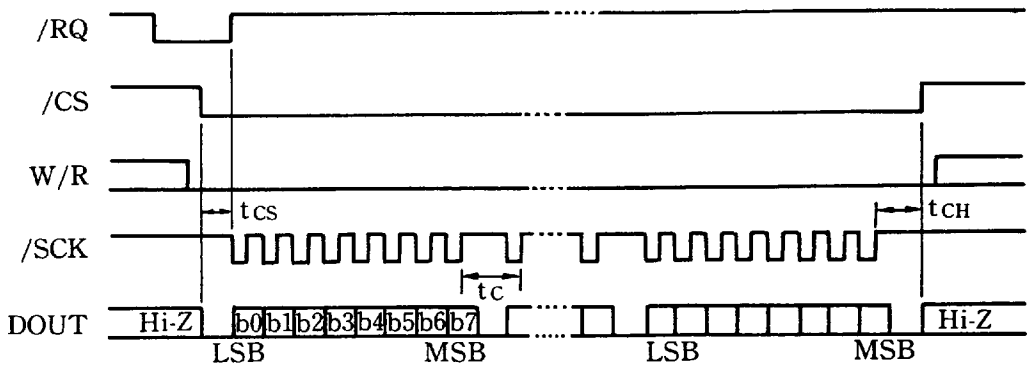
Item	Signal	Min.	Typ.	Max.	Unit
W/R, /CS setup time	t_{CS}	20			ns
W/R, /CS hold time	t_{CH}	1300			ns
Command cycle time	t_C	2250			ns
/SCK Cycle time	t_{cSC}	100			ns
H level period	t_{hSC}	40			ns
L level period	t_{lSC}	40			ns
Rise time	t_{rSC}			10	ns
Fall time	t_{fSC}			10	ns
DIN Setup time	t_{DIS}	30			ns
Hold time	t_{DIH}	30			ns
DOUT Access time	t_{DOA}			30	ns
Hold time	t_{DOH}	630			ns

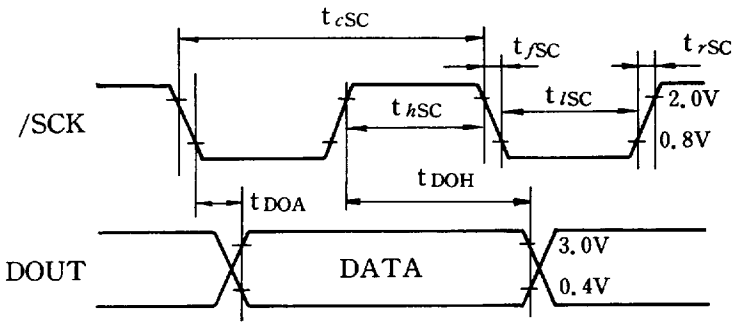
• Command input timing





• Data output timing

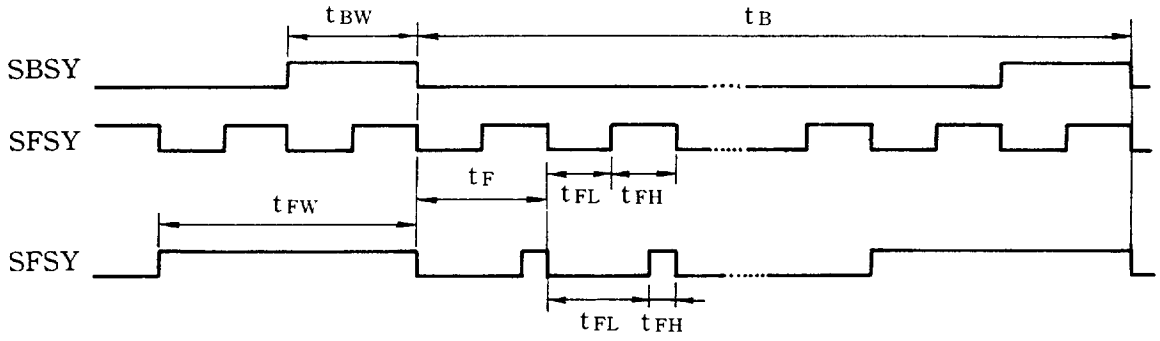


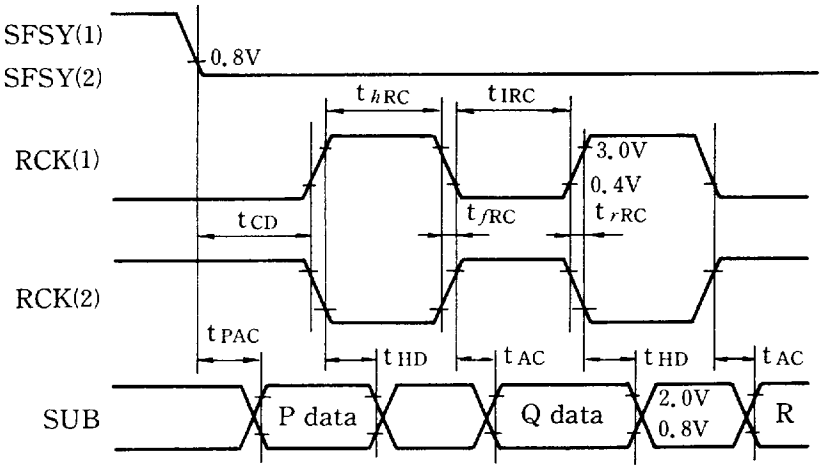


4-3 Subcode interface timing

	Parameter	Symbol	Min.	Typ.	Max.	Unit
SBSY	Block cycle	t_B	12.0	13.3	14.7	ms
	Pulse width	t_{BW}	120			μs
SFSY	Frame cycle	t_F	122	136	150	μs
	Pulse width	t_{FW}	120			μs
	H level period	t_{FH}	2.5			μs
	L level period	t_{FL}	1.0			μs
RCK	H level period	t_{hRC}	4.0	4.5	5.0	μs
	L level period	t_{lRC}	4.0	4.5	5.0	μs
	Rise time	t_{rRC}		10	20	ns
	Fall time	t_{fRC}		10	20	ns
	Output delay time	t_{CD}	23	25	26	μs
	P data access time	t_{PAC}			20	μs
	Data access time	t_{AC}			2.0	μs
	Data hold time	t_{HD}	0			μs

• Subcode input timing





4-4 DRAM interface timing

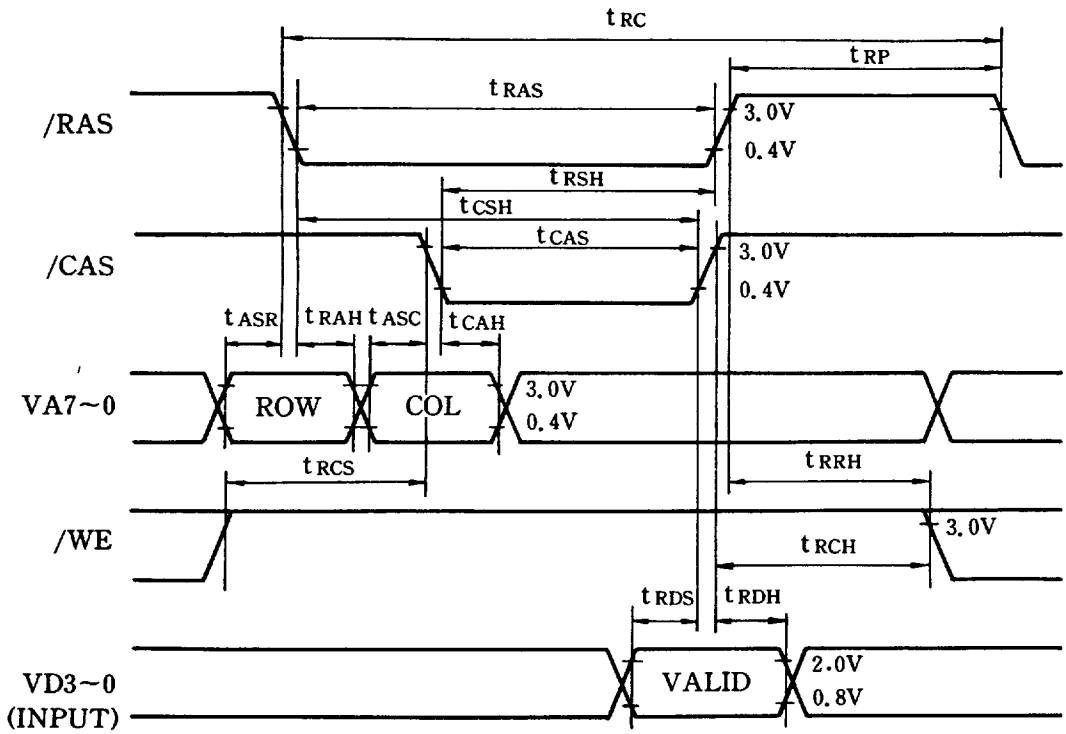
Parameter	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	t_{RC}	279			ns
Page mode cycle time	t_{PC}	139			ns
RAS precharge time	t_{RP}	100			ns
RAS pulse width	t_{RAS}	130			ns
RAS pulse width (when in page mode)	t_{RASP}	130		36000	ns
RAS hold time	t_{RSH}	60			ns
CAS hold time	t_{CSH}	120			ns
CAS pulse width	t_{CAS}	70			ns
CAS precharge time	t_{CPN}	50			ns
CAS precharge time (when in page mode)	t_{CP}	50			ns
Low address setup time	t_{ASR}	50			ns
Low address hold time	t_{RAH}	20			ns
Column address setup time	t_{ASC}	0			ns
Column address hold time	t_{CAH}	50			ns
Read command setup time	t_{RCS}	120			ns
Read command hold time (CAS standard)	t_{RCH}	120			ns
Read command hold time (RAS standard)	t_{RRH}	120			ns

4-4 DRAM interface timing (continued)

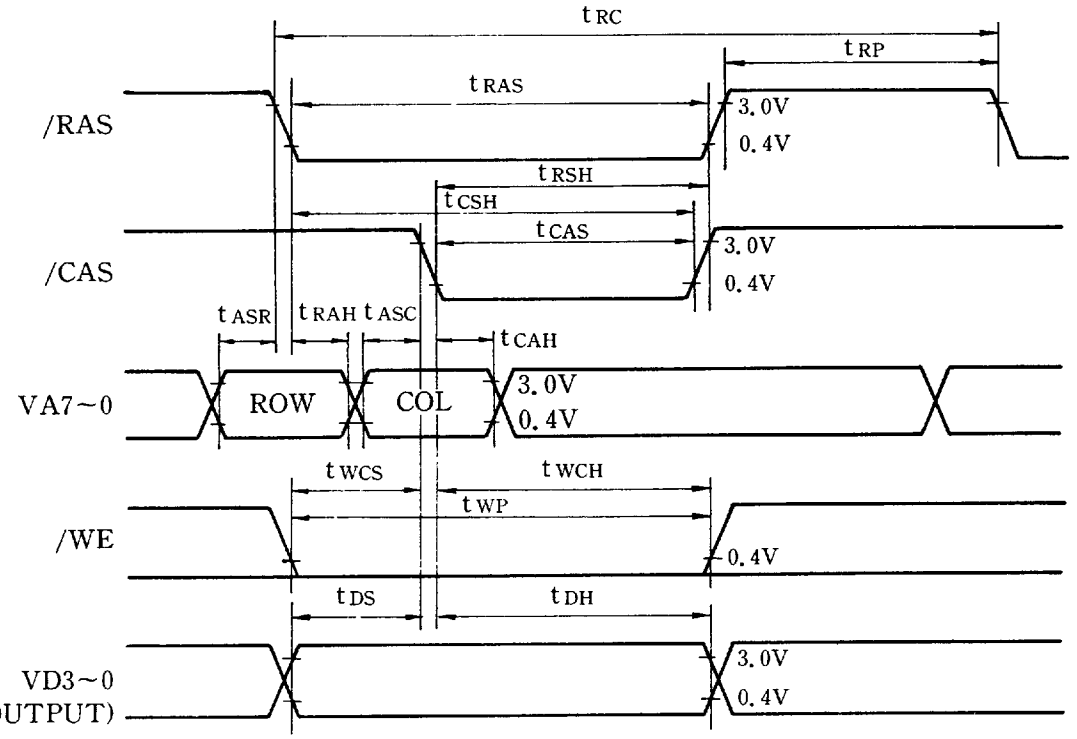
Parameter	Symbol	Min.	Typ.	Max.	Unit
Write command setup time	t_{WCS}	50			ns
Write command hold time	t_{WCH}	50			ns
Write command pulse width	t_{WP}	120			ns
Write data setup time	t_{DS}	50			ns
Write data hold time	t_{DH}	50			ns
CAS setup time (CAS before RAS)	t_{CSR}	50			ns
RAS precharge·CAS active time	t_{RPC}	50			ns
Read data setup time	t_{RDS}	20			ns
Read data hold time	t_{RDH}	0			ns
Refresh time	t_{REF}			3.5	ms

Note: when a 50pF load capacity is connected to the output terminal

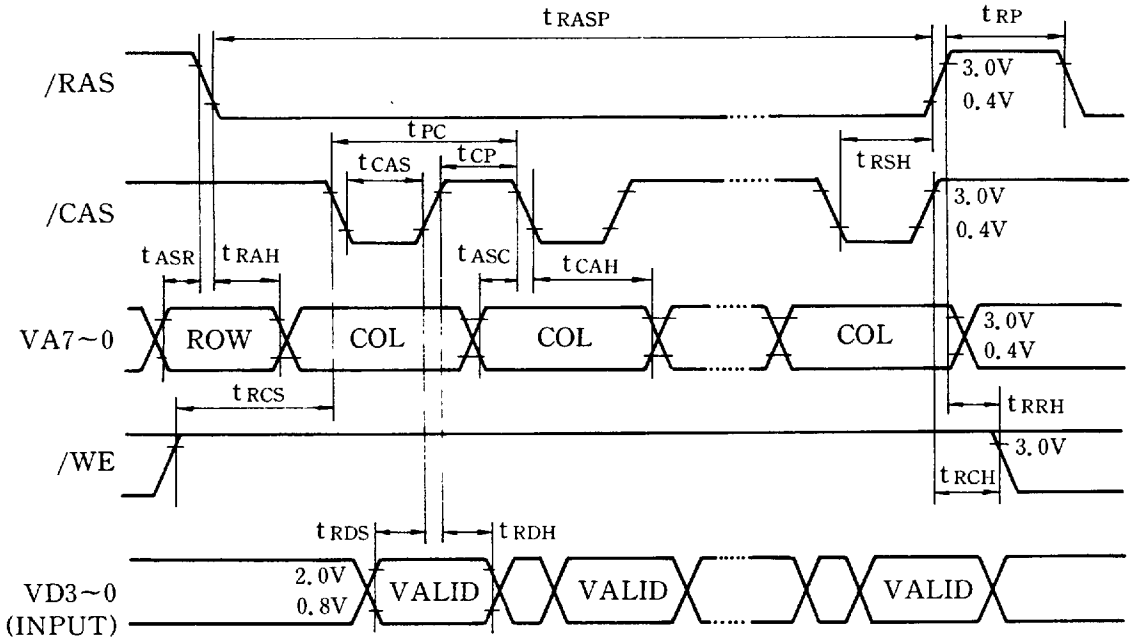
• DRAM read cycle



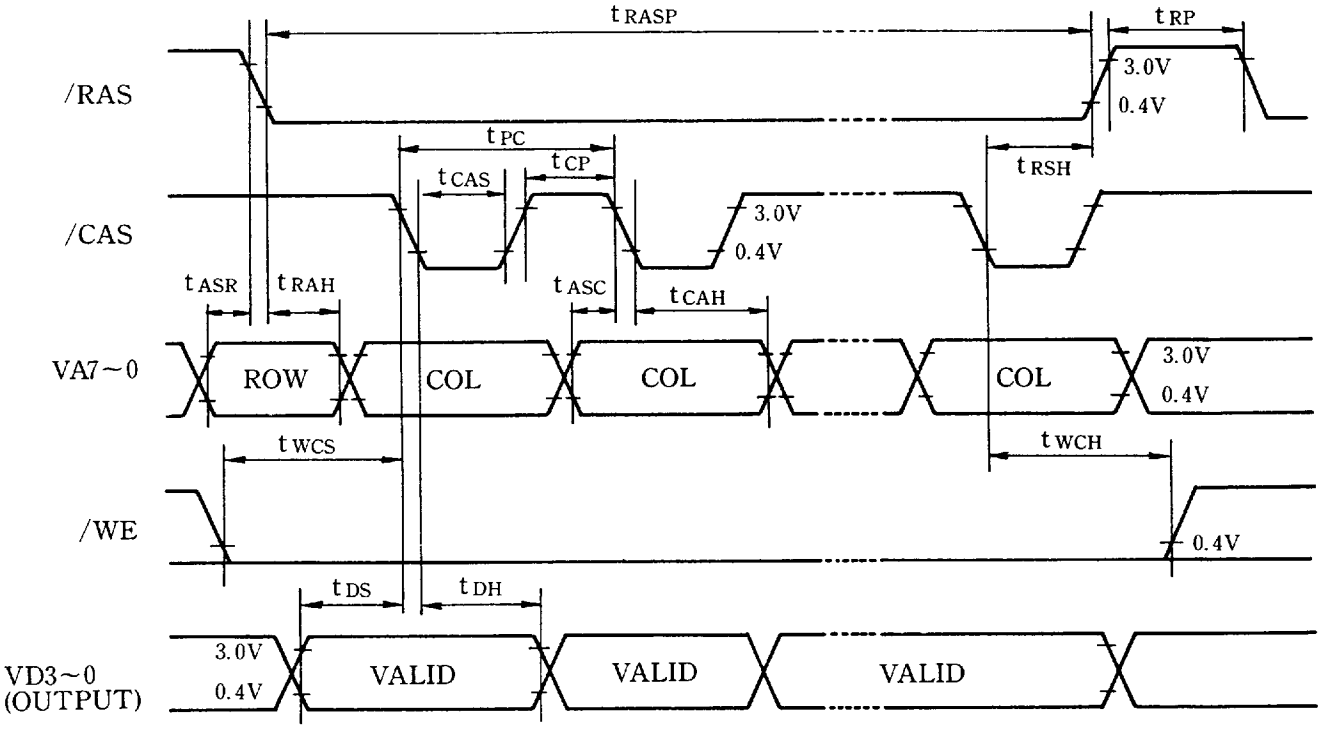
• DRAM early write cycle



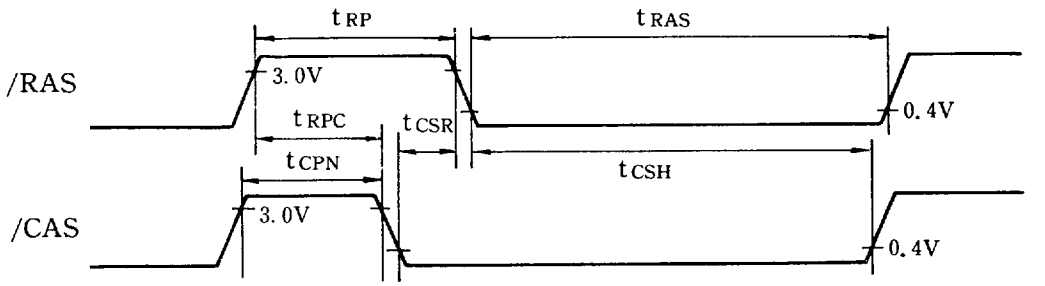
• DRAM page mode read cycle



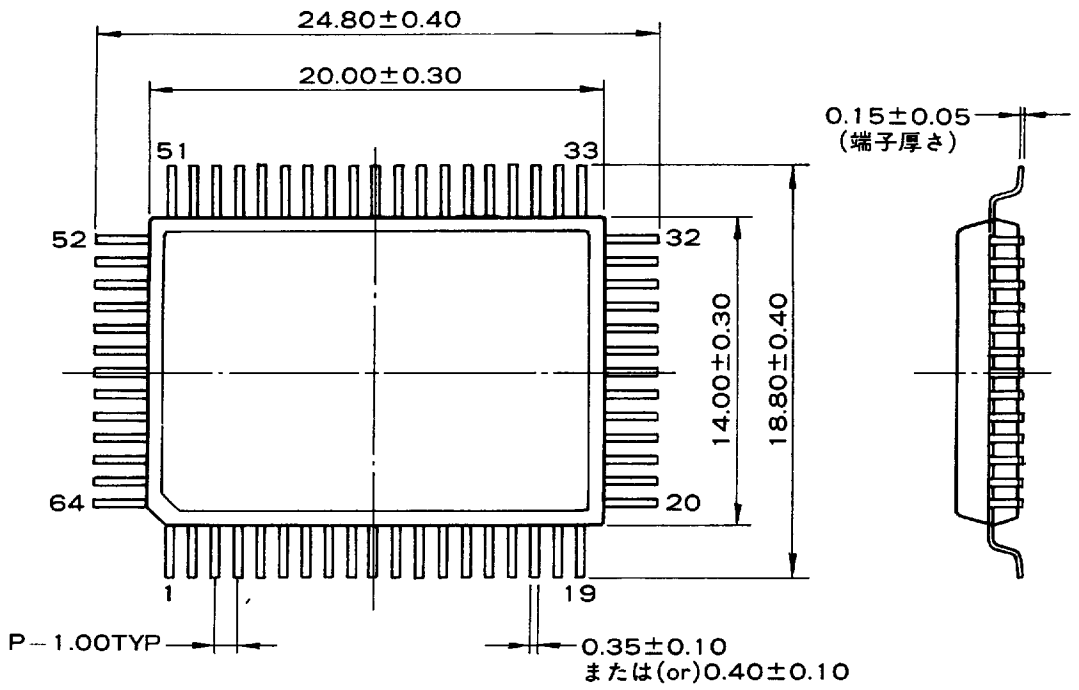
• DRAM page mode write cycle

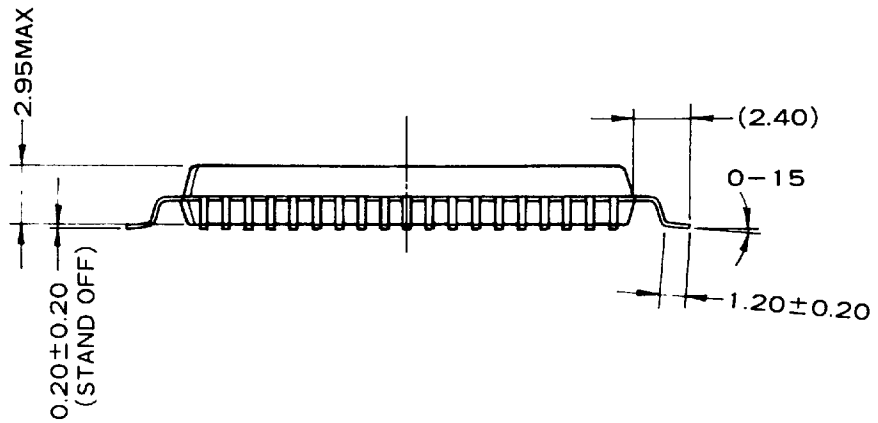


• DRAM CAS before RAS refresh cycle



■ DIMENSIONAL DRAWING





Unit : mm

Note: Specifications of this product are subject to improvement changes without prior notice.

AGENCY

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