74HC138

GENERAL DESCRIPTION

The 74HC138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC138 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled,provide 8 mutually exclusive active LOW outputs (Y_0toY_7).

The “138” features three enable inputs: two active LOW(E_1 and E_2) and one active HIGH (E_3). Every output will be HIGH unless E_1 and E_2 are LOW and E_3 is HIGH.This multiple enable function allows easy parallelexpansion of the “138” to a 1-of-32 (5 lines to 32 lines)decoder with just four “138” ICs and one inverter.

The ”138” can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The ”138” is identical to the “238” but has inverting outputs.

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- ICC category: MSI

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	E_1, E_2	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
7，9-15	Y_0 to Y_7	outputs (active LOW)
16	V_{CC}	positive supply voltage

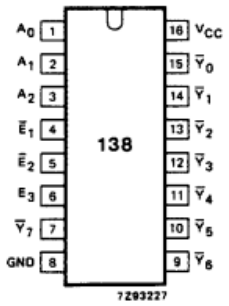


Fig.1 Pin configuration.

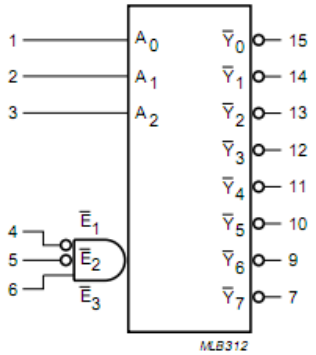


Fig.2 Logic symbol.

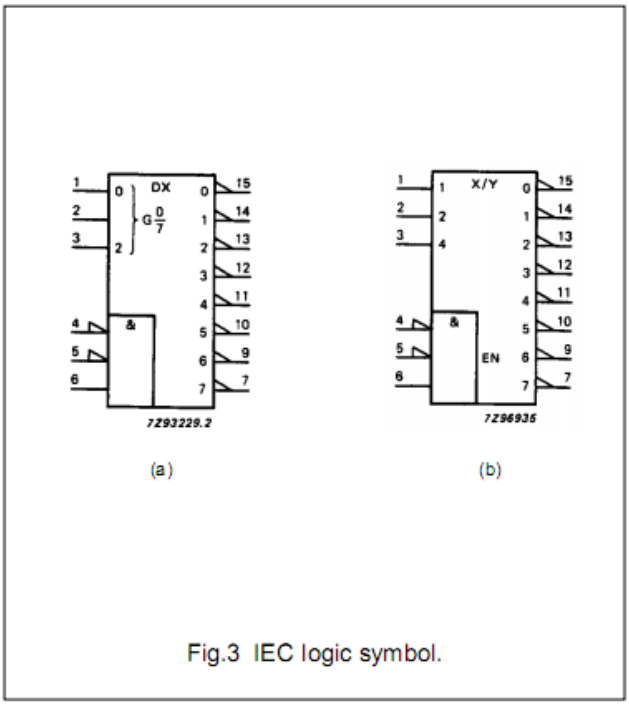


Fig.3 IEC logic symbol.

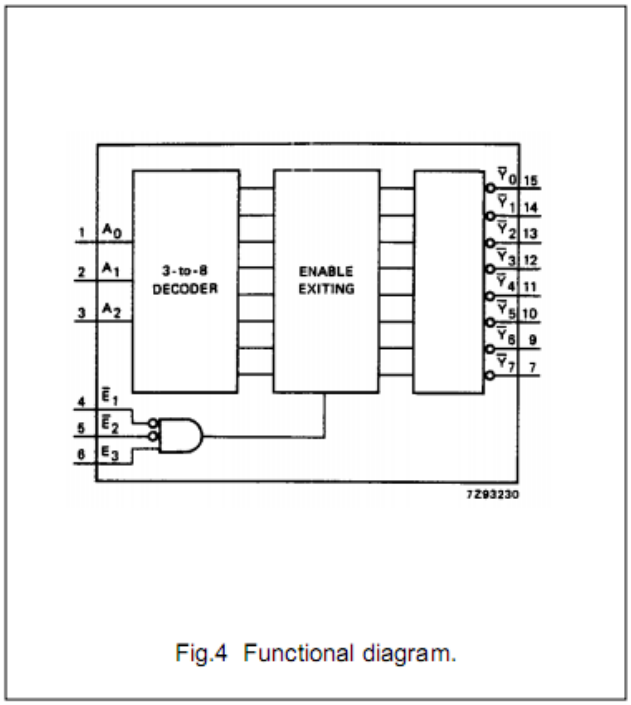


Fig.4 Functional diagram.

QUICK REFERENCE DATA

GND = 0 V; Tamb = 25 °C; tr = tf = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/ t_{PLH} t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n E_3 to Y_n E_n to Y_n	C_L = 15 pF; V_{CC} = 5 V	12 14	ns ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	67	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}2 \times fi + \Sigma$ (CL × $V_{CC}2$ × fo) where:

   f_i= input frequency in MHz

   f_o = output frequency in MHz

   Σ ($C_L \times V_{CC}2 \times fo$) = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} − 1.5

FUNCTION TABLE

INPUTS						OUTPUTS							
E1	E2	E3	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

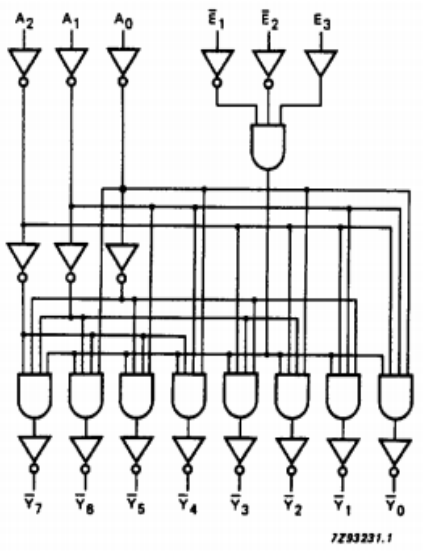


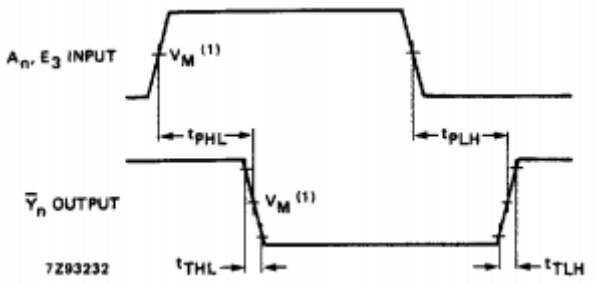
Fig.5 Logic diagram.

AC CHARACTERISTICS

GND = 0 V; tr = t_f = 6 ns; C_L = 50 pF

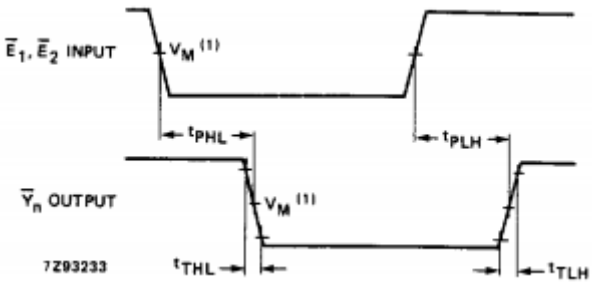
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to 125			V_{CC} (V)	WAVEFORMS
		min.	Typ	max.	min	max.	min	max			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n		41 15 12	150 30 26		190 38 33		225 45 38	na	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation de E_3 to Y_n		47 17 14	150 30 26		190 38 33		225 45 38	na	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay E_n to Y_n		47 17 14	150 30 26		190 38 33		225 45 38	na	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	na	2.0 4.5 6.0	Figs 6 and 7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.

Fig.6 Waveforms showing the address input (A_n) and enable input (E_3) to output (Y_n) propagation delays and the output transition times



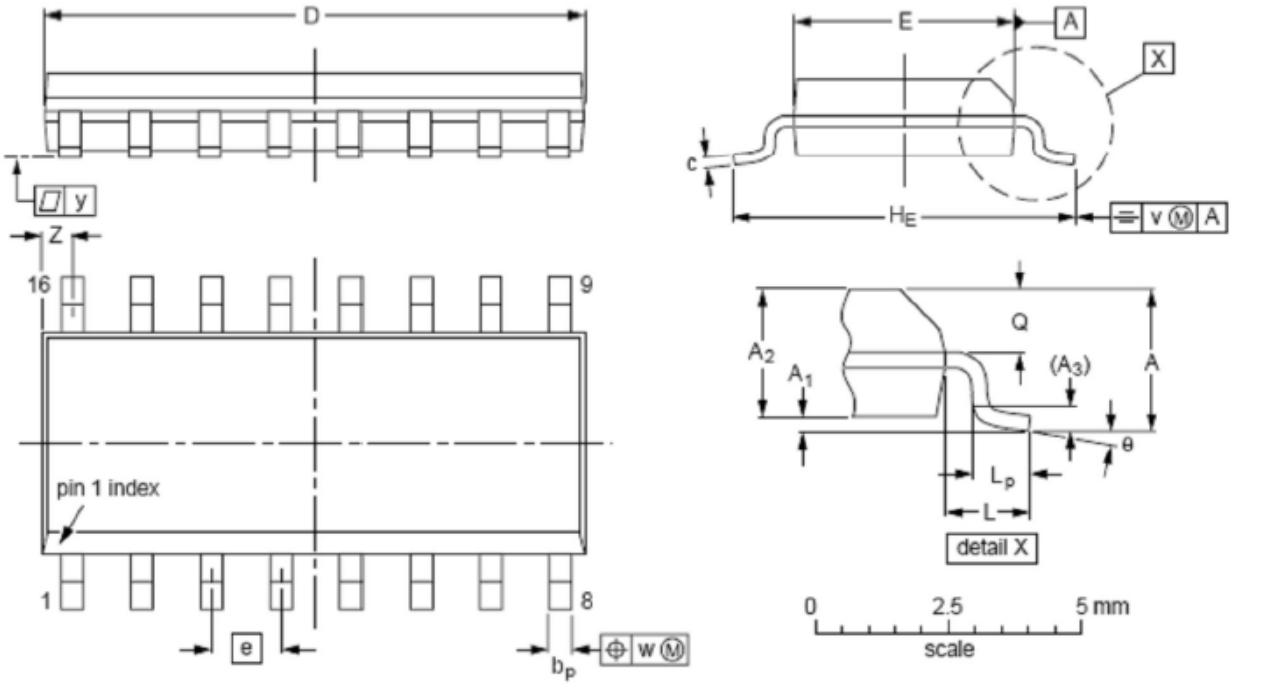
(1) HC : V_M = 50%; V_I = GND to V_{CC}.

HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the enable input (E_n) to output (Y_n) propagation delays and the output transition times.

PACKAGE DESCRIPTION

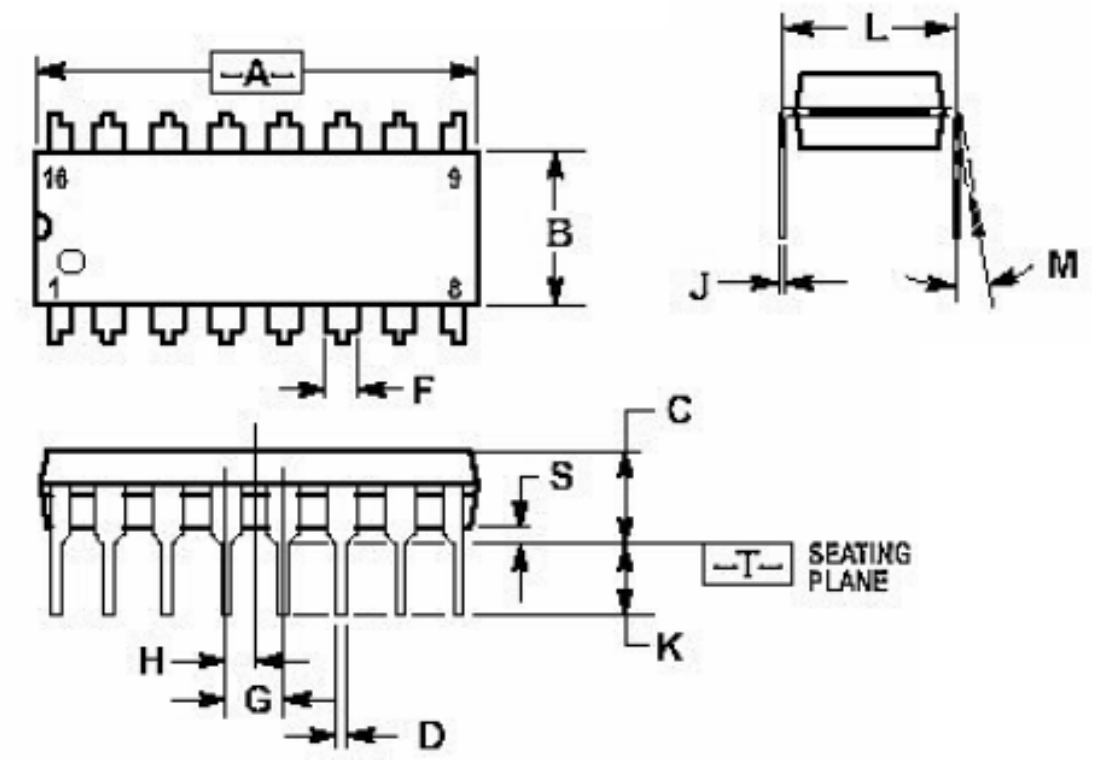
SOP16 PACKAGE OUTLINE DIMENSIONS



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

DIP16 PACKAGE OUTLINE DIMENSIONS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.78
G	0.100BSC		2.54BSC	
H	0.050BSC		1.27BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01