2nd 128M DDR SDRAM

HY5DU28422T
HY5DU28822T
HY5DU281622T

Revision 1.3

April 2001

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128Mb (x4, x8, x16) Double Data Rate SDRAM

DESCRIPTION

The Hynix HY5DU28422, HY5DU28822 and HY5DU281622 are a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

The Hynix 128Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

FEATURES

- V_{DD}, V_{DDQ} = 2.5V +/- 0.2V
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has two bytewide data strobes (UDQS, LDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable $\overline{CAS}$ latency 2 and 2.5 supported
- Programmable burst length 2 / 4 / 8 with both sequential and interleave mode
- Internal four bank operations with single pulsed $\overline{RAS}$
- Auto refresh and self refresh supported
- 4096 refresh cycles / 64ms
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Full strength driver option controlled by EMRS

ORDERING INFORMATION

Part No.	Configuration	Power
HY5DU28422T-X*	32Mx4	Standard
HY5DU28422LT-X*	32Mx4	Low Power
HY5DU28822T-X*	16Mx8	Standard
HY5DU28822LT-X*	16Mx8	Low Power
HY5DU281622T-X*	8Mx16	Standard
HY5DU281622LT-X*	8Mx16	Low Power

OPERATING FREQUENCY

Grade	CL2	CL2.5	Remark**
- H	125MHz	133MHz	DDR266B
- L	100MHz	125MHz	DDR200

* X means speed grade

** JEDEC specification compliant

PIN CONFIGURATION

x4	x8	x16			x16	x8	x4
VDD	VDD	VDD	1	66	VSS	VSS	VSS
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	NC	NC	NC
VDD	VDD	VDD	18	49	VREF	VREF	VREF
DNU	DNU	DNU	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
/WE	/WE	/WE	21	46	/CK	/CK	/CK
/CAS	/CAS	/CAS	22	45	CK	CK	CK
/RAS	/RAS	/RAS	23	44	CKE	CKE	CKE
/CS	/CS	/CS	24	43	NC	NC	NC
NC	NC	NC	25	42	NC	NC	NC
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

400mil X 875mil
66pin TSOP -II
0.65mm pin pitch

ROW AND COLUMN ADDRESS TABLE

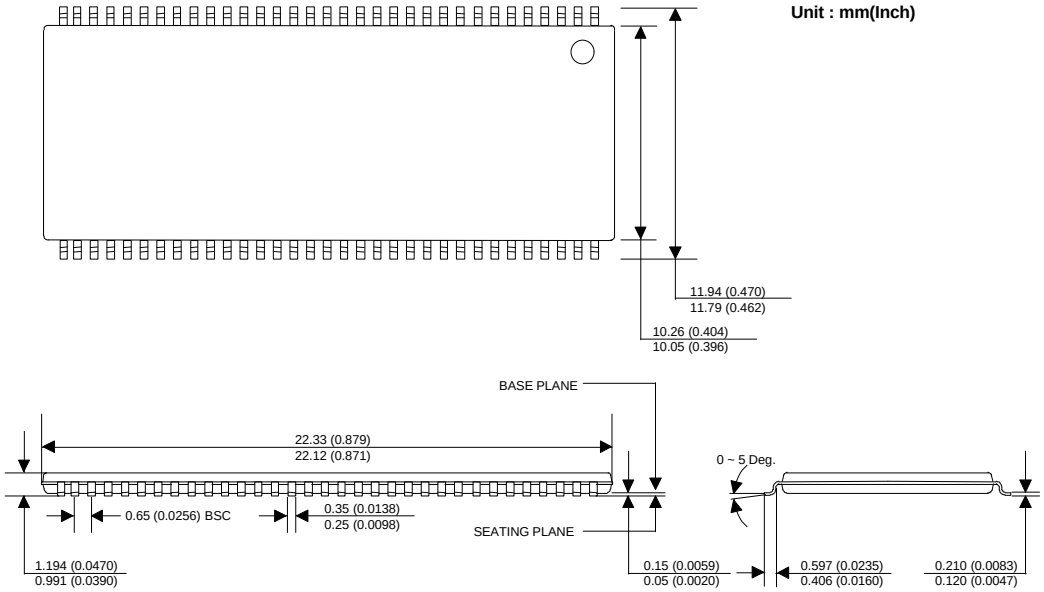
ITEMS	32Mx4	16Mx8	8Mx16
Organization	8M x 4 x 4banks	4M x 8 x 4banks	2M x 16 x 4banks
Row Address	A0 - A11	A0 - A11	A0 - A11
Column Address	A0-A9, A11	A0-A9	A0-A8
Bank Address	BA0, BA1	BA0, BA1	BA0, BA1
Auto Precharge Flag	A10	A10	A10
Refresh	4K	4K	4K

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied.
/CS	Input	Chip Select : Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM (LDM,UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
DQS (LDQS,UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ	I/O	Data input / output pin : Data bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

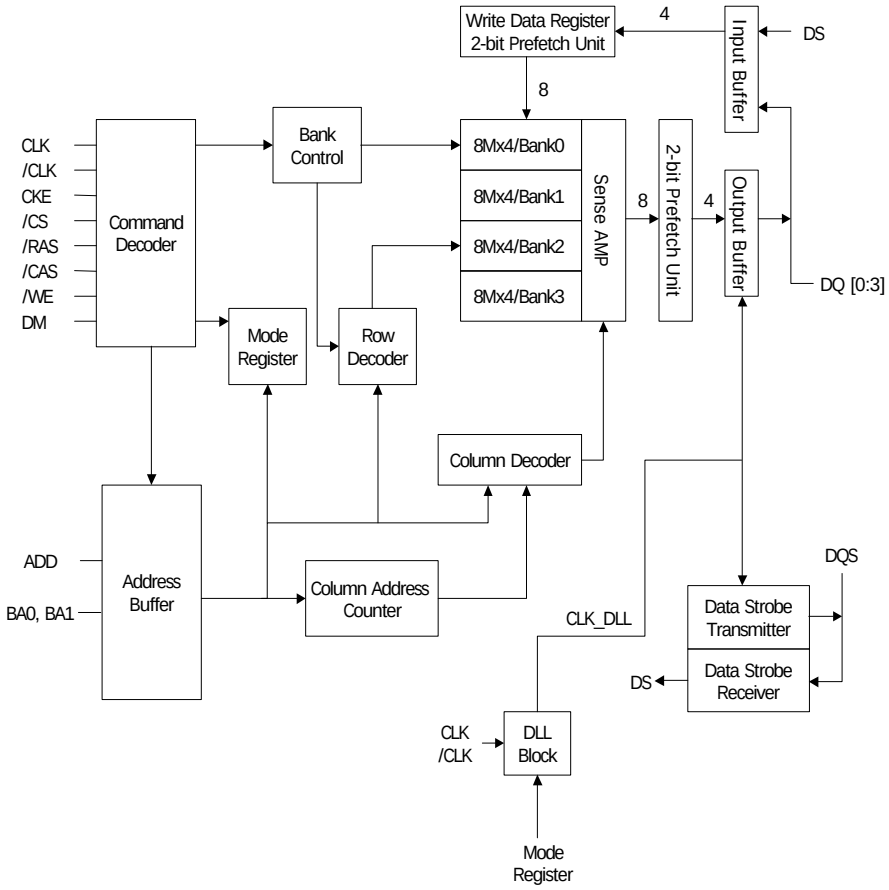
PACKAGE INFORMATION

400mil 66pin Thin Small Outline Package



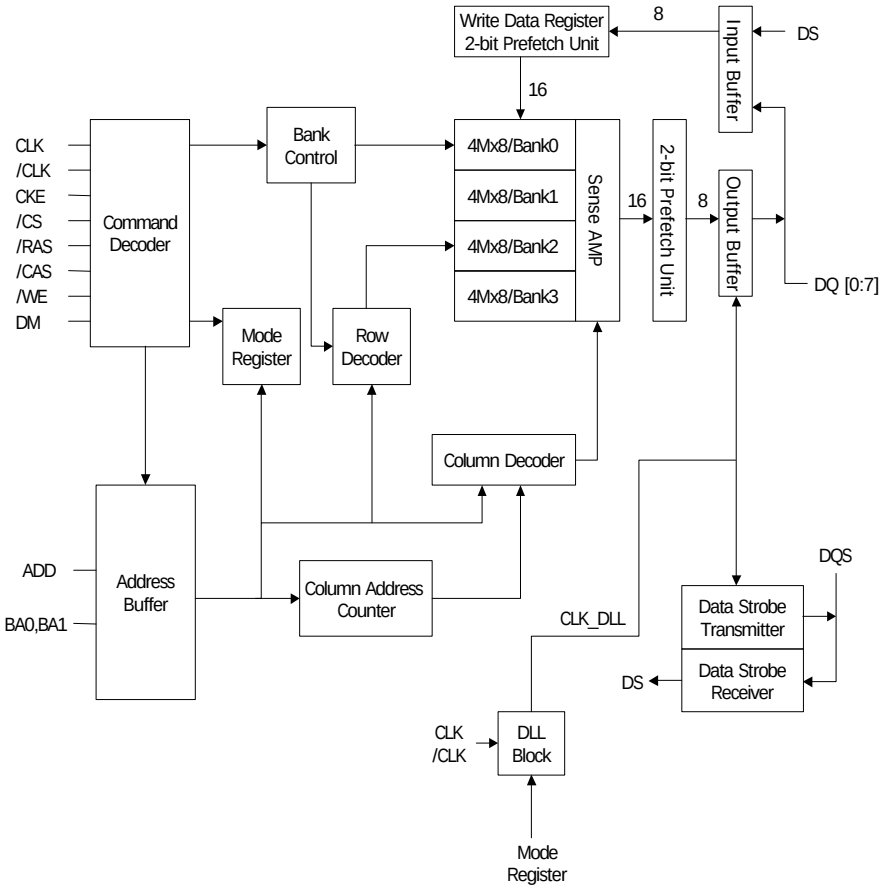
FUNCTIONAL BLOCK DIAGRAM (32Mx4)

4Banks x 8Mbit x 4 I/O Double Data Rate Synchronous DRAM



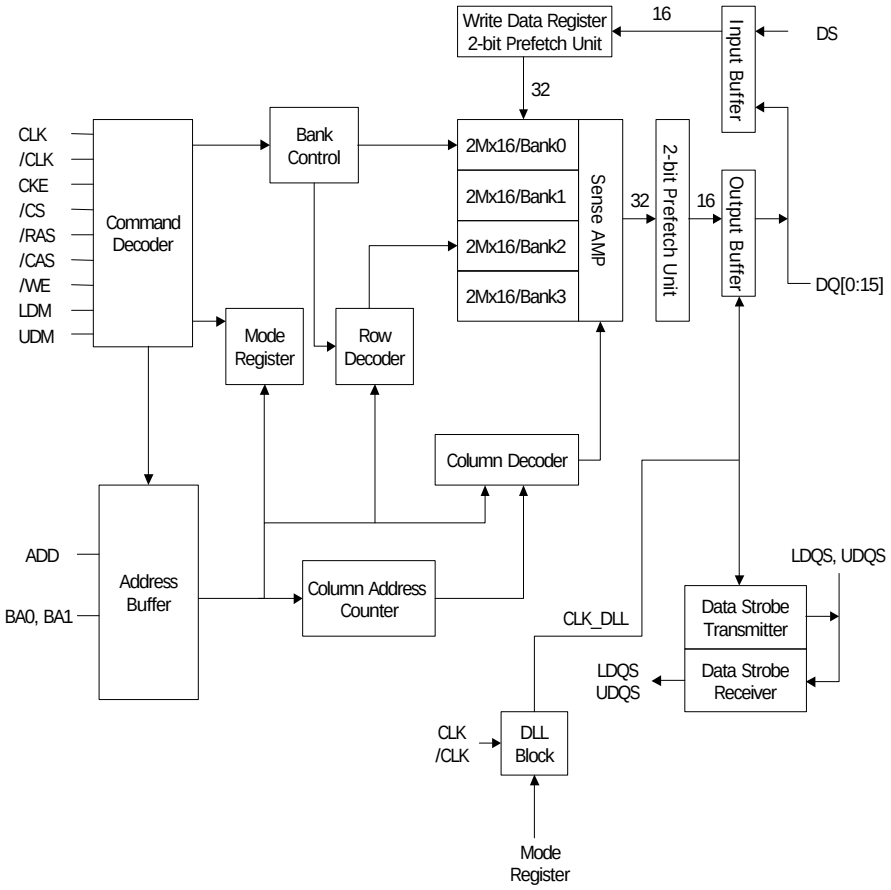
FUNCTIONAL BLOCK DIAGRAM (16Mx8)

4Banks x 4Mbit x 8 I/O Double Data Rate Synchronous DRAM



FUNCTIONAL BLOCK DIAGRAM (8Mx16)

4Banks x 2Mbit x 16 I/O Double Data Rate Synchronous DRAM



SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	A10/AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting duing Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	DM	ADDR	A10/ AP	BA	Note
Data Write	H	X	X	L	X			1
Data-In Mask	H	X	X	H	X			1

Note :

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strobes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.

OPERATION COMMAND TRUTH TABLE-I

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DSEL	NOP or power down[3]
	L	H	H	H	X	NOP	NOP or power down[3]
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4]
	L	L	H	H	BA, RA	ACT	Row Activation
	L	L	H	L	BA, AP	PRE/PALL	NOP
	L	L	L	H	X	AREF/SREF	Auto Refresh or Self Refresh[5]
	L	L	L	L	OPCODE	MRS	Mode Register Set
ROW ACTIVE	H	X	X	X	X	DSEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	Begin read : optional AP[6]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	Begin write : optional AP[6]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Precharge[7]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
READ	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Terminate burst
	L	H	L	H	BA, CA, AP	READ/READAP	Term burst, new read:optional AP[8]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	Term burst, new read:optional AP[8]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	Term burst, new write:optional AP

OPERATION COMMAND TRUTH TABLE-II

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
READ WITH AUTOPRE-CHARGE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE AUTOPRE-CHARGE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
PRE-CHARGE	H	X	X	X	X	DSEL	NOP-Enter IDLE after tRP
	L	H	H	H	X	NOP	NOP-Enter IDLE after tRP
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	NOP-Enter IDLE after tRP
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]

OPERATION COMMAND TRUTH TABLE-III

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
ROW ACTIVATING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tRCD
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tRCD
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,9,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE RECOVERING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tWR
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tWR
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE RECOVERING WITH AUTOPRE-CHARGE	H	X	X	X	X	DSEL	NOP - Enter precharge after tDPL
	L	H	H	H	X	NOP	NOP - Enter precharge after tDPL
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,8,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
REFRESHING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tRC
	L	H	H	H	X	NOP	NOP - Enter IDLE after tRC
	L	H	H	L	X	BST	ILLEGAL[11]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[11]

OPERATION COMMAND TRUTH TABLE-IV

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[11]
	L	L	H	H	BA, RA	ACT	ILLEGAL[11]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
MODE REGISTER ACCESSING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tMRD
	L	H	H	H	X	NOP	NOP - Enter IDLE after tMRD
	L	H	H	L	X	BST	ILLEGAL[11]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[11]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[11]
	L	L	H	H	BA, RA	ACT	ILLEGAL[11]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]

Note :

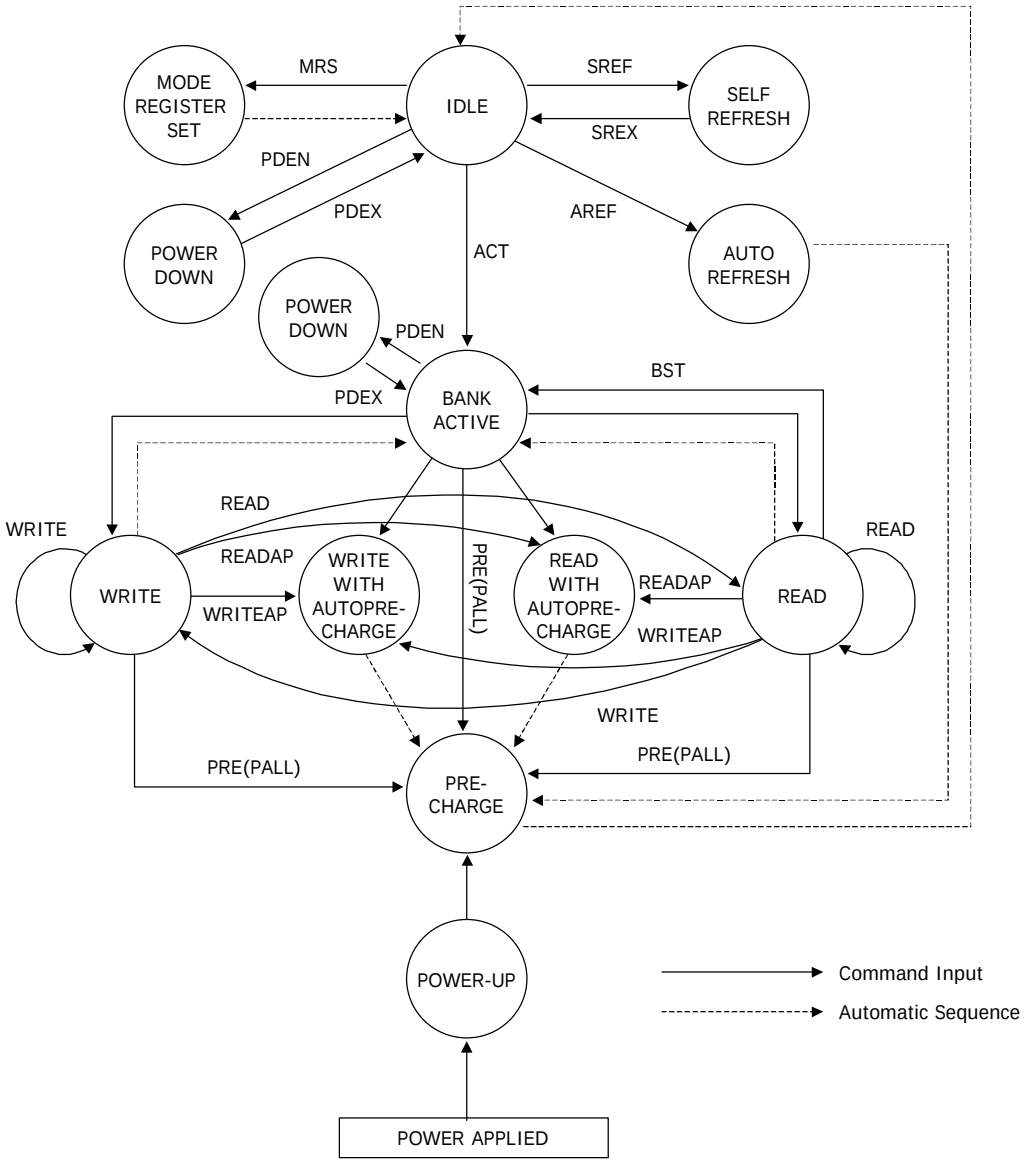
1. H - Logic High Level, L - Logic Low Level, X - Don't Care, V - Valid Data Input,
   BA - Bank Address, AP - AutoPrecharge Address, CA - Column Address, RA - Row Address, NOP - NO Operation.
2. All entries assume that CKE was active(high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive(low level), then in power down mode.
4. Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA) depending on the state of that bank.
5. If both banks are idle and CKE is inactive(low level), then self refresh mode.
6. Illegal if tRCD is not met.
7. Illegal if tRAS is not met.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Illegal if tRRD is not met.
10. Illegal for single bank, but legal for other banks in multi-bank devices.
11. Illegal for all banks.

CKE FUNCTION TRUTH TABLE

Current State	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	/ADD	Action
SELF REFRESH [1]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit self refresh, enter idle after tSREX
	L	H	L	H	H	H	X	Exit self refresh, enter idle after tSREX
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue self refresh
POWER DOWN [2]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit power down, enter idle
	L	H	L	H	H	H	X	Exit power down, enter idle
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue power down mode
ALL BANKS IDLE [4]	H	H	X	X	X	X	X	See operation command truth table
	H	L	L	L	L	H	X	Enter self refresh
	H	L	H	X	X	X	X	Exit power down
	H	L	L	H	H	H	X	Exit power down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
ANY STATE OTHER THAN ABOVE	H	H	X	X	X	X	X	See operation command truth table
	H	L	X	X	X	X	X	ILLEGAL [5]
	L	H	X	X	X	X	X	INVALID
	L	L	X	X	X	X	X	INVALID

Note :
When CKE=L, all DQ and DQS must be in Hi-Z state.
1. CKE and /CS must be kept high for a minimum of 200 stable input clocks before issuing any command.
2. All command can be stored after 2 clocks from low to high transition of CKE.
3. Illegal if CLK is suspended or stopped during the power down mode.
4. Self refresh can be entered only from the all banks idle state.
5. Disabling CLK may cause malfunction of any bank which is in active state.

SIMPLIFIED STATE DIAGRAM



POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied anytime after VDDQ, but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any command. During the 200 cycles of CK, for DLL locking, executable commands are disallowed (a DESELECT or NOP command must be applied). After the 200 clock cycles, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

1. Apply power - VDD, VDDQ, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVCMOS low state. (All the other input pins may be undefined.)

   - VDD and VDDQ are driven from a single power converter output.
   - VTT is limited to 1.44V (reflecting VDDQ(max)/2 + 50mV VREF variation + 40mV VTT variation.
   - VREF tracks VDDQ/2.
   - A minimum resistance of 42 Ohms (22 ohm series resistor + 22 ohm parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.
   - If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up.

Voltage description	Sequencing	Voltage relationship to avoid latch-up
VDDQ	After or with VDD	< VDD + 0.3V
VTT	After or with VDDQ	< VDDQ + 0.3V
VREF	After or with VDDQ	< VDDQ + 0.3V

2. Start clock and maintain stable clock for a minimum of 200usec.

3. After stable power and clock, apply NOP condition and take CKE high.

4. Issue Extended Mode Register Set (EMRS) to enable DLL.

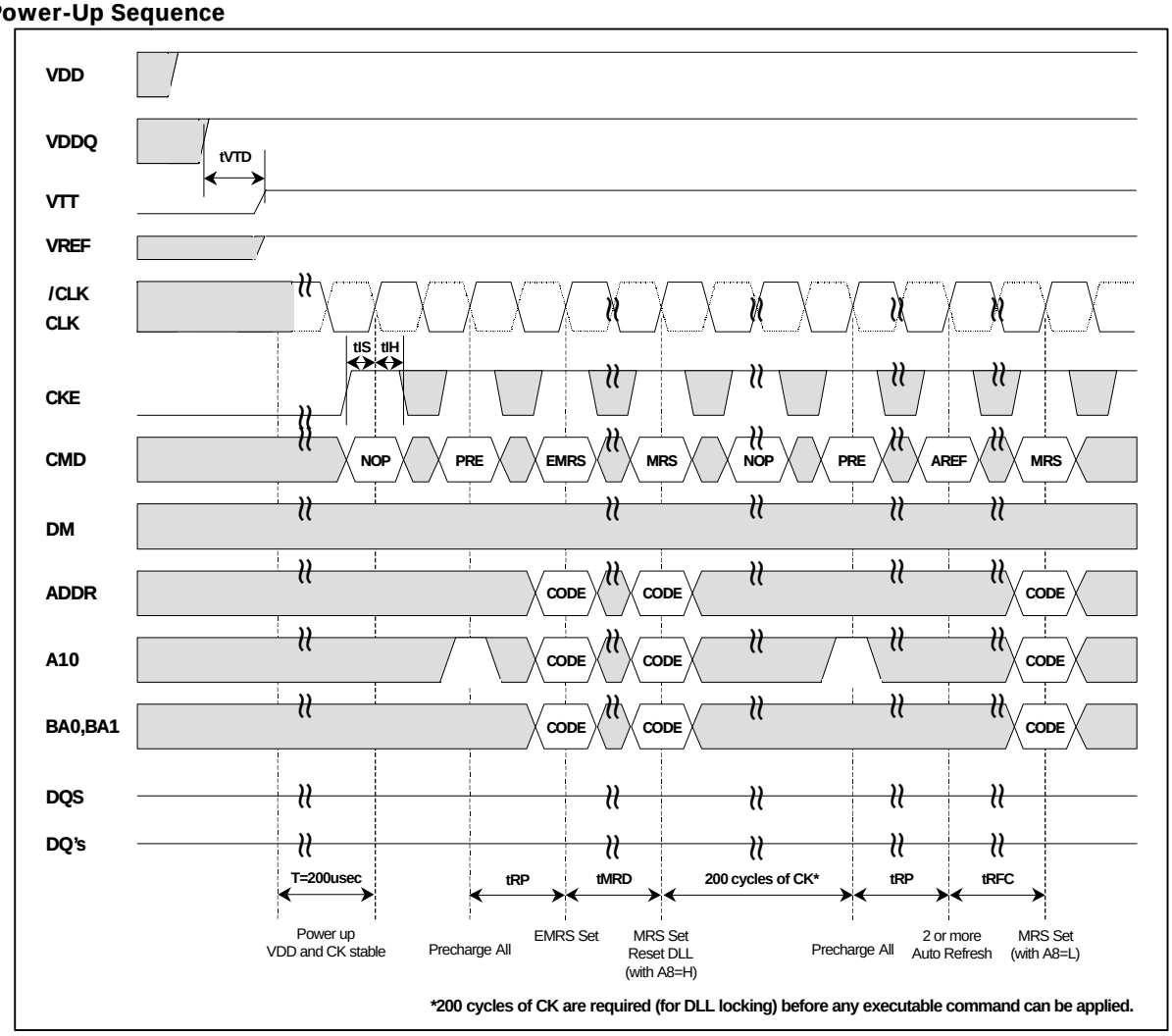
5. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=high. (An additional 200 cycles of clock are required for locking DLL)

6. Issue Precharge commands for all banks of the device.

7. Issue 2 or more Auto Refresh commands.

8. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low.

Power-Up Sequence



MODE REGISTER SET (MRS)

The mode register is used to store the various operating modes such as /CAS latency, addressing mode, burst length, burst type, test mode, DLL reset. The mode register is programed via MRS command. This command is issued by the low signals of /RAS, /CAS, /CS, /WE and BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Two cycles are required to write the data in mode register. During the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until resetted by another MRS command.

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	RFU			DR	TM	CAS Latency			BT	Burst Length		

BA0	MRS Type
0	MRS
1	EMRS

A7	Test Mode
0	Normal
1	Vendor test mode

A8	DLL Reset
0	No
1	Yes

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A2	A1	A0	Burst Length	
			Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

A3	Burst Type
0	Sequential
1	Interleave

BURST DEFINITION

Burst Length	Starting Address (A2,A1,A0)	Sequential	Interleave
2	XX0	0, 1	0, 1
	XX1	1, 0	1, 0
4	X00	0, 1, 2, 3	0, 1, 2, 3
	X01	1, 2, 3, 0	1, 0, 3, 2
	X10	2, 3, 0, 1	2, 3, 0, 1
	X11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	0, 1, 2, 3, 4, 5, 6, 7	7, 6, 5, 4, 3, 2, 1, 0

BURST LENGTH & TYPE

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A 2 -Ai when the burst length is set to four and by A 3 -Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definitionon Table

CAS LATENCY

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks.

If a Read command is registered at clock edge n, and the latency is m clocks, the data is available nominally coincident with clock edge n + m.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DLL RESET

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before an any command can be issued.

OUTPUT DRIVER IMPEDANCE CONTROL

The normal drive strength for all outputs is specified to be SSTL_2, Class II. I-V curves of the full strength driver is included in this document.

EXTENDED MODE REGISTER SET (EMRS)

The mode register is used to store the various operating modes such as /CAS latency, addressing mode, burst length, burst type, test mode, DLL reset. The mode register is program via MRS command. This command is issued by the low signals of /RAS, /CAS, /CS , /WE and BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Two cycles are required to write the data in mode register. During the the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until resetted by another MRS command.

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	RFU*									0**	DS	DLL

BA0	MRS Type
0	MRS
1	EMRS

A0	DLL enable
0	Enable
1	Diable

A1	Output Driver Impedance Control
0	Full Strength Driver
1	Half Strength Driver

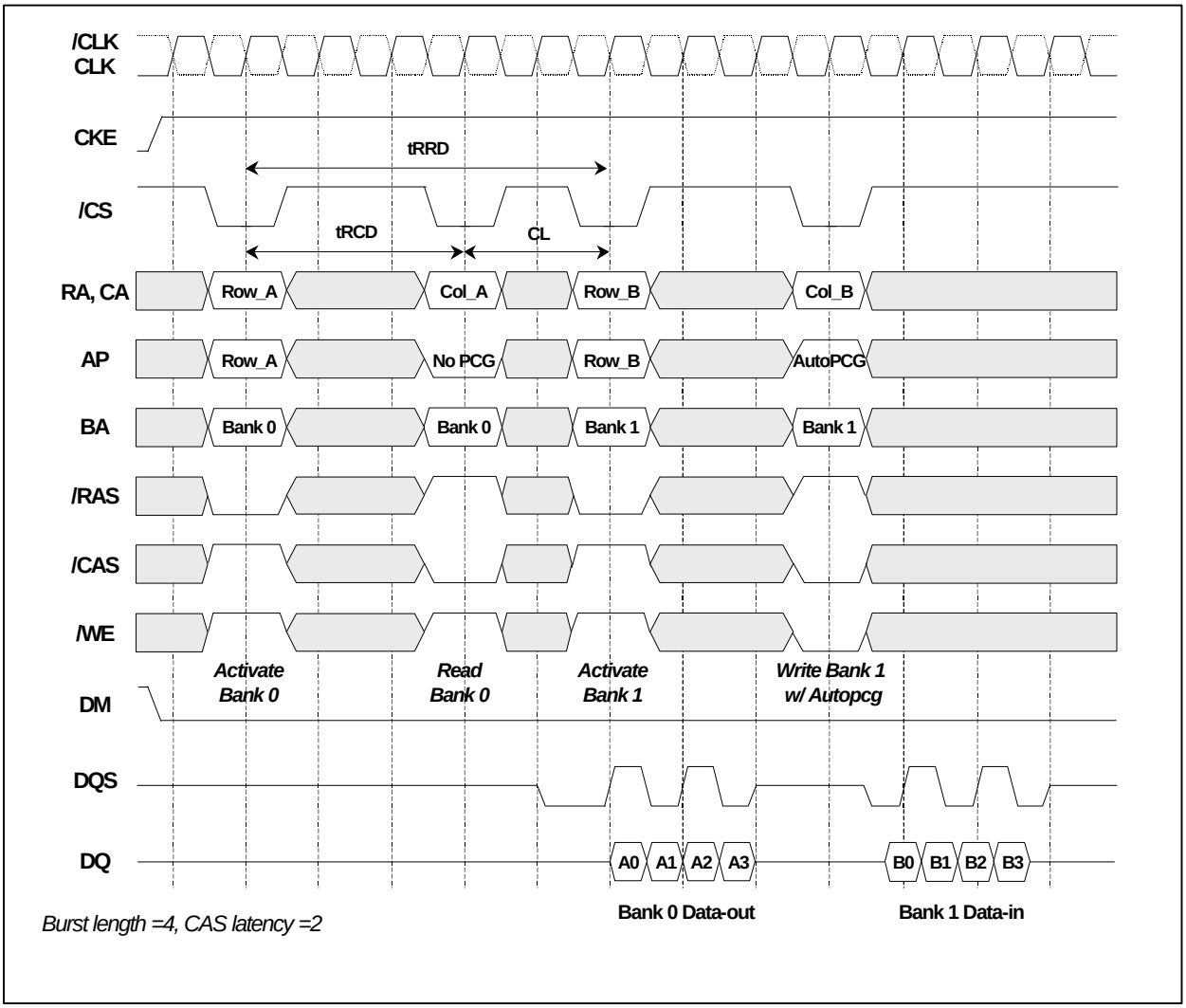
* All bits in RFU address fields must be programmed to Zero, all other states are reserved for future usage
** This part do not support /QFC function, A2 must be programmed to Zero.

FUNCTION DESCRIPTION

Burst Read and Burst Write

Burst Read and Burst Write commands are initiated as listed in Fig.1. Before the Burst Read command, the bank must be activated earlier. After /RAS to /CAS delay (tRCD), read operation starts. DDR SDRAM has been implemented with Data Strobe signal (DQS) which toggles high and low during burst with the same frequency as clock (CLK, /CLK). After CAS Latency (CL) which is defined as the interval between command clock and the first rising edge of the DQS, read data is launched onto data pin (DQ) with reference to DQS signal edge. Burst Write command in another bank can be given with having activated that bank where /RAS to /RAS delay (tRRD) is satisfied. Write data is also referenced and aligned to the DQS signal sent from the memory controller. Since all read operation bursts data out at both the rising and the falling of the DQS, double data bandwidth can be achieved, also for write data.

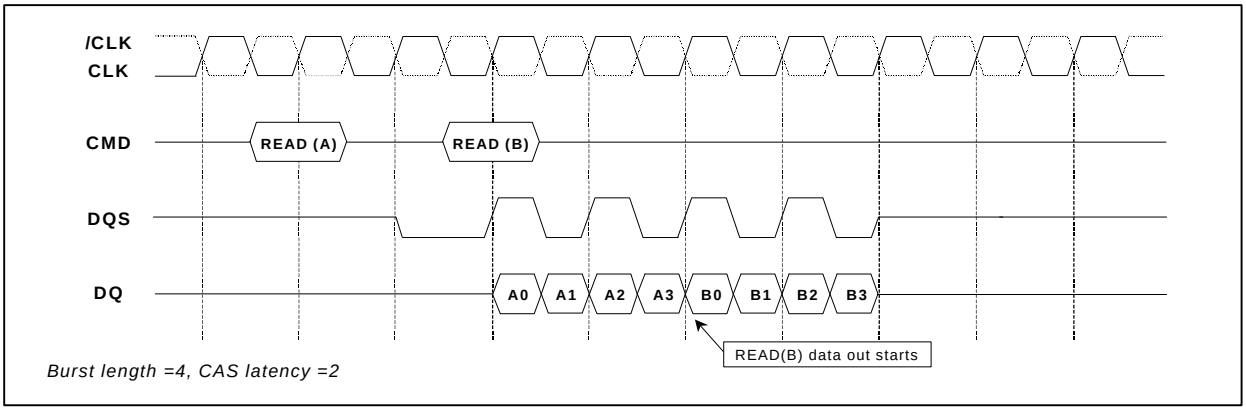
Fig.1. Burst Read and Burst Write



Burst Read followed by Burst Read

Back to back read operation in the same or different bank is possible as shown in Fig.2. Following first Read command, consecutive Read command can be initiated after BL/2 ticks of clock. In other words, minimum earliest possible Read command that does note interrupt the previous read data, can be issued after BL/2 clock is met. When Read(B) data out starts, data strobe signal does not transit to Hi-Z but toggle high and low for Read(B) data.

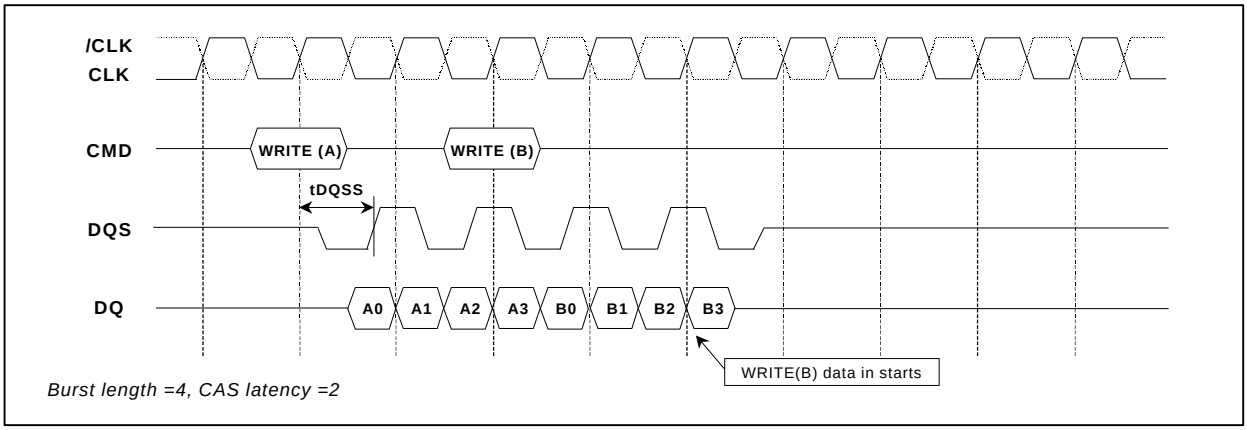
Fig.2. Burst Read followed by Burst Read



Burst Write followed by Burst Write

Back to back write operation in the same or different bank is possible as shown in Fig.3. Following first Write command, consecutive Write command can be initiated after BL/2 ticks of clock. In other words, minimum earliest possible Write command that does note interrupt the previous write data, can be issued after BL/2 clock is met. When Write(B) data in starts, data strobe signal does not transit to Hi-Z but toggle high and low for Write(B) data. Though the timing shown in Fig.3. is based on tDQSS=0.75*tCK, minimum number of clock of BL/2 for back to back write can be applied when tDQSS=1.25*tCK.

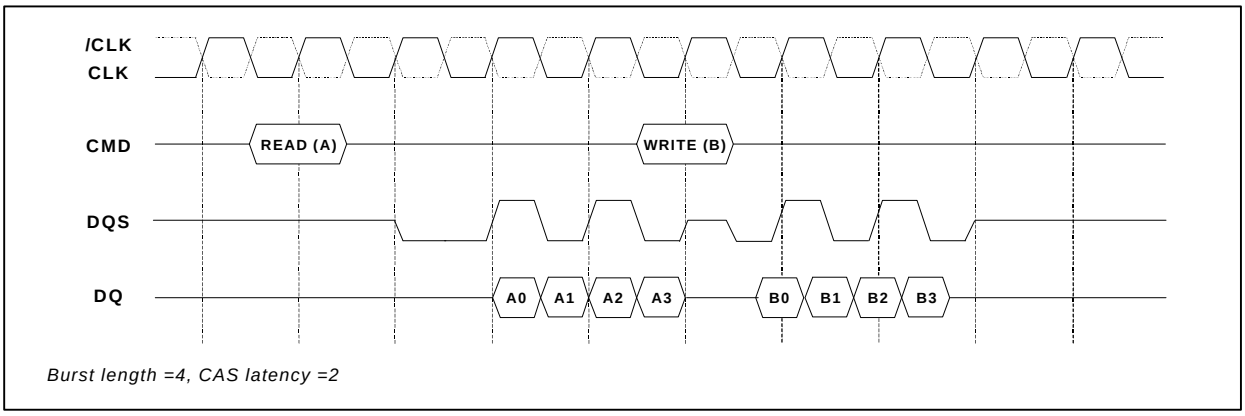
Fig.3. Burst Write followed by Burst Write



Burst Read followed by Burst Write

Back to back read followed by write operation in the same or different bank is possible as shown in Fig.4. Following first Read command, consecutive Write command can be initiated after RU{CL+BL/2} ticks of clock. (RU=Round Up for half cycle of CAS latency, such as 1.5 and 2.5). In other words, minimum earlist possible Write command that does not interrupt the previous read data can be issued after RU{CL+BL/2} clock is met.

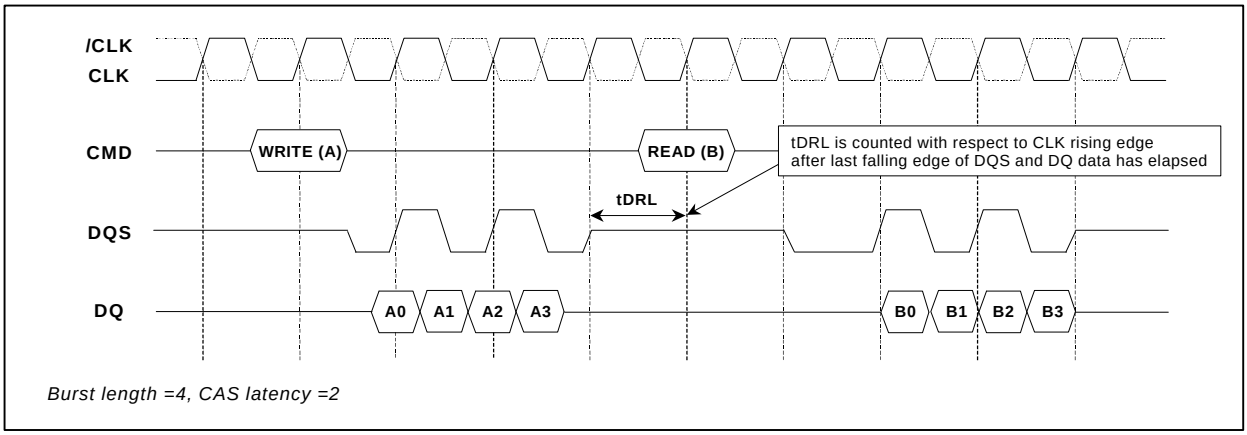
Fig.4. Burst Read followed by Burst Write



Burst Write followed by Burst Read

Back to back write followed by read operation in the same or different bank is possible as shown in Fig.5. Following first Write command, consecutive Read command can be initiated after (BL/2+1+tDRL) ticks of clock. In other words, minimum earlist possible Read command that does not interrupt the previous write data can be issued after (BL/2+1+tDRL) clock is met.

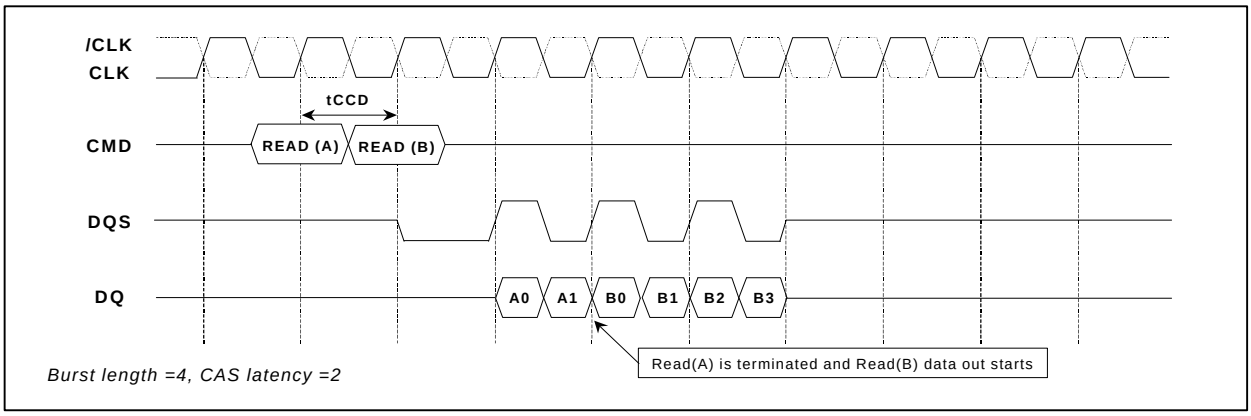
Fig.5. Burst Write followed by Burst Read



Burst Read terminated by another Burst Read

Read command terminates the previous Read command and the data is available after CAS latency for the new command. Minimum delay from a Read command to next Read command is determined by /CAS to /CAS delay (tCCD). Timing diagram is shown in Fig.6.

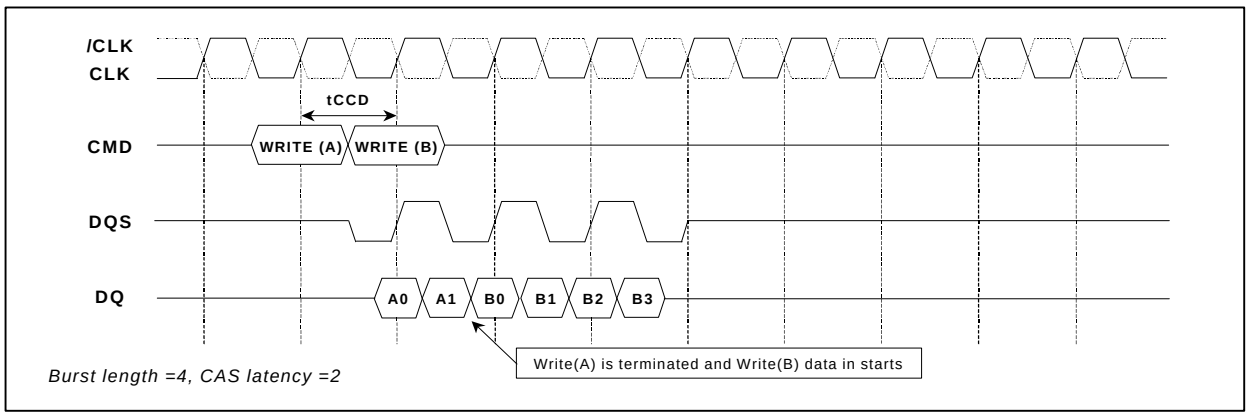
Fig.6. Burst Read terminated by another Burst Read



Burst Write terminated by another Burst Write

Write command terminates the previous Write command and the data is available after CAS latency for the new command. Fastest Write command to next Write command is determined by /CAS to /CAS delay (tCCD). Timing diagram is shown in Fig.7.

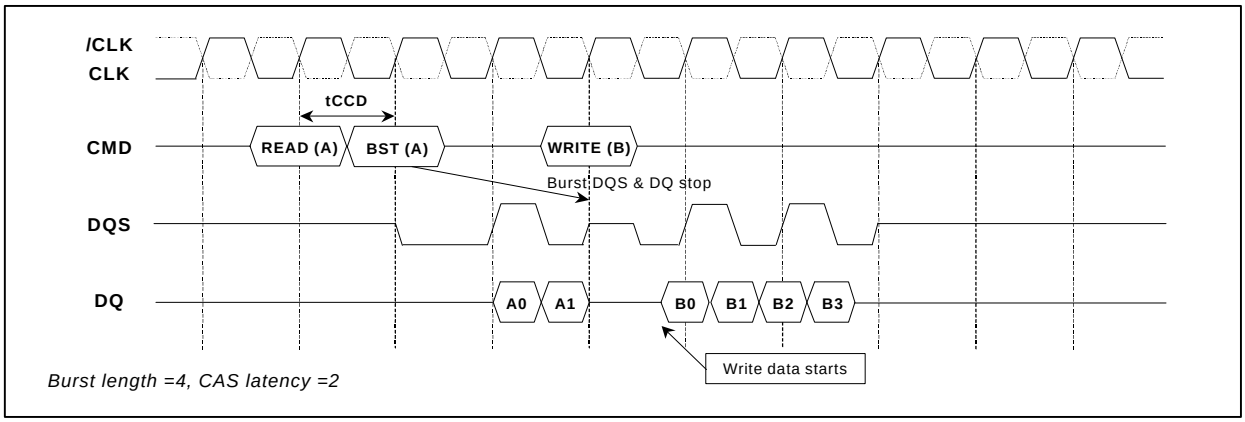
Fig.7. Burst Write terminated by another Burst Write



Burst Read terminated by another Burst Write

Write command terminates the previous Read command with the insertion of Burst Stop command that disables the previous Read command. The Burst Stop command interrupts bursting read data and data strobe signal with the same latency as CAS Latency (CL). The minimum delay for Write command after Burst Stop command is RU{CL} clocks irrespective BL. The Burst Stop command is valid for Read command only.

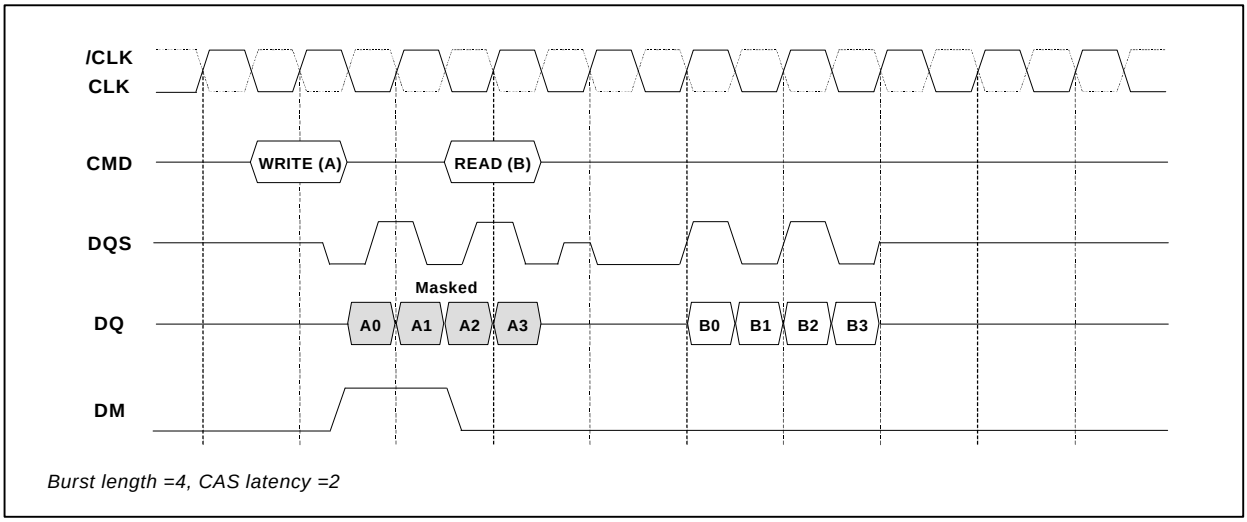
Fig.8. Burst Read terminated by another Burst Write



Burst Write terminated by another Burst Read

Read command terminates the previous Write command and the new burst read starts as shown in Fig.9. The minimum write to read command delay is 2 clock cycle irrespective of CL and BL. If input write data is masked by the Read command, DQ and DQS input are ignored by the DDR SDRAM. It is illegal for a Read command to interrupt a Write with autoprecharge command.

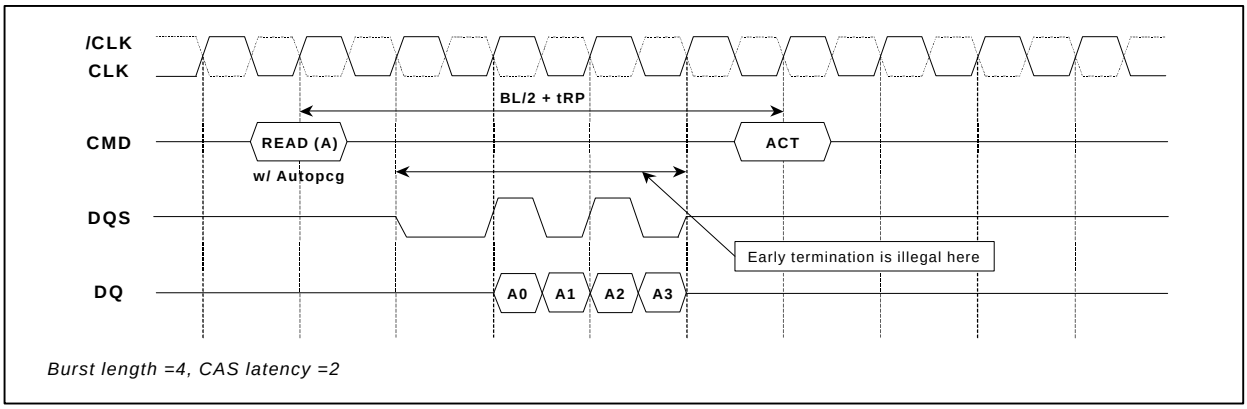
Fig.9. Burst Write terminated by another Burst Read



Burst Read with Autoprecharge

If a Read with Autoprecharge command is detected by memory component in CLK(n), then there will be no commands presented to this bank until CLK(n+BL/2+tRP). Internal precharging action will happen in CLK(n+BL/2).

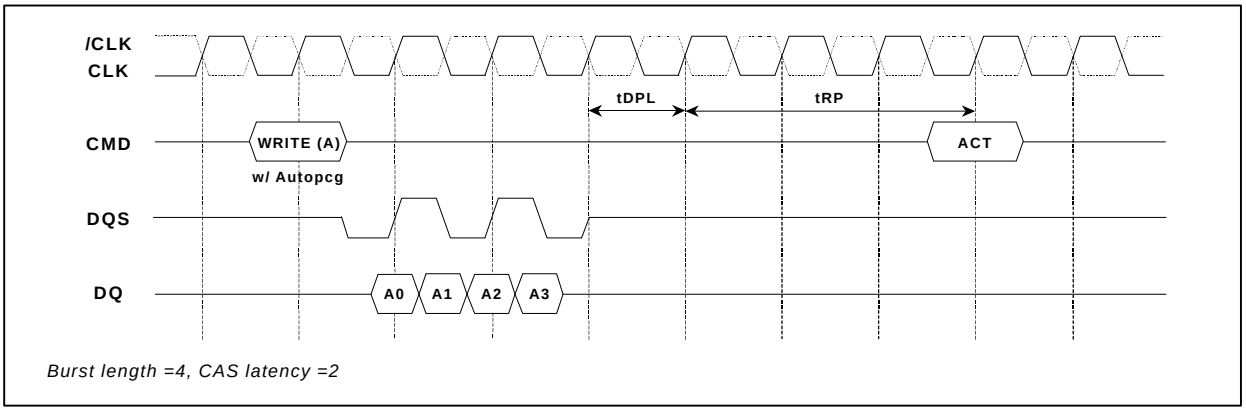
Fig.10. Burst Read with Autoprecharge



Burst Write with Autoprecharge

If a Write with Autoprecharge command is detected by memory component in CLK(n), then there will be no commands presented to this bank until CLK(n+BL/2+1+tDPL+tRP). Last Data in to Precharge delay time (tDPL) is needed to guarantee the last data has been written. tDPL is measured with respect to rising edge of clock where last falling edge of data strobe (DQS) and DQ data has elapsed. Internal precharging action will happen in CLK(n+BL/2+1+tDPL) as shown in Fig.11.

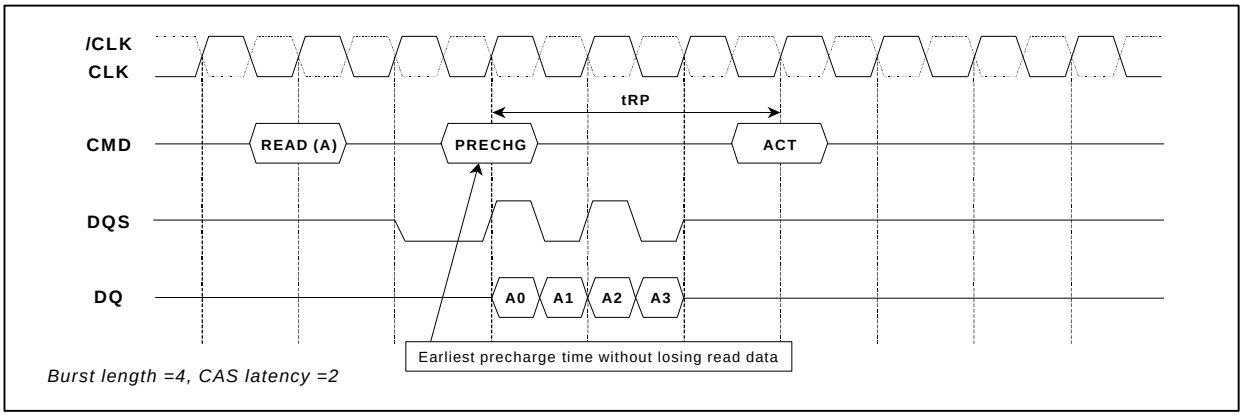
Fig.11. Burst Write with Autoprecharge



Precharge command after Burst Read

The earlist Precharge command can be issued after Read command without the loss of data is BL/2 clocks. The Precharge command can be given as soon as tRAS time is met. Fig.12 shows the earlist possible Precharge command can be issued for CL=2 and BL=4.

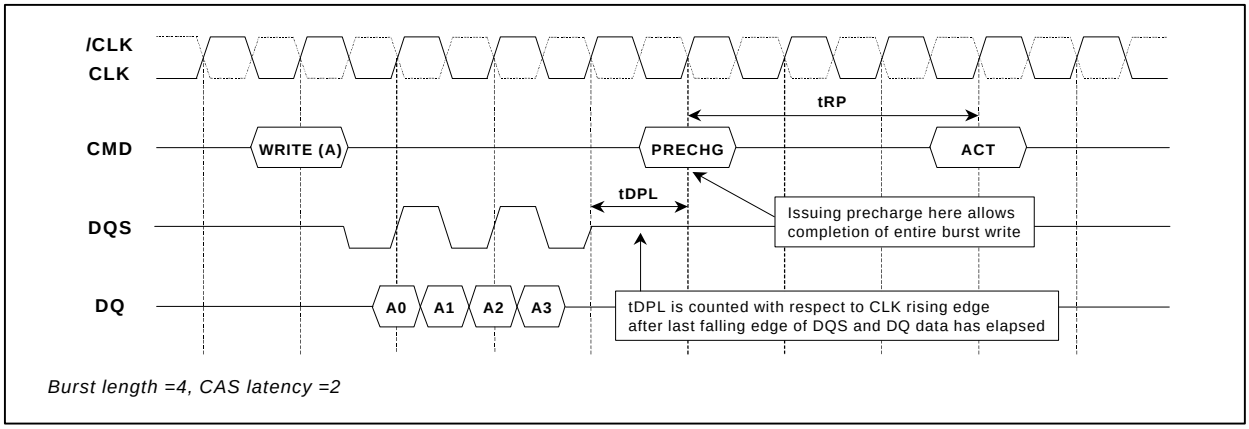
Fig.12. Precharge command after Burst Read



Precharge command after Burst Write

The earliest Precharge command can be issued after Write command without the loss of data is (BL/2+1+tDPL) ticks of clocks. The Precharge command can be given as soon as tRAS time is met. Fig.13 shows the earliest possible Precharge command can be issued for CL=2 and BL=4.

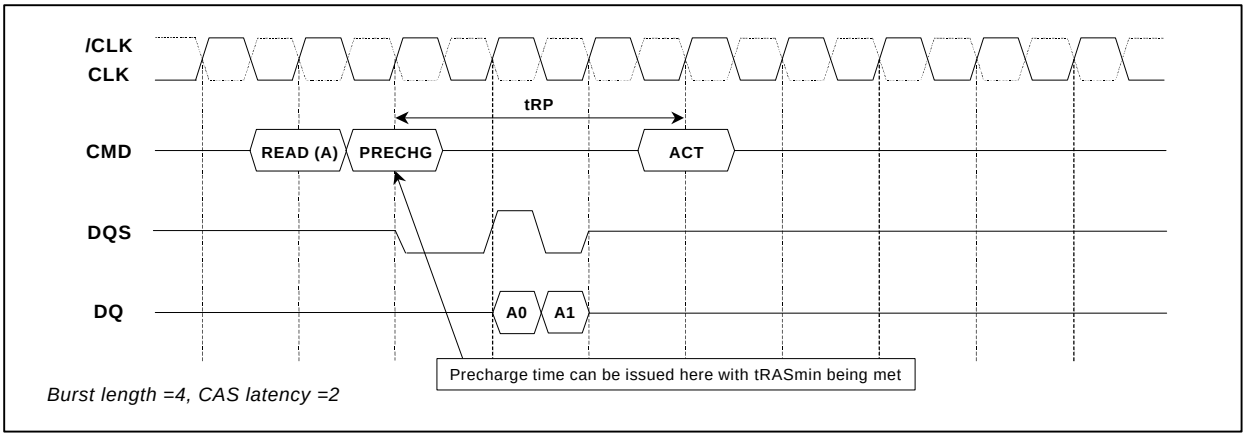
Fig.13. Precharge command after Burst Write



Precharge termination of Burst Read

The Burst Read (with no Autoprecharge) can be terminated earlier using a Precharge command as shown in Fig.14. This terminates read data when the remaining elements are not needed. It allows starting precharge early. The Precharge command can be issued any time after Burst Read command when tRAS time is met. Activation or other commands can be initiated after tRP time.

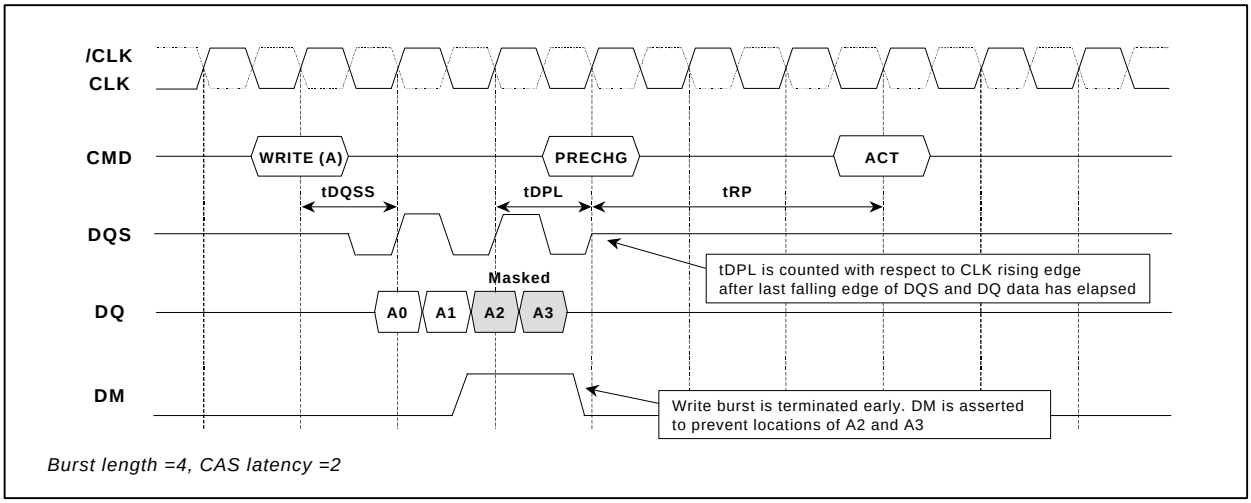
Fig.14. Precharge termination of Burst Read



Precharge termination of Burst Write

The Burst Write (with no Autoprecharge) can be terminated earlier using a Precharge command along with the Write Mask (DM) as shown in Fig.15. This terminates write data when the remaining elements are not needed. It allows starting precharge early. Precharge command can be issued after Last Data in to Precharge delay time (tDPL). tDPL is measured with respect to rising edge of clock where last falling edge of data strobe (DQS) and DQ data has elapsed. DM should be used to mask the remaining data (A2 and A3 for this case). tRAS time must be met to issue the Precharge command.

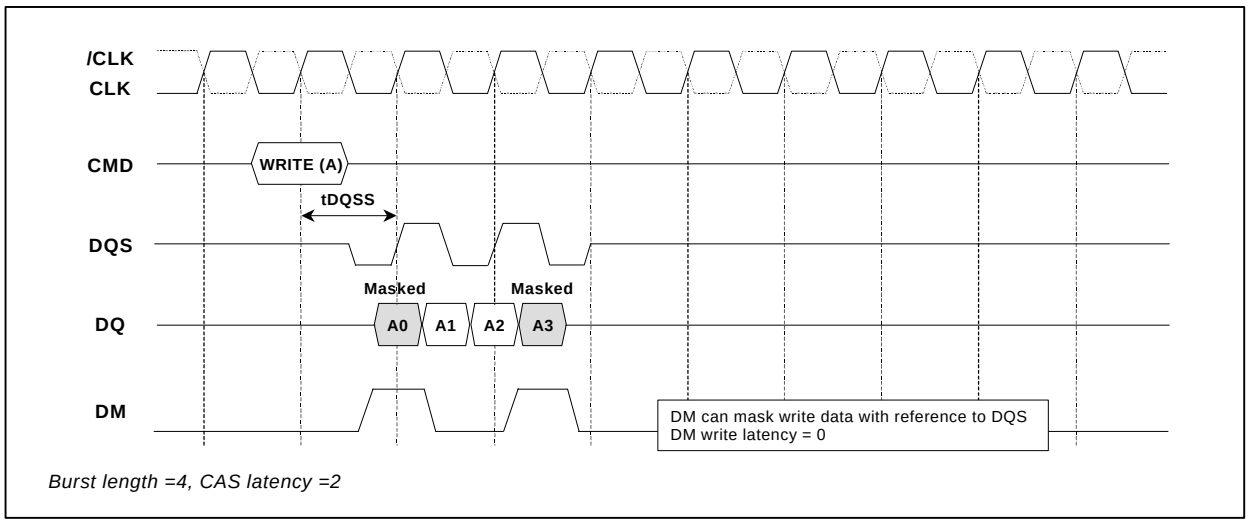
Fig.15. Precharge termination of Burst Write



DM masking (Write)

DM command masks burst write data with reference to data strobe signal and it is not related with read data. DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero. For x16 data I/O, DDR SDRAM is equipped with LDM and UDM which control lower byte (DQ0~DQ7) and upper byte (DQ8~DQ15) respectively.

Fig.16. DM masking (Write)

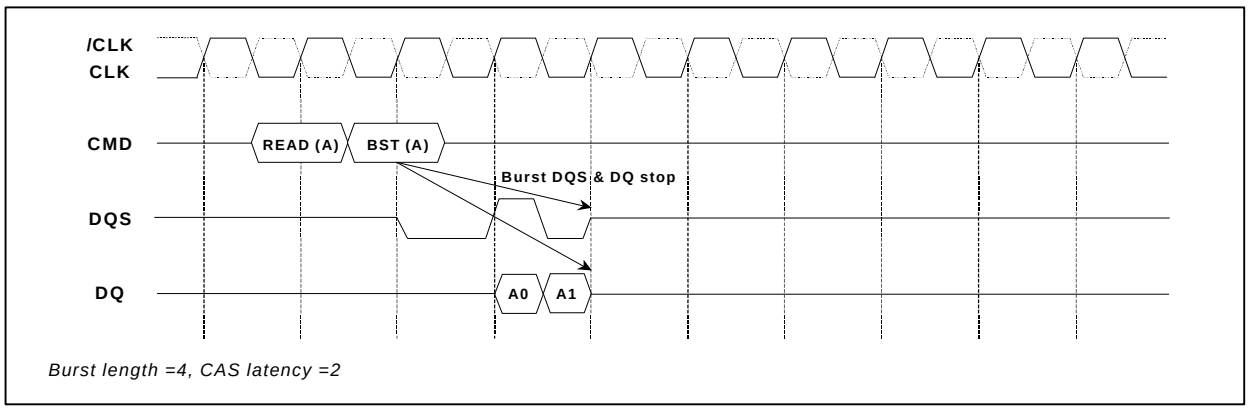


Burst length =4, CAS latency =2

Burst Stop command (Read)

When /CS=L, /RAS=H, /CAS=H and /WE=L, DDR SDRAM enter into Burst Stop mode, which bursts stop read data and data strobe signal with reference to clock signal. BST command can be initiated at the rising edge of the clock as other commands do. BST command is valid for read operation only. BST latency for read operation is the same as CL.

Fig.17. Burst Stop command (Read)

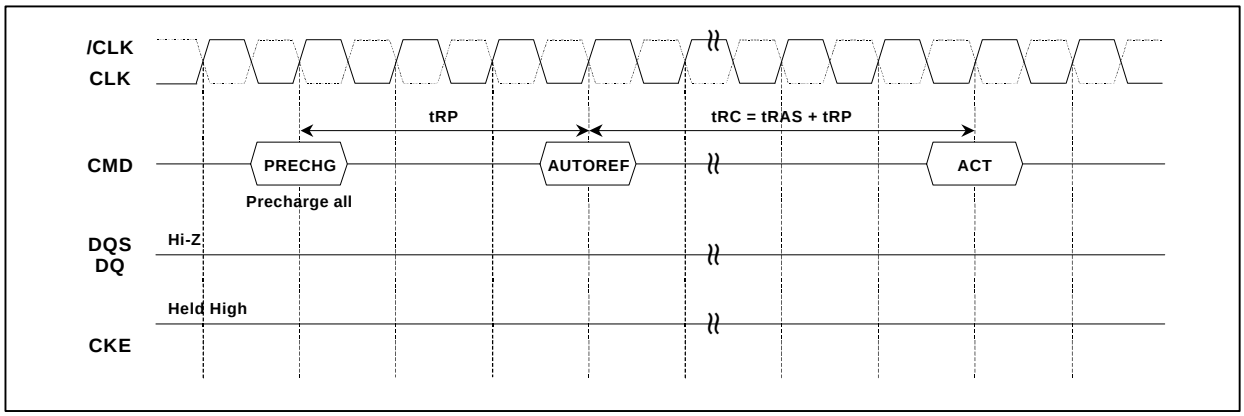


Burst length =4, CAS latency =2

Auto Refresh and Precharge All command

When /CS=L, /RAS=L, /CAS=L and /WE=H, DDR SDRAM enter into Auto Refresh mode, which executes refresh operation with internal address increment. AREF command can be initiated at the rising edge of the clock as other commands do. Before entering Auto Refresh mode, all banks must be in a precharge state and AREF command can be issued after tRP period from Precharge All command.

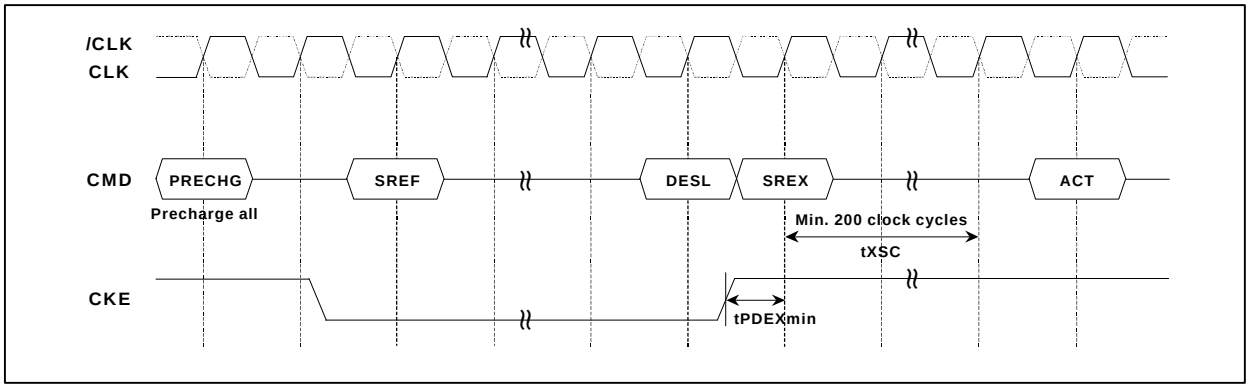
Fig.18. Auto Refresh and Precharge All command



Self Refresh Entry and Exit

When CKE=L, /CS=L, /RAS=L, /CAS=L and /WE=H, DDR SDRAM enter into Self Refresh mode, which executes self refresh operation with internal address increment. Before issuing Self Refresh command, all banks must be in a precharge state and CKE must be low. SREF command can be initiated at the rising edge of the clock as other commands do. Because the clock buffer and internal DLL circuit are disabled during self refresh state, Self Refresh Exit (SREX) should guarantee the stable input clock. Therefore, a minimum of 200 cycles of stable input clock, where CKE is held high, is required to lock the internal DLL circuit of DDR SDRAM. A minimum tPDEX (Power Down Exit Time) must be met before entering SREX command.

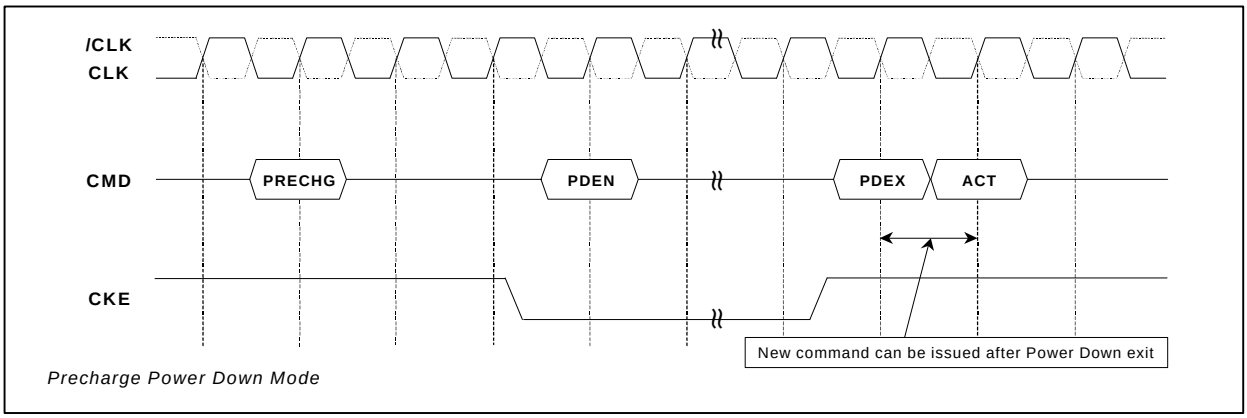
Fig.19. Self Refresh Entry and Exit



Power Down mode

A Power Down mode can be achieved by asserting CKE=L as shown in Fig.20. There are two kinds of Power Down mode: 1. Active and 2. Precharge Power Down mode. The device must be in idle state and all banks must be closed before CKE assertion in Precharge Power Down mode. Active Power Down mode can be initiated in row active state. The device will exit Power Down mode when CKE is sampled high at the rising edge of the clock.

Fig.20. Power Down mode

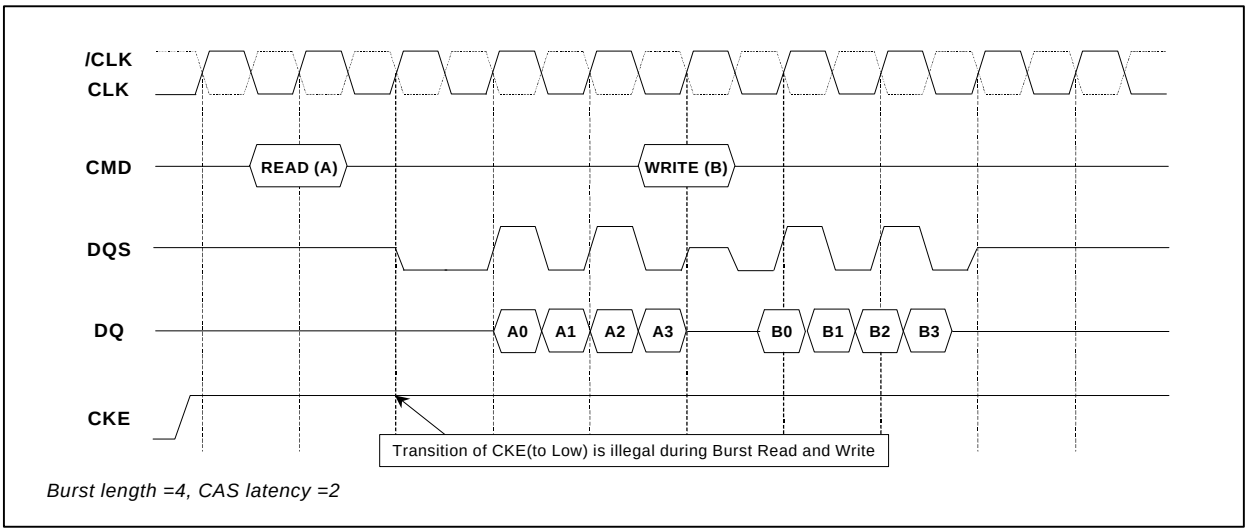


Precharge Power Down Mode

CKE function

Since clock suspend mode in SDR SDRAM cannot be used in DDR SDRAM, it is illegal to issue CKE=L during read or write burst.

Fig.21. CKE function



Burst length =4, CAS latency =2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.3	2.5	2.7	V	
Power Supply Voltage	VDDQ	2.3	2.5	2.7	V	1
Input High Voltage	VIH	VREF + 0.15	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.15	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V	3

Note :
1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak to peak noise on VREF may not exceed +/- 2% of the dc value.

DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-5	5	uA	1
Output Leakage Current	ILO	-5	5	uA	2
Output High Voltage	VOH	VTT + 0.76	-	V	IOH = -15.2mA
Output Low Voltage	VOL	-	VTT - 0.76	V	IOL = +15.2mA

Note : 1. VIN = 0 to 3.6V, All other pins are not tested under VIN =0V. 2. DOUT is disabled, VOUT=0 to 2.7V

DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

32Mx4

Parameter	Symbol	Test Condition		Speed		Unit	Note
				-H	-L		
Operating Current	IDD0	One ban; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle		TBD	TBD		
Operating Current	IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle		130	120	mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)		20		mA	
Idle Standby Current	IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN = VREF for DQ, DQS and DM		40		mA	
Active Power Down Standby Current	IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)		25		mA	
Active Standby Current	IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		50		mA	
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA		TBD	TBD	mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle		TBD	TBD		
Auto Refresh Current	IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh		310			
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK=tCK(min)	Normal	2		mA	
			Low Power	1		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition		TBD	TBD	mA	

DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

16Mx8

Parameter	Symbol	Test Condition	Speed		Unit	Note
			-H	-L		
Operating Current	IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	mA	
Operating Current	IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	140	130	mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	20		mA	
Idle Standby Current	IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN = VREF for DQ, DQS and DM	40		mA	
Active Power Down Standby Current	IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	25		mA	
Active Standby Current	IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	50		mA	
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	TBD	TBD	mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	TBD	TBD		
Auto Refresh Current	IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & PC266B at 133Mhz; distributed refresh	320			
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK=tCK(min) — Normal	2		mA	
		CKE =< 0.2V; External clock on; tCK=tCK(min) — Low Power	1		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition	TBD	TBD	mA	

DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

8Mx16

Parameter	Symbol	Test Condition	Speed		Unit	Note
			-H	-L		
Operating Current	IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	mA	
Operating Current	IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	150	140	mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	20		mA	
Idle Standby Current	IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	40		mA	
Active Power Down Standby Current	IDD3P	One bank active; Power down mode; CKE= Low, tCK=tCK(min)	25		mA	
Active Standby Current	IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC= tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	50		mA	
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	TBD	TBD	mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	TBD	TBD		
Auto Refresh Current	IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	330			
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK=tCK(min) — Normal	2			
		CKE =< 0.2V; External clock on; tCK=tCK(min) — Low Power	1		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition	TBD	TBD	mA	

DETAILED TEST CONDITIONS FOR DDR SDRAM IDD1 & IDD7

IDD1 : Operating current: One bank operation

1. Typical Case : VDD = 2.5V, T=25 °C

2. Worst Case : VDD = 2.7V, T= 10 °C

3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA

4. Timing patterns

   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changingt

     50% of data changing at every burst

   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst

   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD7 : Operating current: Four bank operation

1. Typical Case : VDD = 2.5V, T=25 °C

2. Worst Case : VDD = 2.7V, T= 10 °C

3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA

4. Timing patterns

   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :
1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-H(DDR266B)		-L(DDR200)		Unit	Note
			Min	Max	Min	Max		
Row Cycle Time		tRC	65	-	70	-	ns	
Auto Refresh Row Cycle Time		tRFC	75	-	80	-	ns	
Row Active Time		tRAS	45	120K	50	120K	ns	
Active to Read with Auto Precharge Delay		tRAP	tRAS-(BL/2)xtCK	-	tRAS-(BL/2)xtCK	-	ns	16
Row Address to Column Address Delay		tRCD	20	-	20	-	ns	
Row Active to Row Active Delay		tRRD	15	-	15	-	ns	
Column Address to Column Address Delay		tCCD	1	-	1	-	CK	
Row Precharge Time		tRP	20	-	20	-	ns	
Last Data-In to Precharge Delay Time (Write Recovery Time)		tDPL	15	-	20	-	ns	
Last Data-In to Read Command		tDRL	1	-	1	-	CK	
Auto Precharge Write Recovery + Precharge Time		tDAL	5	-	4	-	CK	15
System Clock Cycle Time	CL = 2.5	tCK	7.5	15	10	15	ns	
	CL = 2		10	15	10	15	ns	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	CK	
Data-Out edge to Clock edge Skew		tAC	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Clock edge Skew		tDQSCK	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Data-Out edge Skew		tDQSQ	-	0.5	-	0.6	ns	
Data-Out hold time from DQS		tQH	tHPmin -tQHS	-	tHPmin -tQHS	-	ns	1, 10
Clock Half Period		tHP	tCH/L min	-	tCH/L min	-	ns	1,9
Data Hold Skew Factor		tQHS	-	0.75	-	1	ns	10
Valid Data Output Window		tDV	tQH-tDQSQ		tQH-tDQSQ		ns	
Data-out high-impedance window from CK, /CK		tHZ			-1.2	0.8	ns	
Data-out low-impedance window from CK, /CK		tLZ			-1.2	0.8	ns	
Input Setup Time (fast slew rate)		tIS	0.9	-	1.2	-	ns	2,3,5,6
Input Hold Time (fast slew rate)		tIH	0.9	-	1.2	-	ns	2,3,5,6

Parameter	Symbol	-H(DDR266B)		-L(DDR200)		Unit	Note
		Min	Max	Min	Max		
Input Setup Time (slow slew rate)	tIS	1.0	-	1.2	-	ns	2,4,5, 6
Input Hold Time (slow slew rate)	tIH	1.0	-	1.2	-	ns	2,4,5, 6
Input Pulse Width	tIPW	2.2		-		ns	6
Write DQS High Level Width	tDQSH	0.35	-	0.35	-	CK	
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	CK	
Clock to First Rising edge of DQS-In	tDQSS	0.75	1.25	0.75	1.25	CK	
Data-In Setup Time to DQS-In (DQ & DM)	tDS	0.5	-	0.6	-	ns	6,7, 11~13
Data-in Hold Time to DQS-In (DQ & DM)	tDH	0.5	-	0.6	-	ns	6,7, 11~13
DQ & DM Input Pulse Width	tDIPW	1.75	-	2	-	ns	
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	CK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	CK	
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	CK	
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	CK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	CK	
Mode Register Set Delay	tMRD	2	-	2	-	CK	
Exit Self Refresh to Any Execute Command	tXSC	200	-	200	-	CK	8
Average Periodic Refresh Interval	tREFI	-	15.6	-	15.6	us	

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
   This derating table is used to increase tIS/tIH in case where the input slew-rate is below 0.5V/ns.
   Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tIS	Delta tIH
V/ns	ps	ps
0.5	0	0
0.4	+50	0
0.3	+100	0

5. CK, /CK slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.

7. Data latched at both rising and falling edges of Data Strobes(LDQS/UDQS) : DQ, LDM/UDM.
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
9. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
10. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects and p-channel to n-channel variation of the output drivers.
11. This derating table is used to increase tDS/tDH in case where the input slew-rate is below 0.5V/ns.
Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tDS	Delta tDH
V/ns	ps	ps
0.5	0	0
0.4	+75	+75
0.3	+150	+150

12. I/O Setup/Hold Plateau Derating. This derating table is used to increase tDS/tDH in case where the input level is flat below VREF +/-310mV for a duration of up to 2ns.

I/O Input Level	Delta tDS	Delta tDH
mV	ps	ps
+280	+50	+50

13. I/O Setup/Hold Delta Inverse Slew Rate Derating. This derating table is used to increase tDS/tDH in case where the DQ and DQS slew rates differ. The Delta Inverse Slew Rate is calculated as (1/SlewRate1)-(1/SlewRate2). For example, if slew rate 1 = 0.5V/ns and Slew Rate2 = 0.4V/n then the Delta Inverse Slew Rate = -0.5ns/V.

(1/SlewRate1)-(1/SlewRate2)	Delta tDS	Delta tDH
ns/V	ps	ps
0	0	0
+/-0.25	+50	+50
+/- 0.5	+100	+100

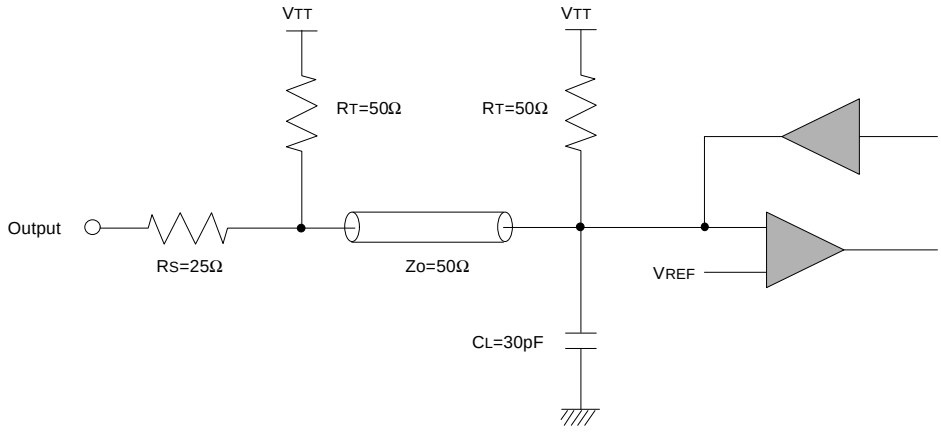
14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
15. tDAL = (tDPL / tCK) + (tRP / tCK). For each of the terms above, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
Example: For DDR266B at CL=2.5 and tCK = 7.5 ns,
tDAL = (15 ns / 7.5 ns) + (20 ns / 7.5 ns) = (2.00) + (2.67)
Round up each non-integer to the next highest integer: = (2) + (3), tDAL = 5 clocks
16. For the parts which do not has internal RAS lockout circuit, Active to Read with Auto precharge delay should be tRAS - BL/2 x tCK.

CAPACITANCE (T_A=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Clock Capacitance	CK, /CK	C_{I1}	2.0	3.0	pF
Delta Input Clock Capacitance	CK, /CK	Delta C_{I1}	-	0.25	pF
Input Capacitance	All other input-only pins	C_{I1}	2.0	3.0	pF
Delta Input Capacitance	All other input-only pins	Delta C_{I2}	-	0.5	pF
Input / Output Capacitance	DQ, DQS, DM	C_{IO}	4.0	5.0	pF
Delta Input / Output Capacitance	DQ, DQS, DM	Delta C_{IO}	-	0.5	pF

Note :
1. VDD = min. to max., VDDQ = 2.3V to 2.7V, V_{ODC} = VDDQ/2, $V_{Opeak-to-peak}$ = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



OUTPUT DRIVE CHARACTERISTICS (FULL STRENGTH DRIVER)

Voltage	Pull Down Current (mA)				Pull Up Current (mA)			
	Nominal Low	Nominal High	Minimum	Maximum	Nominal Low	Nominal High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.8	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Evaluation conditions:

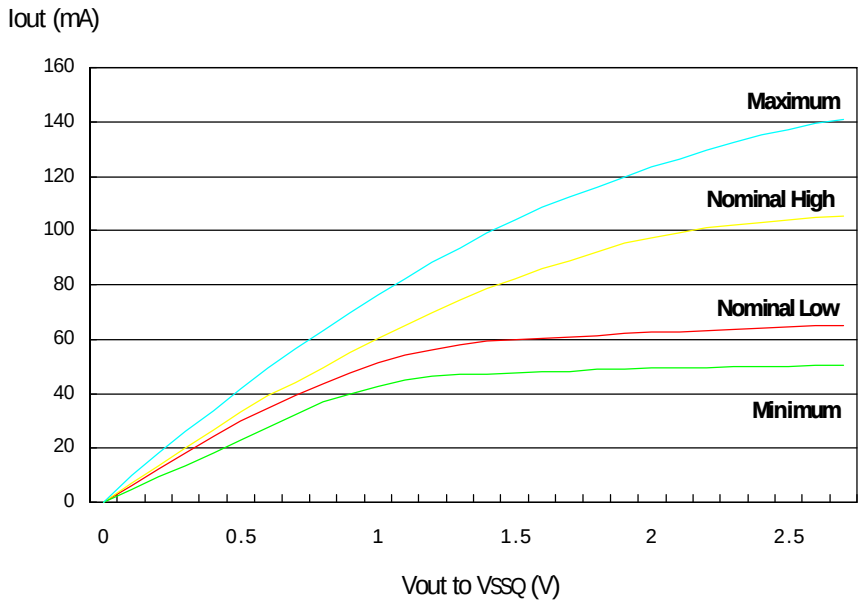
Typical 25 ºC (TAmbient), VDDQ=2.5V, typical process

Minimum 70 ºC (TAmbient), VDDQ=2.3V, slow slow process

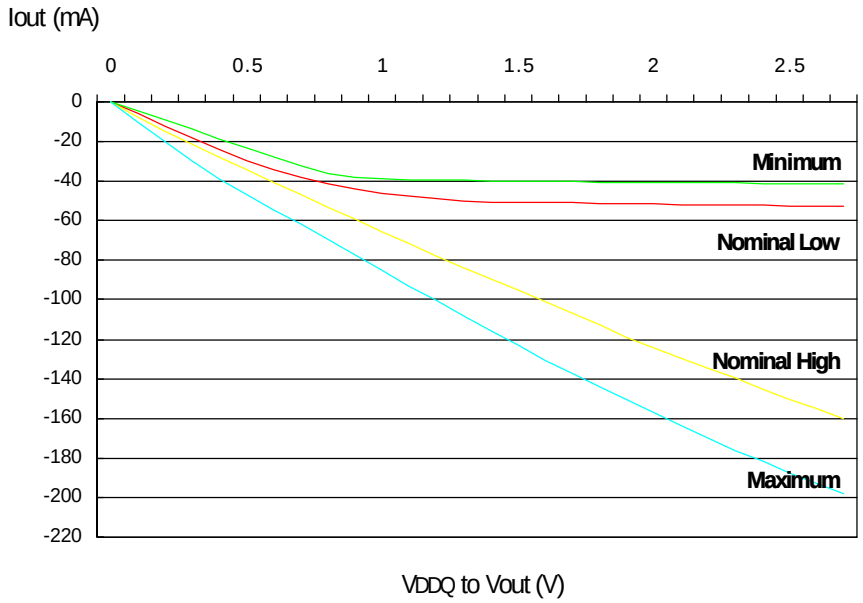
Maximum 0 ºC (TAmbient), VDDQ=2.7V, fast fast process

OUTPUT DRIVE CHARACTERISTICS (FULL STRENGTH DRIVER)

Pull Down Characteristics

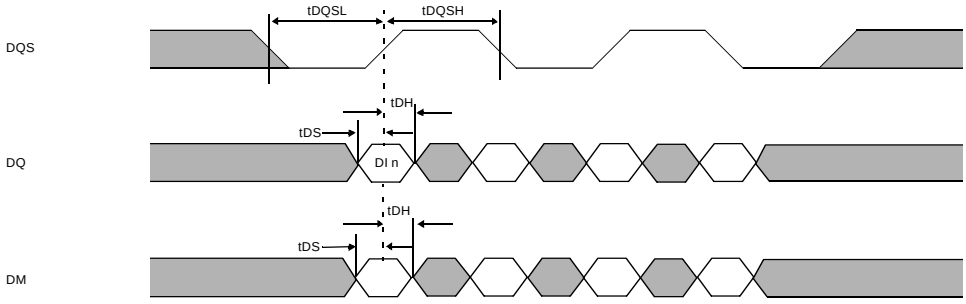


Pull Up Characteristics



Timing Diagram

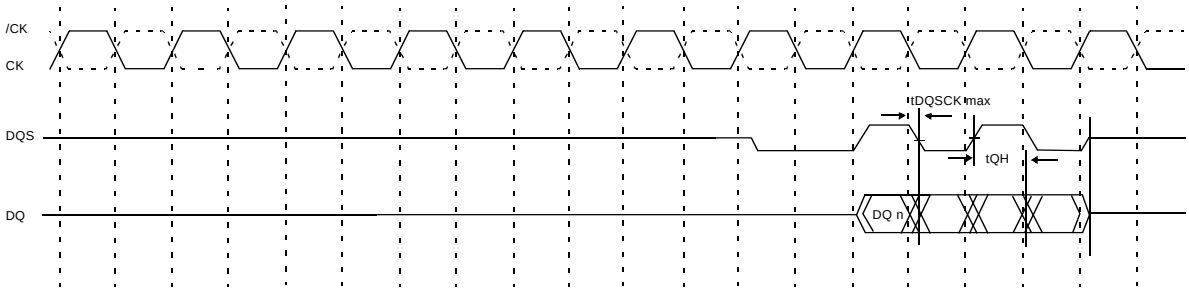
Data Input (Write) Timing (BL=4)



DI n = Data in for column n
3 subsequent elements of data in are applied in the programmed order following DI n

Don't care

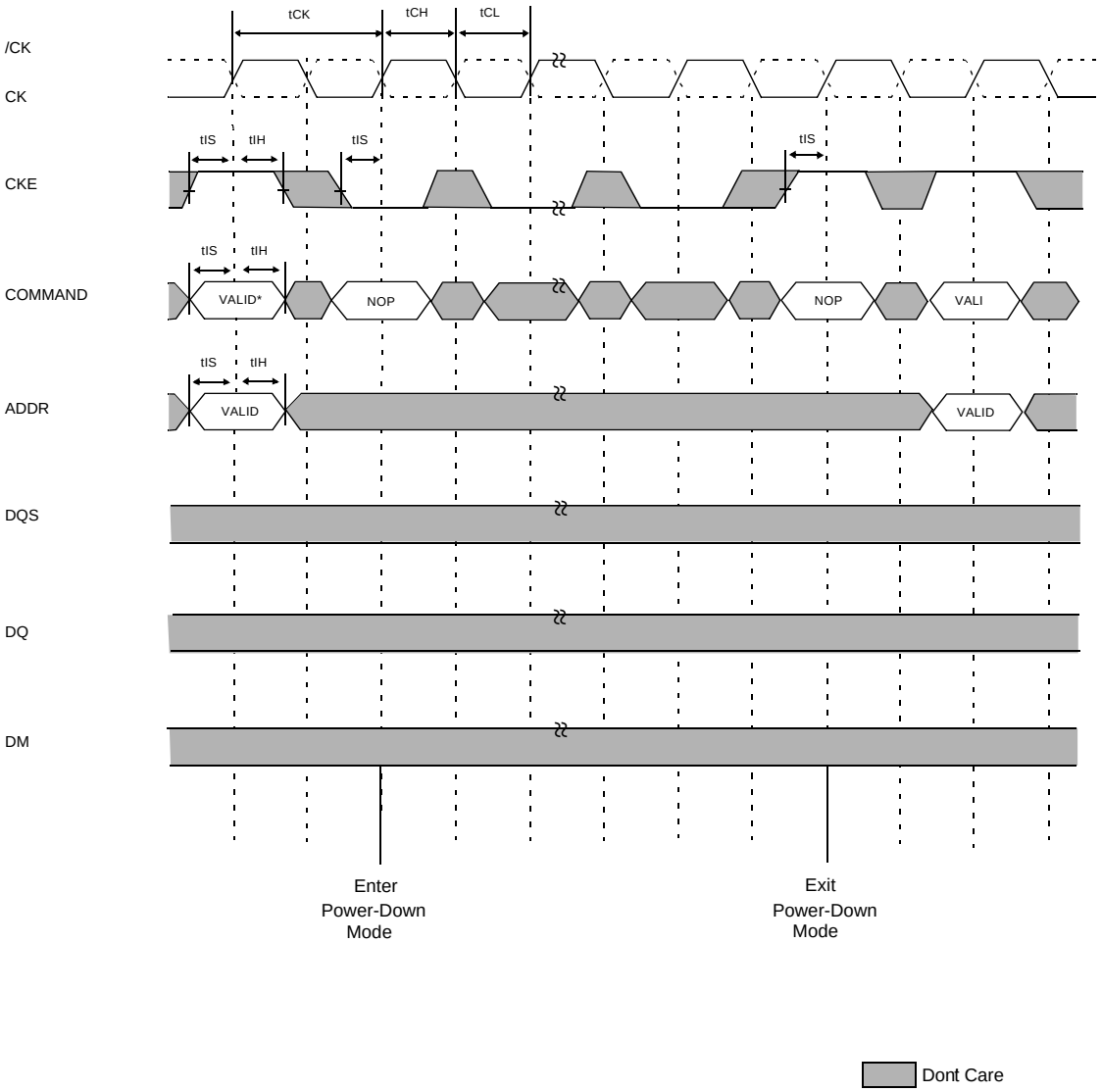
Data Output (Read) Timing (BL=4)



tDQSQ and tQH are only shown once, and are shown referenced to different edges of DQS, only for clarify of illustration.
tDQSQ and tQH both apply to each of the four relevant edges of DQS.

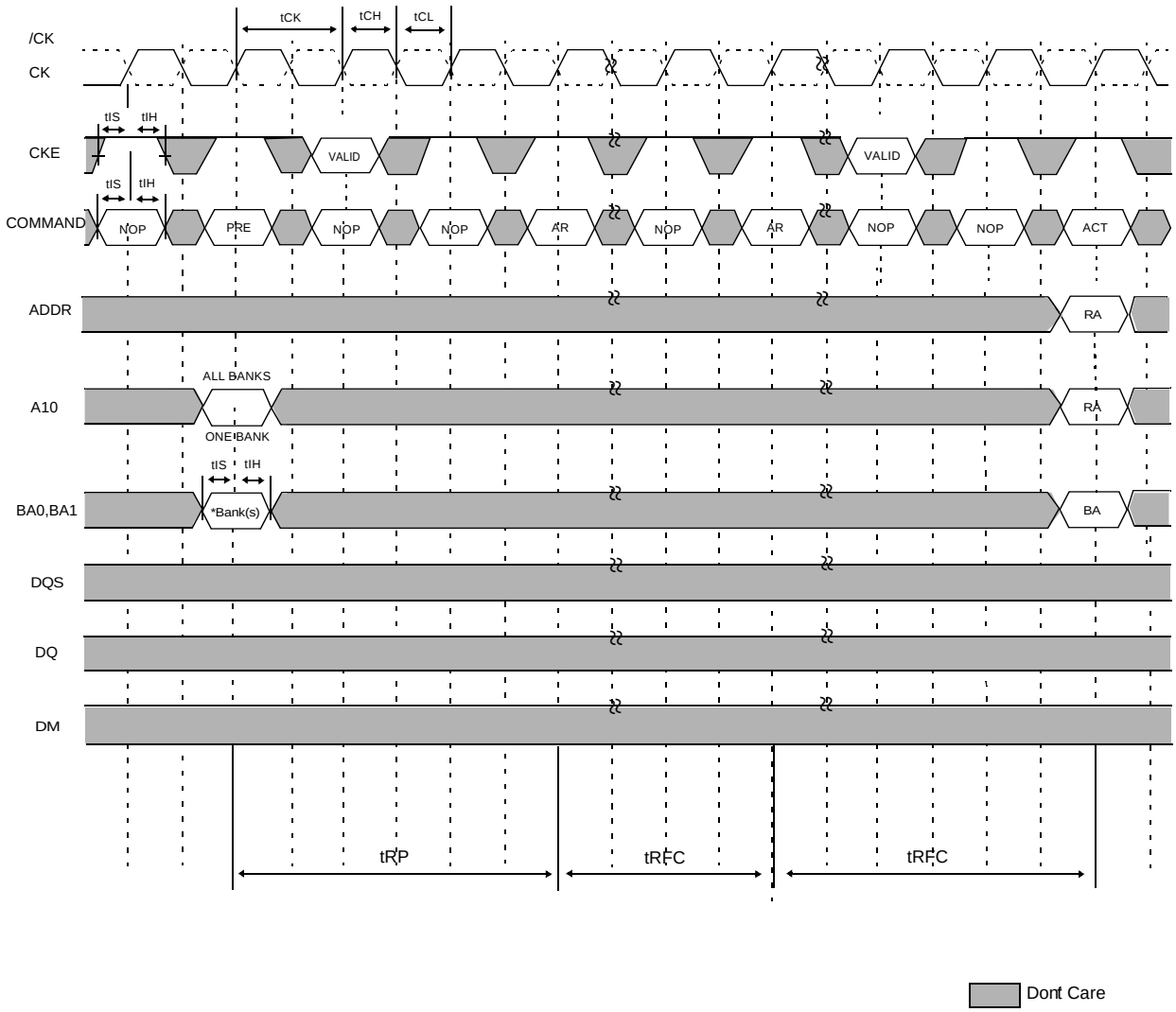
tQHmin = tHPmin - X where ;
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL)
X consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

Power Down Mode



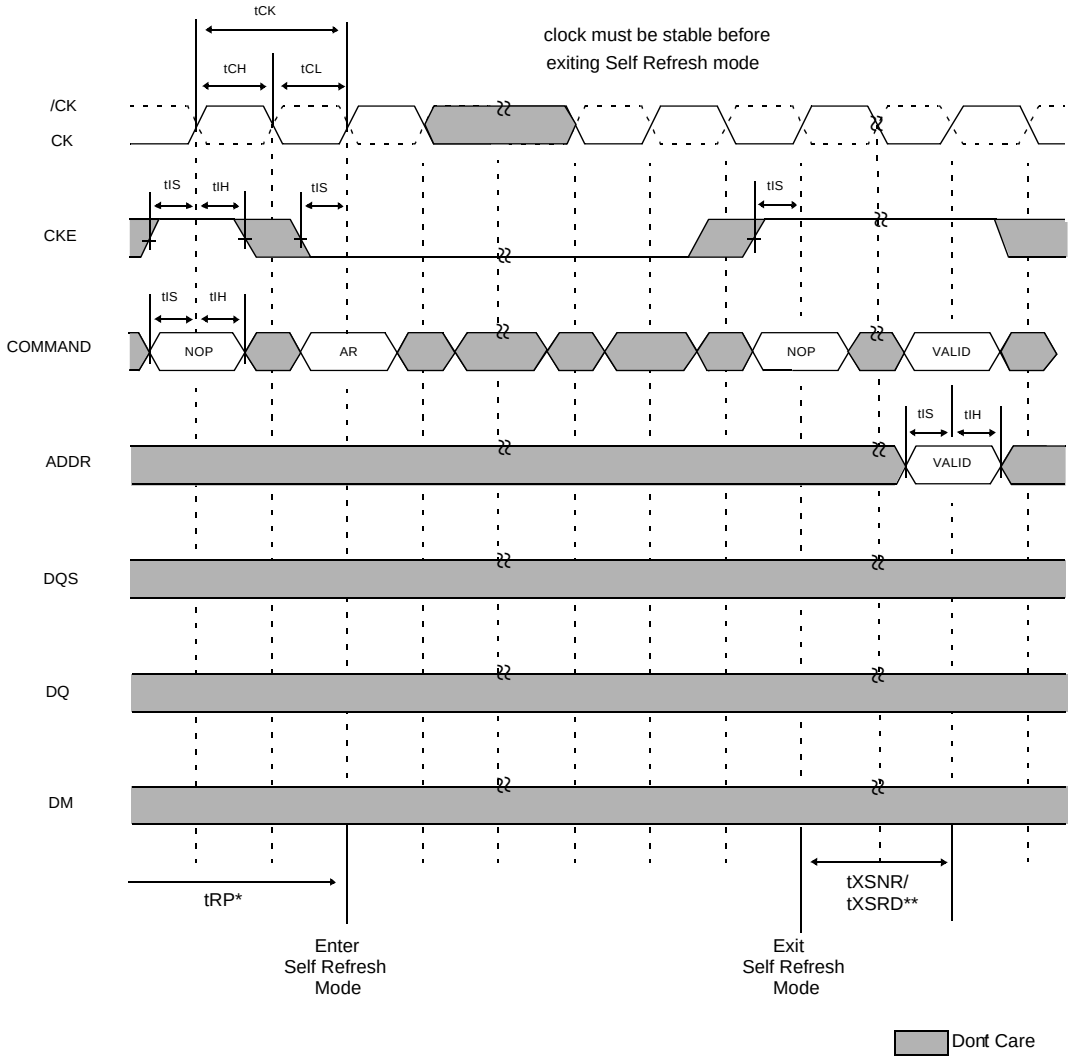
No column accesses are allowed to be in progress at the time Power-Down is entered.
* = If this command is a PRECHARGE (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is Active Power Down.

Auto Refresh Mode



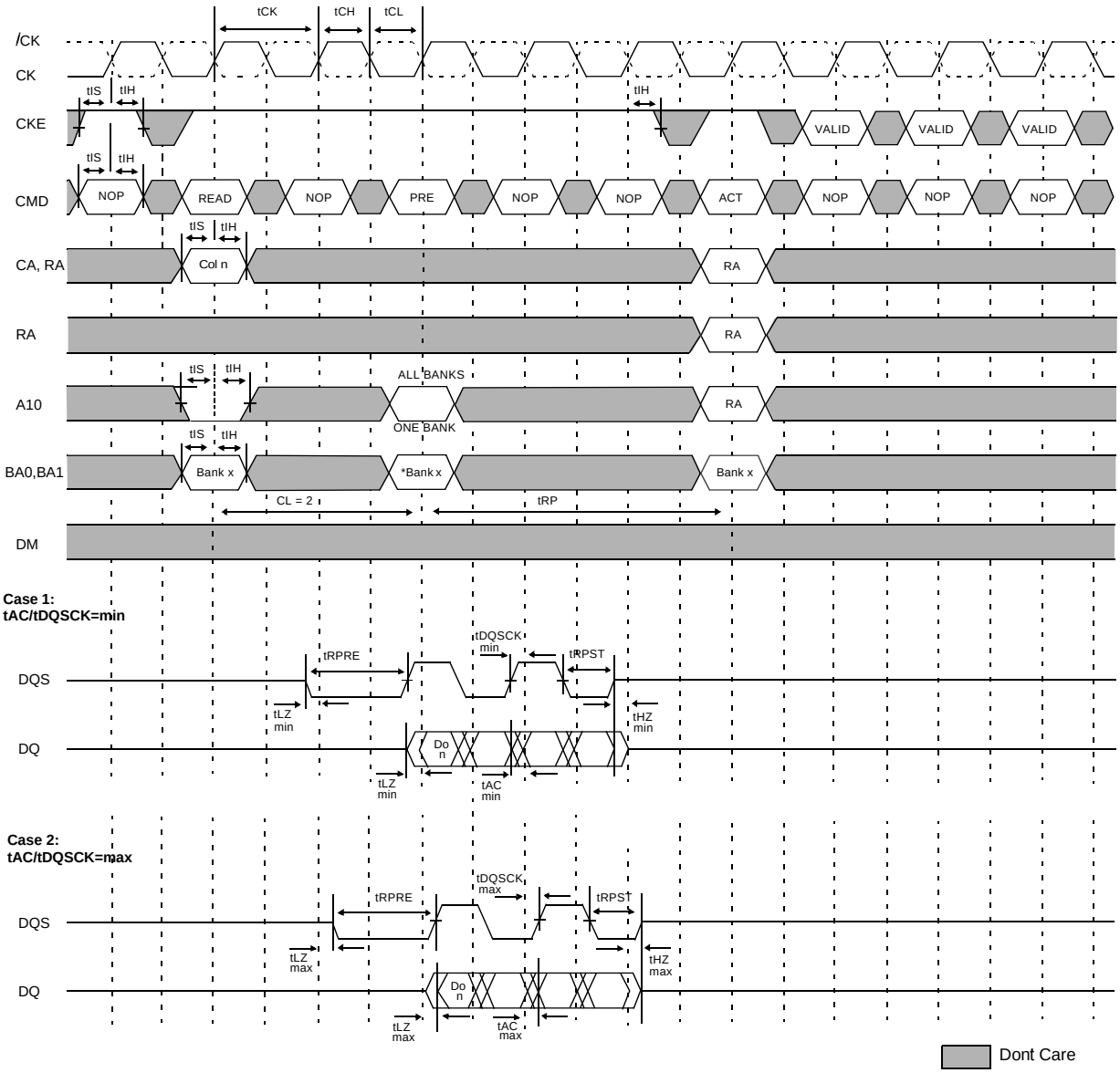
* = "Dont Care", if A10 is High at this point ; A10 must be High if more than one bank is active (i.e., must precharge all a ctive banks)
PRE = Precharge, ACT = Active, RA = Row Address, BA = Bank Address, AR = Autorefresh.
NOP commands are shown for ease of illustration ; other valid commands may be possible at these times.
DM, DQ and DQS signals are all "Dont Care" / High-Z for operation shown.

Self Refresh Mode



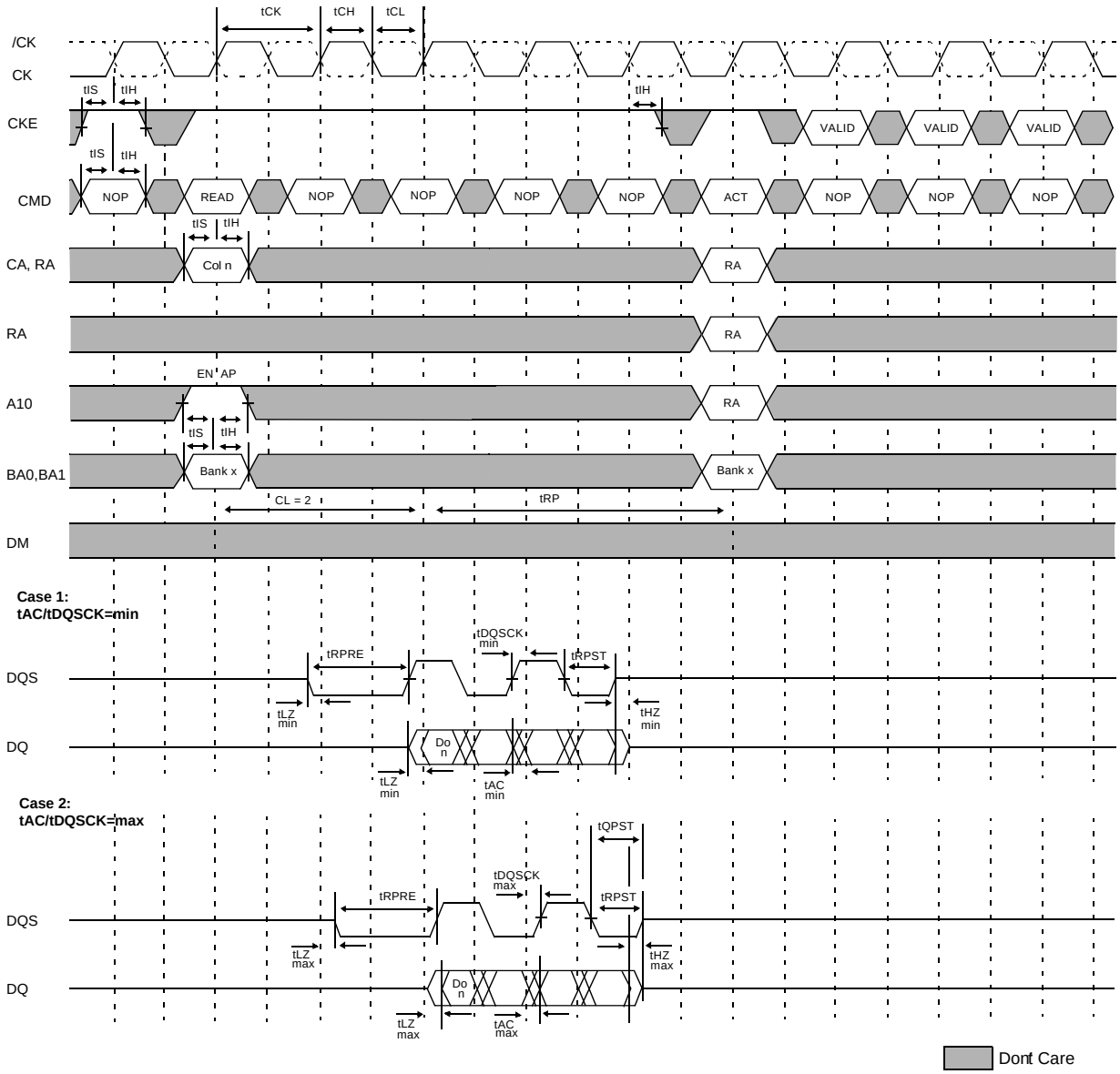
* = Device must be in the "All banks idle" state prior to entering Self Refresh mode
** = tXSNR is required before any non-READ command can be applied, and tXSRD (200 cycles of CK) are required before a READ command can be applied.

Read Without Auto Precharge



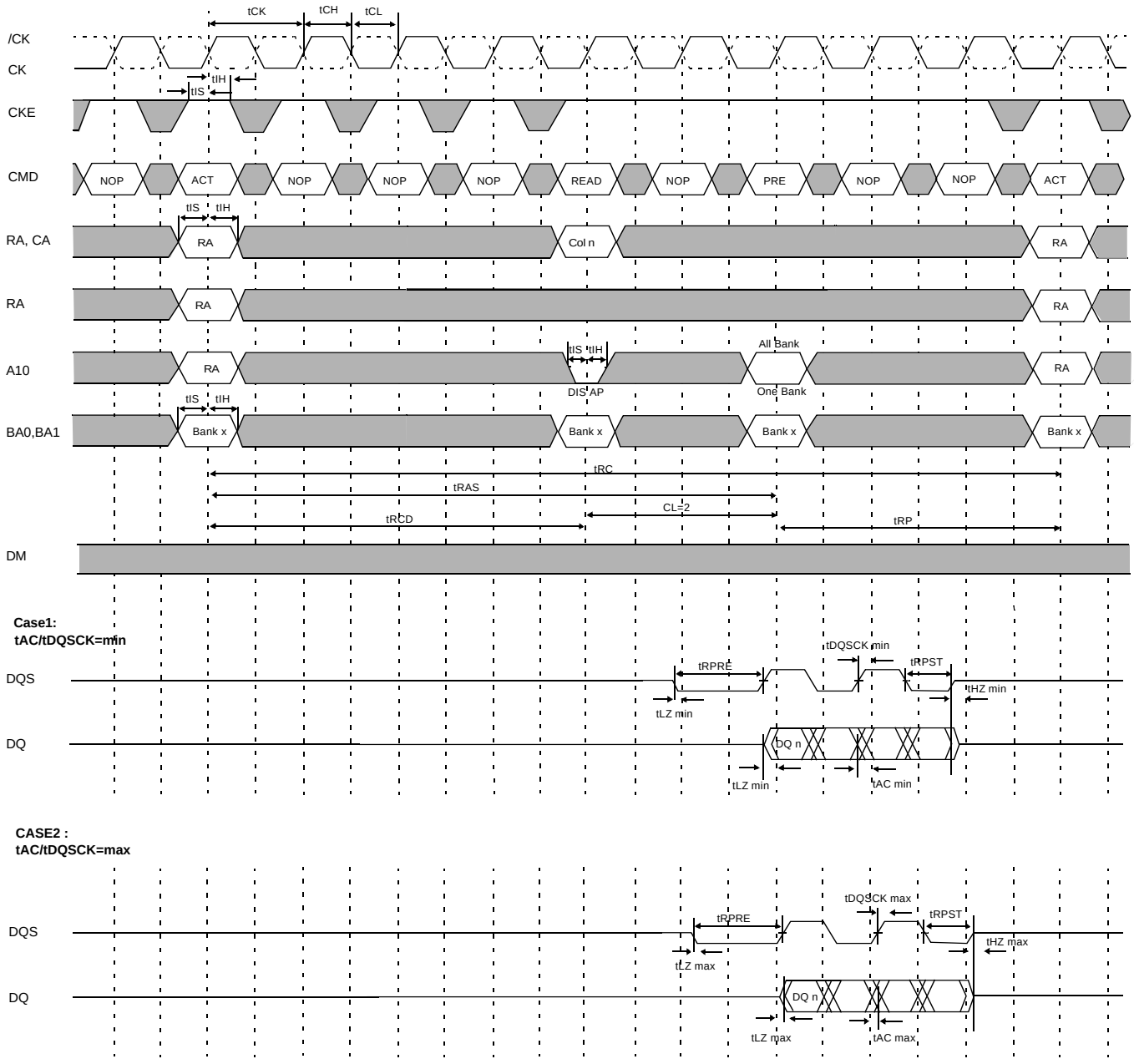
DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = "Dont Care", if A 10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration ; other commands may be valid at these times

Read With Auto Precharge



DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
EN AP = Enable Autoprecharge, ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration ; other commands may be valid at these times

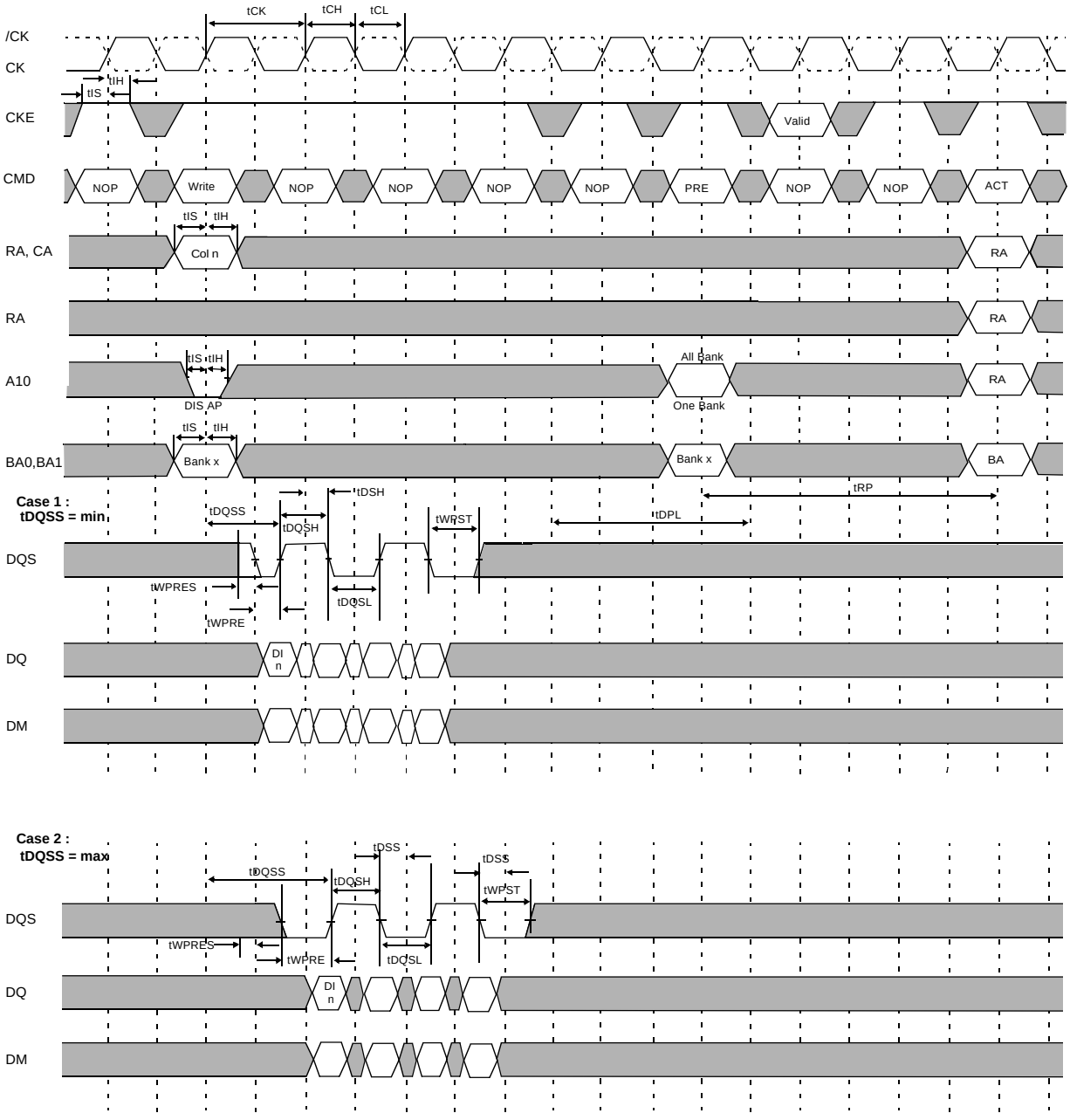
Bank Read Access



DQ n = Data out from column n
Burst length = 4 in the case shown
3 subsequent elements of Data out are provided in the programmed order following DQ n
DIS AP = Disable Autoprecharge
* = * "Dont Care", if A10 is high at this point
PRE = Precharge, ACT=Active, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD min so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Dont care

Write Without Auto Precharge

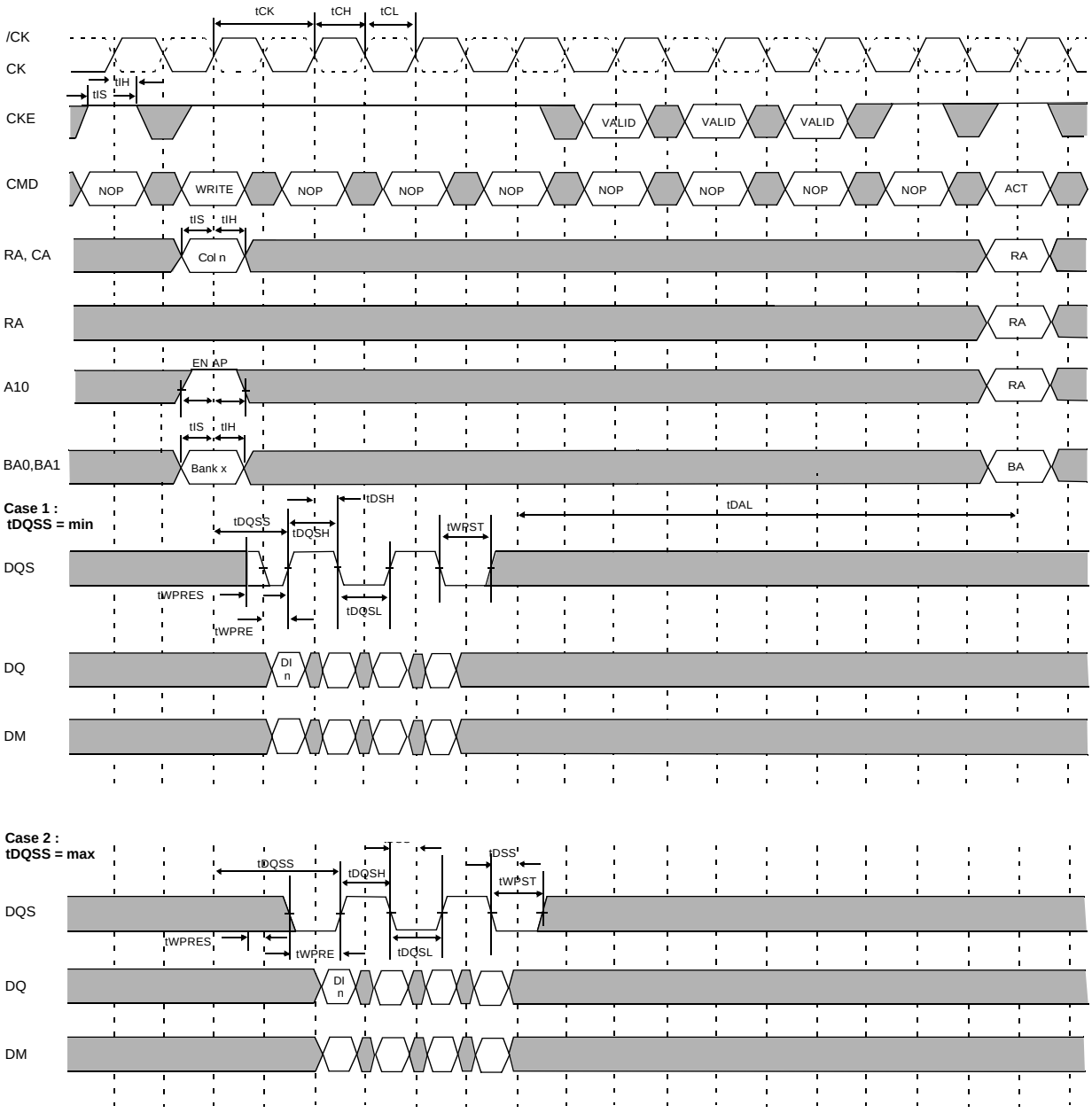


DI n = Data in for column n
Burst length = 4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = * "Dont Care", if A10 is high at this point
PRE = Precharge, ACT=Active, RA=Row Address, BA=Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Dont care

Write With Auto Precharge

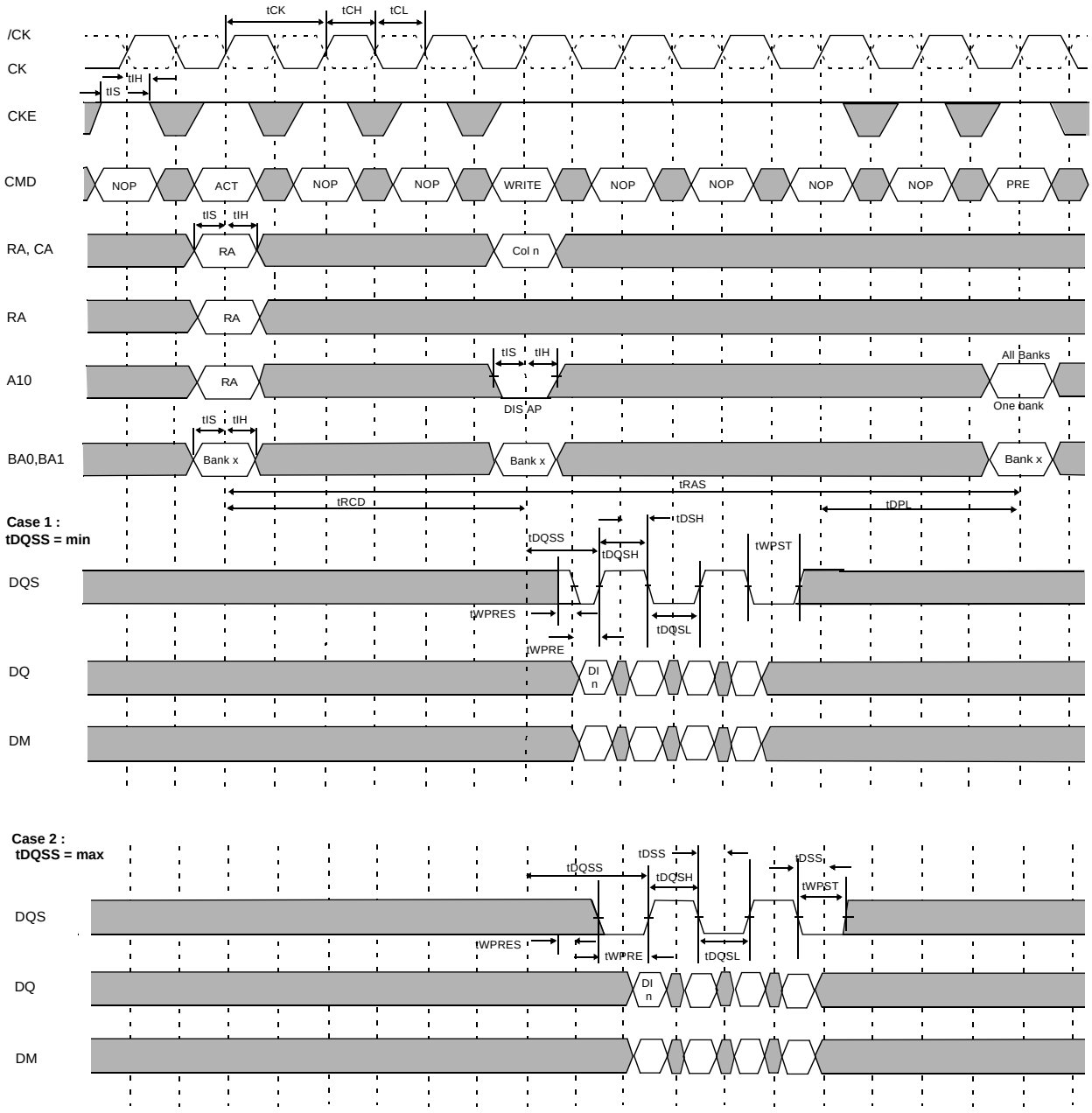


DI n = Data in for column n
Burst length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following Data In
EN AP = Enable Autoprecharge
* = * "Dont Care", if A10 is high at this point
ACT=Active, RA=Row Address, BA=Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Dont care

Bank Write Access

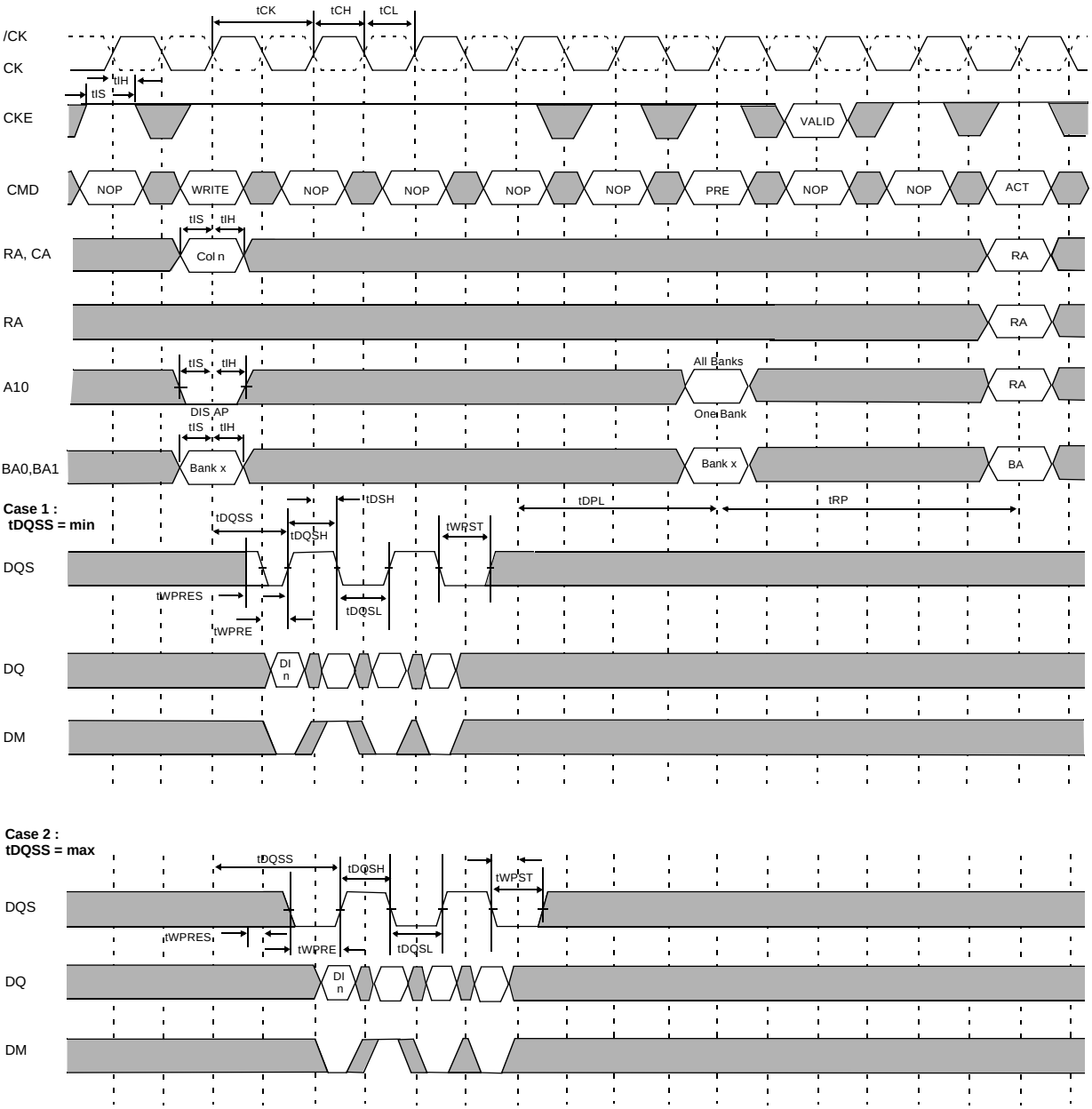


Dont care

DI n = Data in for column n
Burst length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following Data In
DIS AP = Disable Autoprecharge
* = * "Dont Care", if A10 is high at this point
PRE=Precharge, ACT=Active, RA=Row Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Write DM Operation



Dont care

DI n = Data in for column n
Burst length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following Data In
(the second element of the four is masked)
DIS AP = Enable Autoprecharge
* = * "Dont Care", if A10 is high at this point
PRE=Precharge, ACT=Active, RA=Row Address, BA=Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times