STw4510

2 step-down DC/DC converters / 5 LDO power management

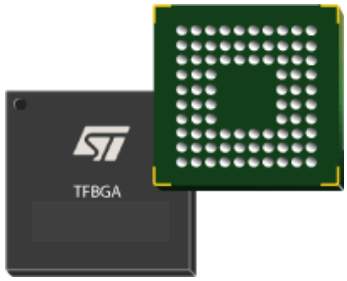
Preliminary Data

Features

- 2 Step-down converters
  - Vsdc1: 1 to 1.5 V with
    . 15 steps at 600 mA (I2C control available)
    . Programmable start-up value
    (1.2V by default)
  - Vsdc2: 1.8 V at 600 mA for general purpose usage
- 5 Low-drop output regulators for different uses
  - Vdig: 1.0V (100mA), 1.2V, 1.5V (250 mA)
    . Can be supplied by Vsdc2 to minimize the voltage drop
    . Programmable start-up value
    (1.2V by default)
  - Vana1: 1.5, 1.8, 2.5, 2.8 V - 150 mA
  - Vana2: 1.8, 2.8, 3.0, 3.3 V - 150 mA
  - Vana3: 1.8, 2.8, 3.0, 3.3 V - 150 mA
  - Vmmc: 1.8, 2.5, 2.85, 3.0 V - 150mA
- Miscellaneous
  - Vana(i) have programmable start-up output voltage and ON or OFF (default) status
  - 32 kHz input used for state machine
  - Processor supply monitoring
  - Processor reset control
  - Control by serial I2C interface
  - Thermal shutdown

Applications

- Any portable application
  - Mobile phones
  - Personal digital assistants (PDA)
  - Portable media players



TFBGA84 6 mm x 6 mm x 1.2 mm 0.5 mm pitch
TFBGA49 4 mm x 4 mm x 1.2 mm 0.5 mm pitch

Description

STw4510 is a 7-channel integrated power management device for application powered by one Li-Ion or Li-Polymer cell. STw4510 embeds 2 highly efficient step-down DC/DC converters and 5 LDO regulators.

It has been designed to typically supply portable processor and its peripherals. Thanks to the multiple output voltages, high current capability and programmable start-up value, it can easily adapt to various applications.

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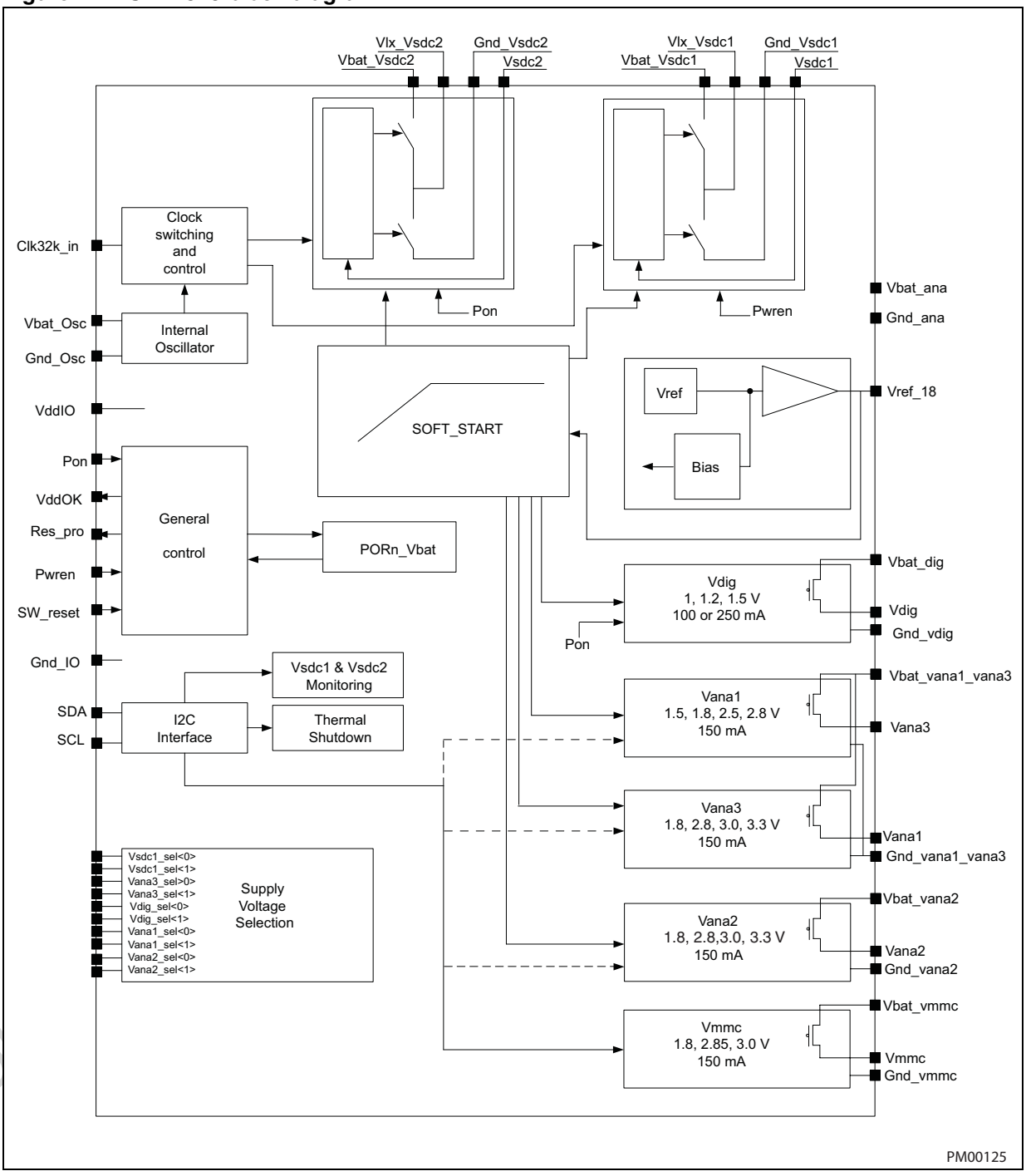
1 Functional block diagram

Figure 1. STw4510 block diagram



2 Ball information

The 6 mm x 6 mm package is useful for keeping all the selected value available for Vana(i) (i=1 to 3), Vdig and Vsdc1.

When using the 4 mm x 4 mm package, Vdig is set to 1.2V, Vsdc1 output voltage is controlled via I2C and Vana(i) have only one selection bit available instead of 2.

2.1 Ball connections in TFBGA84 6 mm x 6 mm package

Table 1. STw4510 ball connections in TFBGA84 6 mm x 6 mm x 1.2 mm package

	1	2	3	4	5	6	7	8	9	10
A	Clk32k_in	Gnd_Vsdc2	Vlx_Vsdc2	Vbat_Vsdc2	Vsdc2	Vdig	Vana1	Vana3	Vref_18	Vsdc1
B	“Reserved”	“Reserved”	Gnd_Vsdc2	Vbat_Vsdc2	Gnd_ana	Vbat_Vdig	Gnd_Vana1 _Vana3	“Reserved”	“Reserved”	Gnd_Vsdc1
C	“Reserved”	“Reserved”	Gnd_osc	Vlx_Vsdc2	Gnd_Vdig	Vbat_ana	Vbat_Vana1 _Vana3	Pon	Gnd_Vsdc1	Vlx_Vsdc1
D	Vbat_osc	“Reserved”	“Reserved”					Vlx_Vsdc1	Vbat_Vsdc1	Vbat_Vsdc1
E								Vsdc1_sel1	Gnd_Vana2	Reserved
F								Gnd_Vana2	Vbat_Vana2	Vana2
G								Gnd_IO	Vana1_sel1	VddIO
H						Pwren	SDA	Vana3_sel1	Vdig_sel1	Reserved
J		VddOK	Res_pro	Vbat_Vmmc	Vdig_sel0	SCL	Vana2_sel0	Vana3_sel0	Gnd_IO	Reserved
K				Sw_resetn	Vmmc	Vana1_sel0	Vsdc1_sel0	Vana2_sel1		Reserved

2.2 Ball connections in TFBGA49 4 mm x 4 mm package

Table 2. STw4510 ball connections in TFBGA49 4 mm x 4 mm x 1.2 mm package

	1	2	3	4	5	6	7
A	Gnd_Vsdc2	Vlx_Vsdc2	Vbat_Vsdc2	Gnd_ana	Vdig	Vbat_vdig	Vbat_vana1_ vana3
B	Gnd_Vsdc2	Vlx_Vsdc2	Vbat_Vsdc2	Vsdc2	Vbat-ana	Vana1	Vana3
C	Reserved	Reserved	Clk32k_in	Reserved	Pon	Gnd_Vsdc1	Gnd_Vsdc1
D	Gnd_osc	Reserved	Reserved	Vref_18	Vsdc1	Vlx_Vsdc1	Vlx_Vsdc1
E	Vbat_osc	Reserved	VddOK	Vana1_sel<0>	Reserved	Vbat_Vsdc1	Vbat_Vsdc1
F	Res_pro	SW_Reset	Pwren	SDA	Vana2_ sel<0>	Vana3_ sel<0>	Vminus
G	Vbat_mmc	Vmmc	SCL	Vana2	Vbat_ana2	VddIO	Vminus

2.3 Ball functions

STw4510 includes the following ball types

- VDDD/VDDA: Digital/analog power supply
- VSSD/VSSA: Digital/analog ground supply
- DO/DI/DIO: Digital Output / Digital Input / Digital Input-Output
- DOz: Digital Output with high impedance capability
- AO/AI/AIO: Analog Output / Analog Input / Analog Input-Output
- G: To be connected to ground
- O: To be left open

2.3.1 Signal description for the TFBGA84 6 mm x 6 mm package

Table 3. STw4510 ball description for the 6 mm x 6 mm package

Ball	Ball name	Ball type	Description
General supply balls			
D1	Vbat_osc	VDDD	Battery supply for digital/oscillator
C3	Gnd_osc	VSSD	Internal ground oscillator
C6	Vbat_ana	VDDA	Analog part battery supply
B5	Gnd_ana	VSSA	Analog ground
A9	Vref_18	AO	Internal reference
G10	VddIO	VDDD	IO digital supply
G8, J9	Gnd_IO	VSSD	IO ground
Digital control balls			
C8	Pon	DI (Nmos) Pull Down 1.5MΩ	Power-on and reset
K4	Sw_resetn	DI Vddio voltage Pull up 1.5MΩ	Software reset, reset all application, when Sw_resetn = 0
J2	VddOK	DO Vddio voltage	Supply monitoring for processor. Interruption for high temperature warning
J3	Res_pro	DO Vddio voltage	Reset for processor
H6	Pwren	DI Vddio voltage Pull up 1.5MΩ	Sleep mode from main processor
J6	SCL	DI Vddio voltage	I2C clock interface
H7	SDA	DIO Vddio voltage	I2C data interface
A1	Clk32k_in	DI Vddio voltage Pull Down 1.5MΩ	32 kHz clock input
Step down DC/DC converters & voltage regulators			
A4, B4	Vbat_Vsdc2	VDDA	Vsdc2 Step Down DC/DC input power supply converter
A2, B3	Gnd_Vsdc2	VSSA	Vsdc2 Step Down DC/DC ground converter

Table 3. STw4510 ball description for the 6 mm x 6 mm package (continued)

Ball	Ball name	Ball type	Description
A3, C4	Vlx_Vsdc2	AIO (Vbat)	Vsdc2 Step Down DC/DC output converter
A5	Vsdc2	AO (Vbat)	Vsdc2 Step Down DC/DC output converter
D9, D10	Vbat_Vsdc1	VDDA	Vsdc1 Step Down DC/DC input power supply converter
B10, C9	Gnd_Vsdc1	VSSA	Vsdc1 Step Down DC/DC ground converter
C10, D8	Vlx_Vsdc1	AIO (Vbat)	Vsdc Step Down DC/DC output converter
A10	Vsdc1	AO (Vbat)	Vsdc1 Step Down DC/DC output converter
C7	Vbat_Vana1_Vana3	VDDA	Vana1 & Vana3 low drop input supply regulator
A8	Vana3	AO (Vbat)	Vana3 low drop output supply regulator
B7	Gnd_Vana1_Vana3	VSSA	Vana1 & Vana3 low drop ground regulator
B6	Vbat_Vdig	VDDA	Vdig low drop input supply regulator
A6	Vdig	AO (Vbat)	Vdig low drop output supply regulator
C5	Gnd_Vdig	VSSA	Vdig low drop ground regulator
A7	Vana1	AO (Vbat)	Vana1 low drop output supply regulator
F9	Vbat_Vana2	VDDA	Vana2 low drop input supply regulator
F10	Vana2	AO (Vbat)	Vana2 low drop output supply regulator
E9, F8	Gnd_Vana2	VSSA	Vana2 low drop ground regulator
J4	Vbat_Vmmc	VDDA	Vmmc low drop input supply regulator
K5	Vmmc	AO (Vbat)	Vmmc low drop output supply regulator
Step down DC/DC converters & voltage selection			
K7	Vsdc1_sel0	DI (Vbat)	Vsdc1 voltage selection
E8	Vsdc1_sel1	DI (Vbat)	Vsdc1 voltage selection
J8	Vana3_sel0	DI (Vbat)	Vana3 voltage selection
H8	Vana3_sel1	DI (Vbat)	Vana3 voltage selection
J5	Vdig_sel0	DI (Vbat)	Vdig voltage selection
H9	Vdig_sel1	DI (Vbat)	Vdig voltage selection
K6	Vana1_sel0	DI (Vbat)	Vana1 voltage selection
G9	Vana1_sel1	DI (Vbat)	Vana1 voltage selection
J7	Vana2_sel0	DI (Vbat)	Vana2 voltage selection
K8	Vana2_sel1	DI (Vbat)	Vana2 voltage selection

Table 3. STw4510 ball description for the 6 mm x 6 mm package (continued)

Ball	Ball name	Ball type	Description
Interface balls			
K3, G3, K2, K9 H4, G2, H5 H1, K1, H3, J1, H2, F3, G1, F2, E1, E2, E3, F1	Not connected ball		to be left not connected
Other balls			
C1, D2, B9, D3	Reserved	G	To be connected to ground
B1, B2, B8, C2, E10, H10, J10, K10	Reserved	O	To be left opened

2.3.2 Signal description for the TFBGA49 4 mm x 4 mm package

Table 4. STw4510 ball description for the 4 mm x 4 mm package

Ball	Ball name	Ball type	Description
General supply balls			
E1	Vbat_Dig	VDDD	Battery supply for digital/oscillator
D1	Gnd_Dig	VSSD	Internal ground oscillator
B5	Vbat_ana	VDDA	Analog part battery supply
A4	Gnd_ana	VSSA	Analog ground
D4	Vref-18	AO	Internal reference
G6	VddIo	VDDD	IO digital supply
F7, G7	Vminus	VSSD	IO ground
Digital control balls			
C5	Pon	DI (Nmos) Pull Down 1.5MΩ	Power-on and reset
F2	Sw_Resetn	DI (VddIO voltage) pull up 1.5MΩ	Software reset, reset all application, when Sw-resetn =0
E3	VddOK	DO (VddIO voltage)	Supply monitoring for processor. Interruption for high temperature warning
F1	Res_pro	DO (VddIO voltage)	Reset for processor

Table 4. STw4510 ball description for the 4 mm x 4 mm package (continued)

Ball	Ball name	Ball type	Description
F3	Pwren	DI (VddIO voltage) pull up 1.5MΩ	Sleep mode from main processor
G3	SCL	DI (VddIO voltage)	I2C clock interface
F4	SDA	DI (VddIO voltage)	I2C data interface
C3	Clk32k_In	DI (VddIO voltage) pull up 1.5MΩ	32KHz clock input
Step down DC/DC conversers & voltage regulators			
A3, B3	Vbat_vscd2	VDDA	Vsdc2 step down DC/DC input power supply converter
A1, B1	Gnd_Vsdc2	VSSA	Vsdc2 step down DC/DC ground converter
A2, B2	Vlx_Vsd2	AIO (Vbat)	Vsdc2 step down DC/DC output converter
B4	Vsdc2	AO (Vbat)	Vsdc2 step down DC/DC feedback converter
E6, E7	Vbat_vscd1	VDDA	Vsdc1 step down DC/DC input power supply converter
C6, C7	Gnd_Vsdc1	VSSA	Vsdc1 step down DC/DC ground converter
D6, D7	Vlx_Vsd1	AIO (Vbat)	Vsdc1 step down DC/DC output converter
D5	Vsdc1	AO (Vbat)	Vsdc1 step down DC/DC feedback converter
A7	Vbat_Vana1_Vana3	VDDA	Vana1 & Vana3 low drop input supply regulator
B7	Vana3	AO (Vbat)	Vana3 low drop output supply regulator
A5	Vdig	AO (Vbat)	Vdig low drop output supply regulator
A6	Vbat_Vdig	VDDA	Vdig low drop input supply regulator
B6	Vana1	AO (Vbat)	Vana1 low drop output supply regulator
G5	Vbat_Vana2	VDDA	Vana2 low drop input supply regulator
G4	Vana2	AO (Vbat)	Vana2 low drop output supply regulator
G1	Vbat-Vmmc	VDDA	Vmmc low drop input supply regulator
G2	Vmmc	AO (Vbat)	Vmmc low drop output supply regulator
Voltage selection			
E4	Vana1_sel<0>	DI (Vbat)	Vana1 voltage selection
F5	Vana2_sel<0>	DI (Vbat)	Vana2 voltage selection
F6	Vana3_sel<0>	DI (Vbat)	Vana3 voltage selection
Other balls (connected to ground)			
C1	Reserved		Connected to ground
E2	Reserved		Connected to ground
E5	Reserved		Connected to ground

Table 4. STw4510 ball description for the 4 mm x 4 mm package (continued)

Ball	Ball name	Ball type	Description
Other balls (left opened)			
C2	Reserved		Left open
D2	Reserved		Left open
D3	Reserved		Left open
C4	Reserved		Left open

3 Functional description

3.1 Introduction

The STw4510 integrates supplies for the processor cores and associated peripherals

- Two step down DC/DC converters
  - Vsdc1 (programmable start-up and 1.2V default value), programmable via I2C interface, for the processor cores (*Table 18*)
  - Vsdc2, 1.8 V, for the Input/Output supply of all the system devices and for all peripherals which require 1.8 V supply (*Table 19*)
- Five low drop regulators for general purposes.
  - Four of them, Vana(i) (i=1 to 3) and Vdig can be used for critical features like PLL or analog and digital processor peripherals. These low-drop regulator output voltage values are programmable through **Vdig_sel [n]** and **Vana(i)_sel[j]** pads connected to Vbat or to ground. *Table 5* shows the available output voltages. The electrical characteristics are listed in *Table 20*, *Table 21* and *Table 22*.
  - The last one is Vmmc and can supply different feature and in particular SD/MMC card. This regulator is completely controlled via the I2C interface. *Table 6* shows the available output voltages. The electrical characteristics are indicated in *Table 21*.

Table 5. Low drop regulator output voltage programmable values

LDO	I (mA)	Output voltage values (V)							
		1.0	1.2	1.5	1.8	2.5	2.8	3.0	3.3
Vdig	250	X(1) (100mA)	X	X					
Vana1	150			X	X	X	X		
Vana2	150				X		X	X	X
Vana3	150				X		X	X	X

1. X means available output voltage value.

Table 6. Vmmc low drop regulator output voltage

LDO	I (mA)	Output voltage values (V)			
		1.8	2.5	2.85	3.0
Vmmc	150	X(1)	X	X	X

1. X means available output voltage value.

3.2 Digital control module

This module describes the interfaces used to program the device and the related registers.

3.2.1 State machine

Each state is described here below and represented in *Figure 2*

OFF: In this mode the STw4510 is switched off. Off is when **Pon** signal = “0”, when battery level is below 2.4V or when thermal shutdown is activated (in this particular case: not a permanent state). There is no power supply. The only active cell is the Vbat level detection.

OSC_START: Oscillator is enabled and the power up module is waiting for the rising edge of the internal signal ‘Osc_OK’ to start power up sequence. This state duration is 300 µs.

START_BIAS: Bias, reference and thermal shut-down are enabled, a counter is activated to wait for rising edge of internal signals ‘pdn_regulators’. This state duration has a typical value of 7.8 ms and a worst case value of 9.46 ms.

START_PM: soft start period, during this state, **Vdig, Vsdc2** progressively reach their final values. At the end of this state, processor power supplies (Vdig, Vsdc2) are available, internal signal ‘pdn_ls’ is set to 1 and then the device can allow I2C communication, output power supply monitoring and application. Typical duration of this state is 0.67ms and never goes over than the maximum duration of 1 ms.

OFF2: STw4510 is waiting for the 32 kHz processor signal. This state has an indeterminate duration. (if 32 kHz is present during the states describes above, it has no effect on STw4510 behavior, 32 kHz signal is taking in account by STw4510 at the end of START_PM state, the duration of this state is 0.4 ms minimum).

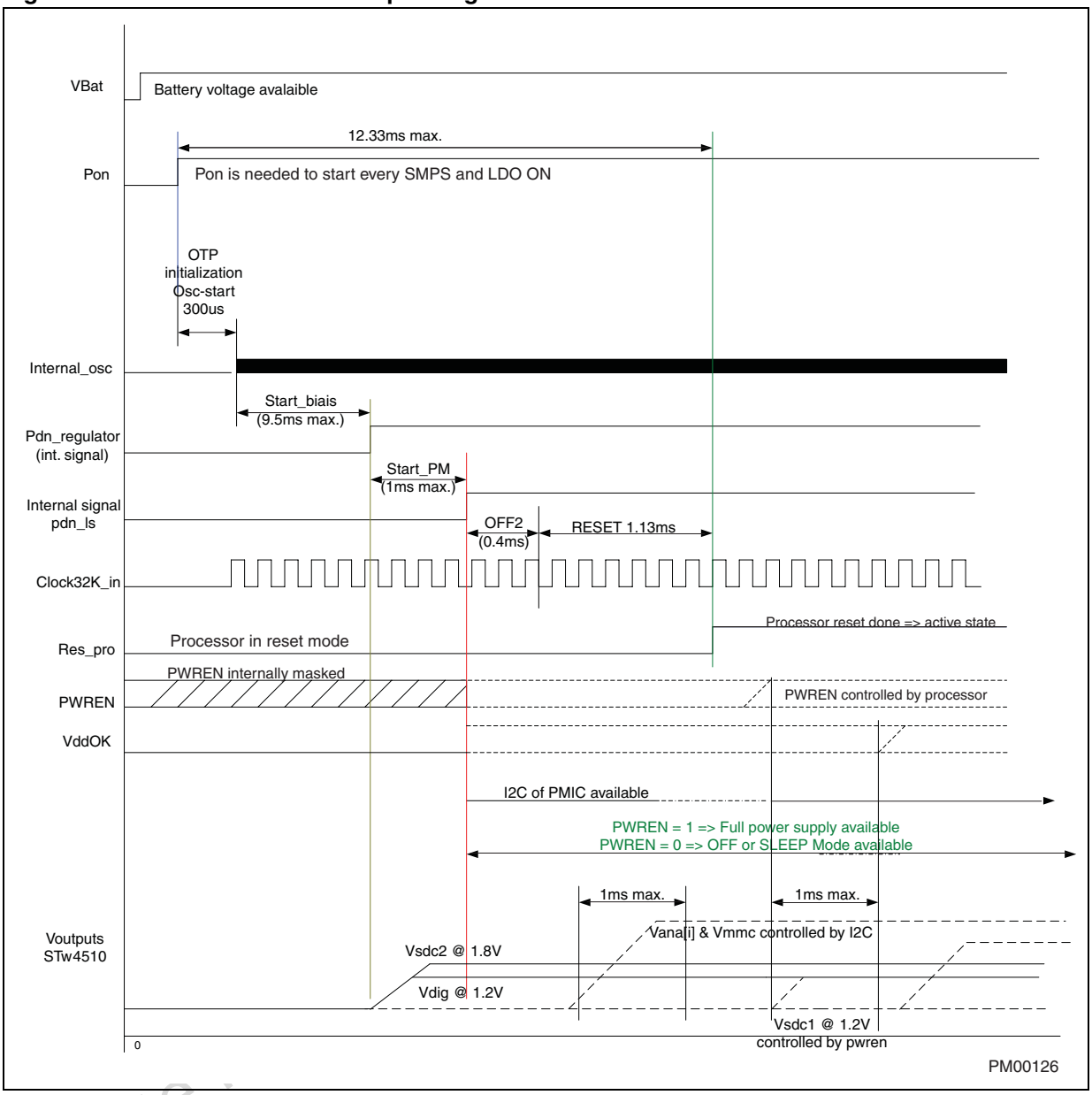
RESET: STw4510 forces a reset during 36*1/32 kHz period (duration of 1.13ms) before setting **Res_pro** signal high. This signal **Res_pro** is high if **Pon** is high and 32kHz clock available.

SLEEP & Vsdc1_OFF: Sleep mode (*Section 3.2.3*) and Vsdc1_OFF mode (*Section 3.2.4*) are required by processor by setting **Pwren** signal at low level. Then **VddOK** signal is forced to “0”, Step Down DC/DC converter Vsdc2, and LDO Vana_i (i = 1 to 3) switch to sleep mode, SMPS converter Vsdc1 switches off and wait for **Pwren** signal at high level (*Figure 3*).

WAKE-UP: From sleep mode and Vsdc1_OFF, the processor requests to switch back to high power mode (HPM) and ON mode for Vsdc1 by setting Pwren to high level. Thus the device switches regulators from Low power mode (sleep) to high power mode and informs processor with **VddOK** signal at high level (*Figure 3*).

Note: Sleep mode has no effect on Vdig nor Vmmc.

Figure 2. State machine: Start-up timing



Vsdc2, Vdig are started with internal pdn_regulators signals.

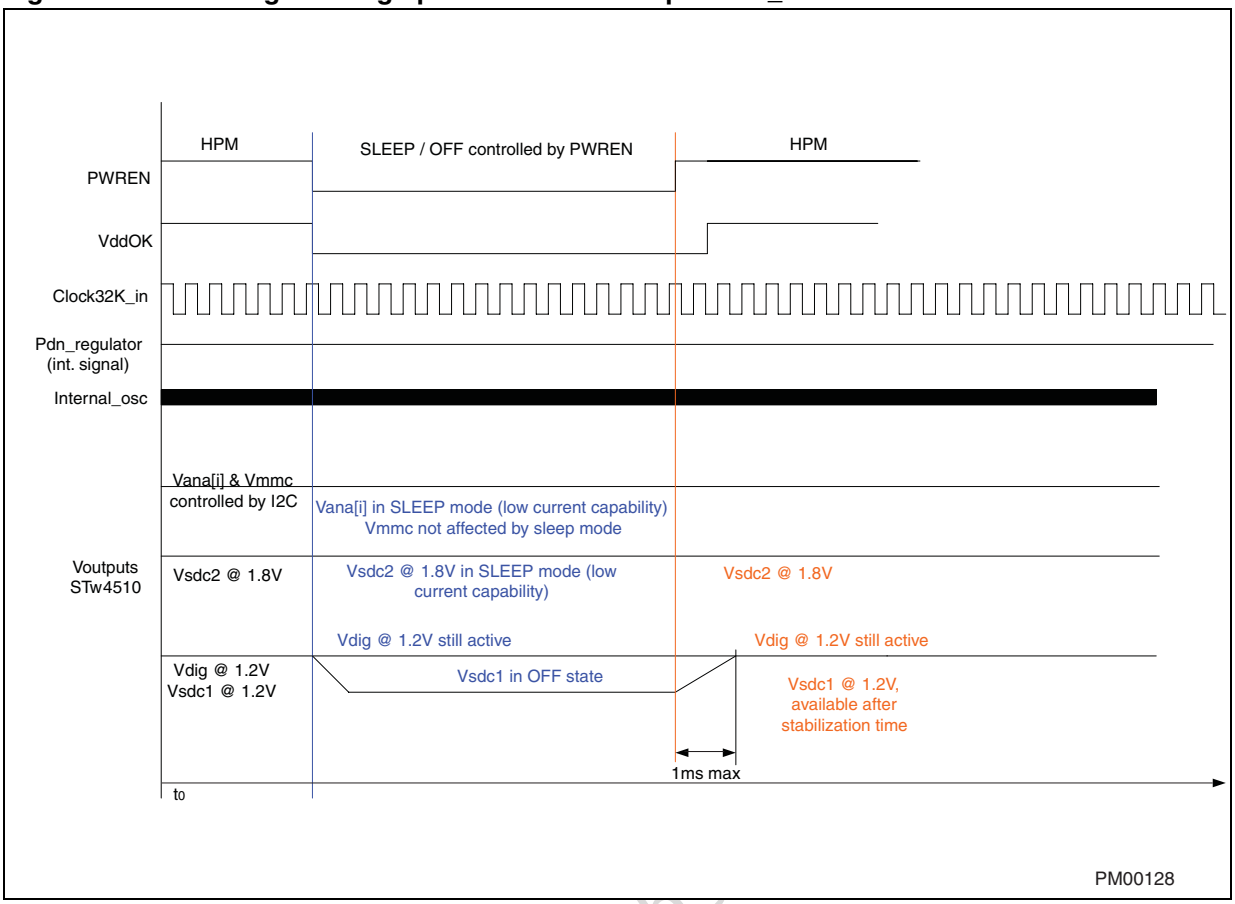
I2C is available after internal **'pdn_ls'** signal is set to "1".

Processor reset done on the **Res_pro** signal is synchronous of the 32 kHz clock.

During power-up, Pwren is masked. Nevertheless, Vsdc1 power supply that is controlled by **Pwren**, is in OFF state during the starting phase and this up to internal signal "**pdn_ls** =1" and then, the control of the Vsdc1 is done via the external **Pwren** signal.

The soft start feature limits the peak current sink in the Vbat supply when a supply is set to ON state.

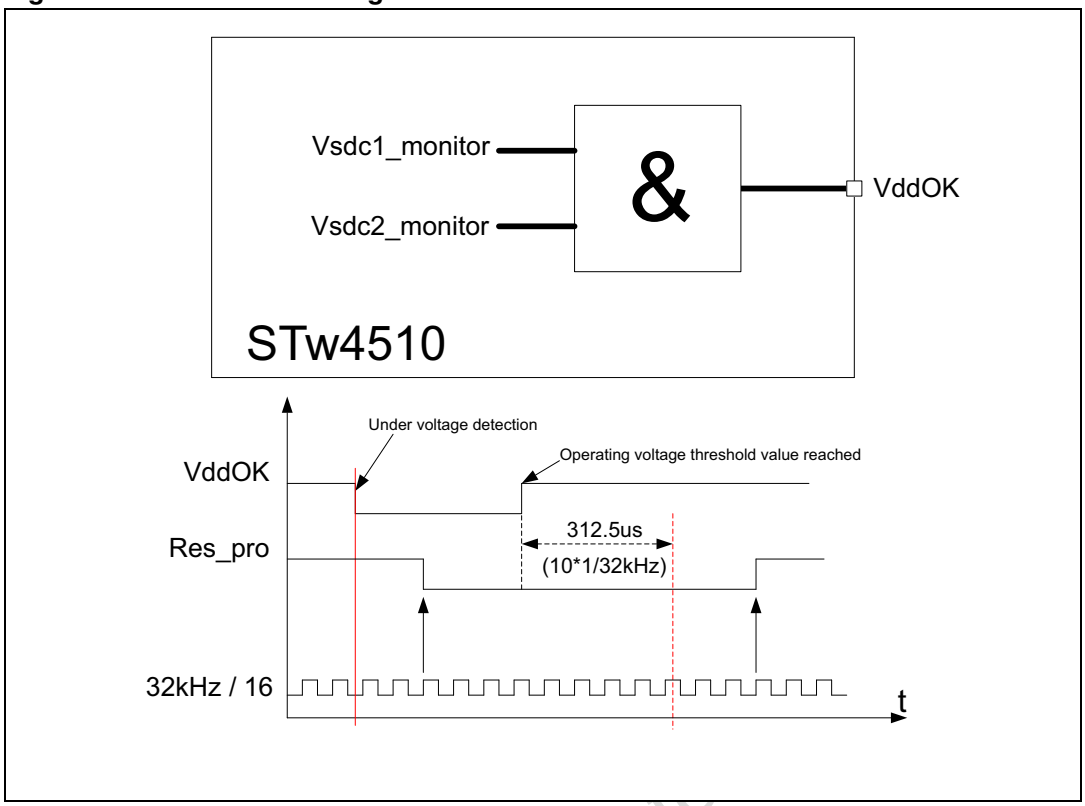
Figure 3. Switching from high power mode to sleep/Vsdc1_OFF mode



3.2.2 POWER OFF / VddOK

- In case of **VddOK** falling edge (under voltage on **Vsdc1**, **Vsdc2** detected), the processor is reset (**Res_pro** low during 1.8 ms minimum) and started again with no time-out. (See *Figure 4*)
- In case of **VddOK** falling down edge (under **Pwren** falling edge) the processor is not reset (Res_pro keeps its high level)
- In case of **Pon** falling edge (switch off of STw4510 from the main processor), the processor is also reset with no time-out. It is considered that clean switch off between modem and processor is done by software directly.

Figure 4. VddOK block diagram



3.2.3 Sleep mode

STw4510 sleep mode is only active with the presence of the 32kHz clock on pin Clk32_in and STw4510 power supplies Vsdc2, Vana1, Vana2, Vana3 go into sleep. The voltage is still present on the power supply output with current capability reduced. Sleep mode is activated each time the **Pwren** signal is at low level (logical 0).

To exit sleep mode state it is mandatory to have the **Pwren** signal at high level (logical 1).

In this present version, sleep mode is available each time Pwren = 0.

When Pwren = 0, some application may require that Vsdc2 and/or Vana(I) remain in high power mode. STw4510 may be able to comply with this requirement. For more information please contact the STMicroelectronics sales office.

3.2.4 Vsdc1_OFF mode

Vsdc1_OFF mode is only referenced to the **Pwren** signal. When **Pwren** signal is high (logical level 1) the Vsdc1 DC/DC regulator is in high power mode and the application processor can be supplied. In the case of **Pwren** is low level (logical 0) Vsdc1 is switched off and the consumption is reduced to the leakage current.

3.2.5 Power supplies at start-up

After Pon, and considering the state machine, different regulators (Vana(i), Vdig) can be switched ON or OFF at start-up with the default output voltage configured by the selection pin available.

In this present version, Vdig is ON at start-up and Vana(i) are switched OFF.

For more information, please contact STMicroelectronics sales office.

3.2.6 Device reset by processor Sw_resetn

In the event of a reset from processor to STw4510, **Sw_resetn** signal set to “0”, the device resets all control registers, except registers at address 1Eh, 1Fh and 03h.

As a consequence, after a Sw_reset, **Vmmc** is switched OFF, all **Vana(i)** (i=1 to 3) and **Vdig** are set to their start-up default value (ON or OFF).

When a low level is applied on **Pon** signal, all registers are reset at their initial value and **Pon** signal goes back to “1”.

3.2.7 I2C interface

The I2C interface controls power management and all programmable functions.

I2C is configured as slave serial interface compatible with I2C registered trademark of Phillips Inc. (version 2.1).

I2C interface description

STw4510 I2C is a slave serial interface with a serial data line (SDA) and a serial clock line (SCL)

SCL: input clock used to shift data

SDA: input/output bidirectional data transfers

It is composed of:

On filter to reject spikes on the bus data line and preserve data integrity

Bidirectional data transfers up to 400kbit/s (Fast-mode) via SDA signal

The SDA signal contains the input/output control and data signals that are shifted in the device, MSB first. The first bit must be high (START) followed by the Device ID (7 bits) and Read/Write bit control (1 indicates read access, a logical 0 indicates a write access).

Device ID:

Device ID in write mode: 5Ch (01011100)

Device ID in read mode: 5Dh (01011101)

STw4510 then sends an acknowledge at the end of an 8 bit transfer. The following 8-bits correspond to the register address followed by another acknowledge. The 8-bit data field is sent last and is also followed by a last acknowledge.

Table 7. Device ID

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/W

Table 8. Register address

b7	b6	b5	b4	b3	b2	b1	b0
RegADR7	RegADR6	RegADR5	RegADR4	RegADR3	RegADR2	RegADR1	RegADR0

Table 9. Register data

b7	b6	b5	b4	b3	b2	b1	b0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

I2C interface modes

Figure 5. Control interface: I2C format

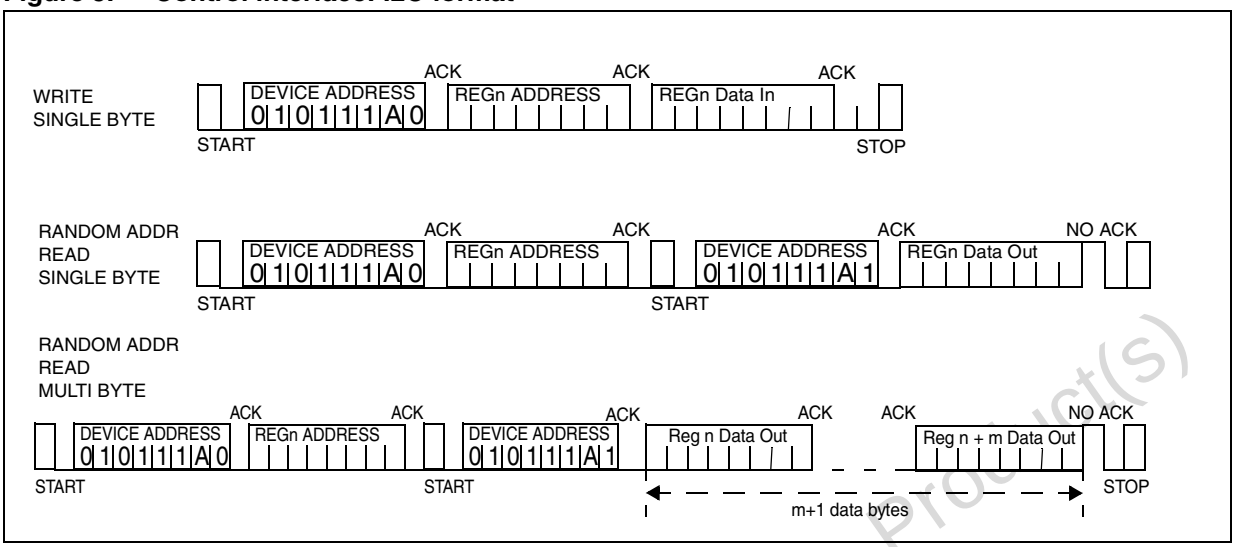
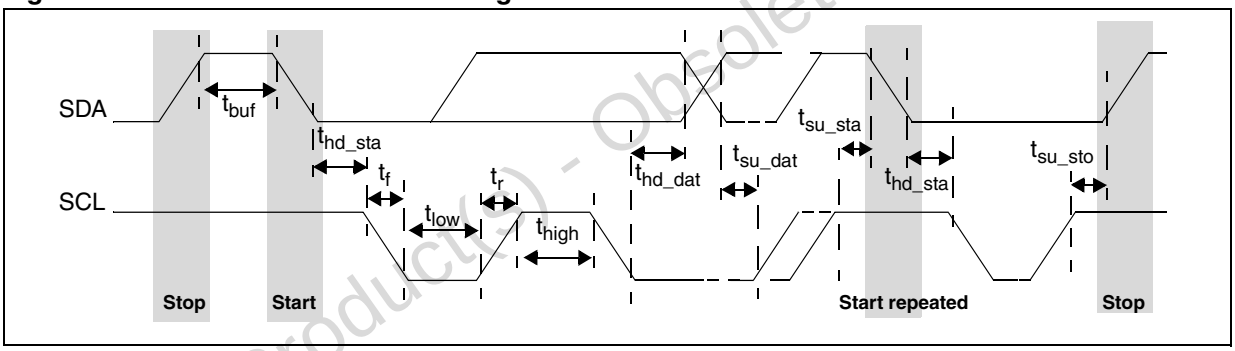


Figure 6. Control interface: I2C timing



Note: Multi-write possibility is not available. For each data it is mandatory to send the address first.

3.2.8 Control registers

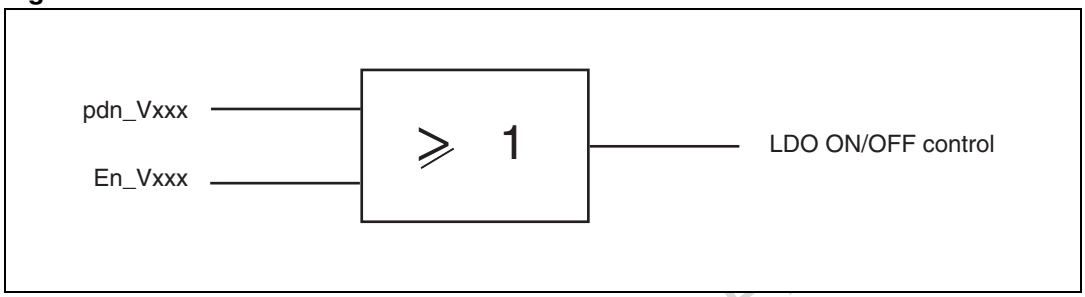
Control registers have the following functions:

- Manage high power, sleep and power down modes.
- Control the state machine

Switch ON/OFF control of LDO's can be done by I2C for Vana(i) and Vmmc. Two commands exist to turn ON/OFF the LDO's, one is **pdn_Vxxx** and the other one is **en_Vxxx** (Vxxx takes place of Vana1/2/3 or Vmmc); these commands have been put in different registers and the **pdn_Vxxx** has a easier accessibility than **en_Vxxx** that needs to program the two following registers 1F and 1E.

These two commands control the same LDO's and a logical OR had been design between these bits.

Figure 7. LDO ON/OFF control



Note: In the following tables, please set the bits noted "not used" or "reserved" at 0 when programming the registers.

Table 10. Register general information

Address	Type	Comment
00h, 01h, 02h		Reserved
03h	R	STw4510 version ID
10h	R/W	Application control register 1
11h	R/W	Application control register 2
12h to 1Dh		Test registers
1Eh to 1Fh	R/W	Power control registers

Register summary

Register	Add.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	00h	Reserved							
Reserved	01h	Reserved							
Reserved	02h	Reserved							
STw4510 version ID	03h	0	1	0	0	0	0	0	1
Application Control Register 1	10h	Reserved						pdn_ vana2	Reserved
Application Control Register 2	11h	pdn_ vana1	Reserved	monitoring_V sdc2 Vsdc1	0	pdn_ vana3	sel_vmmc<1:0>		pdn_ vmmc

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Power control	Reserved						reg address 2 bits		reg address 3 bits			data din/dout 4 bits				EN
Address	1Fh								1Eh							

Note: Register 1Fh must be sent on the I2C before the register 1Eh (MSB address must be sent first).

Application control register 1

7	6	5	4	3	2	1	0
Reserved						pdn_Vana2	Reserved
						R/W	

Address: 10h

Type: R/W

Reset: 0000_0000

Description:

[7:2] Reserved

[1] **pdn_vana2**
0: Vana2 in power down mode (default)
1: Vana2 in high power mode

[0] Reserved

Application control register 2

7	6	5	4	3	2	1	0
pdn_vana1	reserved	monitoring_vsdc2_vsdc1	0	pdn_vana3	sel_vmmc[1:0]		pdn_vmmc
R/W		R(1)	W	R/W	R/W		R/W

1. These bits are reset (0) after reading

Address: 11h

Type: R/W

Reset: 0000_0000

Description:

[7] **pdn_vana1**
0: Vana1 in power down mode (default)
1: Vana1 in high power mode

[6] **Reserved**

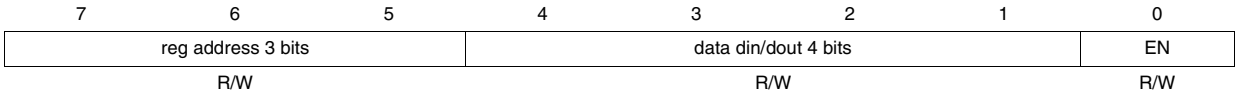
[5] **monitoring_vsdc2_vsdc1**
0: Outputs in the good range (default)
1: Outputs lower than expected on Vsdc2 or Vsdc1

[3] **pdn_vana3**
0: Vana3 in power down mode (default)
1: Vana3 in high power mode

[2:1] **sel_vmmc[1:0]**
00: 1.8V selection (default)
01: 2.5V selection
10: 2.85V selection
11: 3V selection

[0] **pdn_vmmc**
0: Vmmc in power down mode
1: Vmmc in high power mode

Power control register @ 1Eh



Address: 1Eh

Type: R/W

Reset: 0000_0000

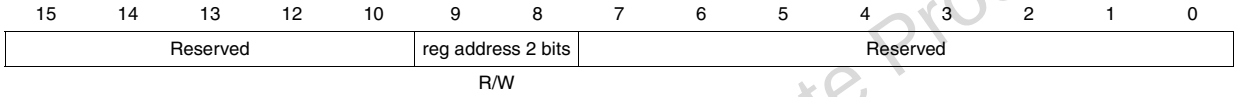
Description:

[7:5] **reg address 3 bits**
See *Table 11* “Address” column (LSB’s). Default = 0

[4:1] **data din/dout 4 bits**
See *Table 11* control register

[0] **EN**
0: Read enabled (default)
1: Write enabled

Power control register @ 1Fh



Address: 1Fh

Type: R/W

Reset: 0000_0000

Description:

[15:8] Reserved

[9:8] **reg address 2 bits**
See *Table 11* “Address” column (MSB’s), default = 0

[7:0] Reserved

Power control register mapping

Table 11. Power control register mapping

Address 1Fh								Address 1Eh								Comment
Reserved						reg address					data din/dout				EN	
						2-bit MSB		3-bit LSB								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						00h to 04h										Test purpose
						05h to 08h					Setting					*Power control register @ 05h* to *Power control register @ 08h*
						0Bh to 1E										Test purpose

Power control register @ 05h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						0	0	1	0	1	vsdc1_prg[3:0]				EN
											R/W				R/W

Address: 05h

Type: R/W

Reset: 0001_0000

Description:

[15:10] Reserved

[4:1] **vscd1_prg[3:0]**
0000: 1.00 V
0001: 1.05V
0010: 1.10V
0011: 1.15V
0100: 1.20V (default)
0101: 1.22V
0110: 1.24V
0111: 1.26V
1000: 1.28V
1001: 1.30V
1010: 1.32V
1011: 1.34V
1100: 1.36V
1101: 1.38V
1110: 1.40V
1111: 1.50V

[0] **EN**
0: Read enabled (default)
1: Write enabled

Power control register @ 06h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						0	0	1	1	0	en_vana1	en_vdig	Reserved	1	EN
												R/W			R/W

Address: 06h

Type: R/W

Reset: 0000_1000

Description:

[15:10] Reserved

[4] **en_vana1**
0: Vana in power down mode (default)
1: Vana in high power mode

[3] **en_vdig**
0: Vdig in power down mode
1: Vdig in high power mode (default)

[2] Reserved

[0] **EN**
0: Read enabled (default)
1: Write enabled

Power control register @ 07h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						0	0	1	1	1	en_vana3	Reserved			EN
												R/W			R/W

Address: 07h

Type: R/W

Reset: 0000_0000

Description:

[15:10] Reserved

[4] **en_vana3**
0: Vana3 in power down mode (default)
1: Vana3 enabled in high power mode

[3:1] Reserved

[0] EN
0: Read enabled
1: Write enabled

Power control register @ 08h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						0	1	0	0	0	reserved	en_monitoring	en_ vana2	Re-served	EN
											R/W	R/W	R/W		R/W

Address: 08h

Type: R/W

Reset: 0000_1000

Description:

[15:10]**Reserved**

[4]**Reserved**

[3]**en_monitoring**

0: Disabled/ Monitoring = OFF

1: Enabled/Vsdc1 & Vsdc2 monitoring = ON (default)

[2]**en_vana2**

0: Vana2 in power down mode (default)

1: Vana2 enabled in high power mode

[1]**Reserved**

[0]**EN**

0: Read enabled (default)

1: Write enabled

3.2.9 IT generation

STw4510 has one interrupt signal: **VddOK**. This signal has two functions:

- When **VddOK** is high, Vsdc1 and Vsdc2 output voltages are within the right range
- When **VddOK** is low,
  - it means that step-up DC/DC output converter (**Vsdc1** or **Vsdc2**) are not regulated properly. The internal interrupt set to “1” the bit 5 of the *Application control register 2*. This bit is reset after reading.
  - it means that the signal **Pwren** is low and sleep mode has been requested.

3.3 Power management module

STw4510 includes step-down DC/DC converters and regulators that supply the portable application. These supplies can work in different modes depending on the application needs.

The nominal mode is called high power mode (HPM). The mode is selected by **Pwren** signal according to the state of the portable processor and of STw4510.

When **Pwren** signal = “0”, sleep mode and Vsdc1_OFF are selected. High power mode is selected as default when **Pwren** signal = “1”.

When the STw4510 has it **Pwren** signal = “0”, the Vsdc2, Vanai (i = 1 to 3) current output are reduced to save energy via the lower capability output current.

Each supply has a dedicated battery power supply and Vdig that has low output voltage capabilities (1V, 1.2V, 1.5V) can be supplied by Vsdc2 to minimize the regulator voltage drop, thus, reducing the power dissipation.

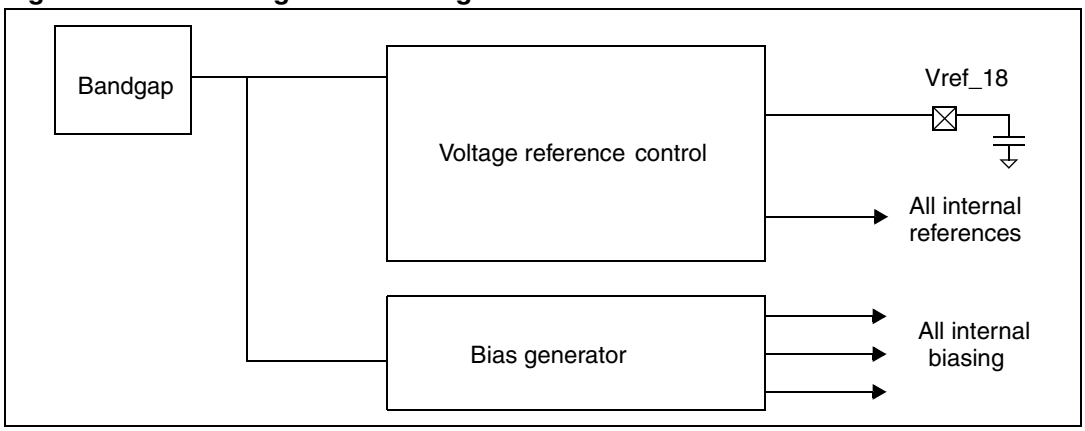
Each supply can be controlled and powered down through I2C programming, Pwren or by Pon signals, excepted **Vdig** and **Vsdc2**. Power down can be programmed by default at power up (special device configuration with dedicated start-up, see *Section 3.2.5: Power supplies at start-up*) or during the application management (*Power control register @ 06h*, *Power control register @ 07h*, *Power control register @ 08h*).

Table 12. Power supplies status

Power supplies	PWREN status		I2C interface control	Status after Pon - Initial status
	0	1		
Vsdc1 @ 1.2V	OFF	ON	Value can be changed	OFF
Vdig @ 1.2V (alive)	No effect	No effect	No effect	ON
Vsdc2 @ 1.8V (alive)	Sleep mode	HPM	No effect	ON
Vana1 @ 2.8V	Sleep mode	HPM	Switch ON/OFF	OFF
Vana3 @ 2.8V	Sleep mode	HPM	Switch ON/OFF	OFF
Vana2 @ 3.3V	Sleep mode	HPM	Switch ON/OFF	OFF
Vmmc @ 3.0V	No effect	No effect	Switch ON/OFF and value can be changed	OFF

In addition, an output current limitation prevents high current delivery in case of output short circuit. Band gap, biasing and references have been performed by dedicated blocks.

Figure 8. Block diagram of biasing and references of the device



3.3.1 Power supply domains

Table 13 lists the register bits and the signals that control the different STw4510 supply domains for each supply.

Table 13. Power supply domains

Supply name	Description	Supply domains		
		HPM	Sleep	Power down
Vsdc1	Step-down	through vsdc1_prg[3:0] bits then Vsdc1_sel[1:0] pads = 00 600 mA	No	Pwren signal low (logical 0)
Vsdc2	Step-down	1.8 V 600 mA	10 mA	Pon signal (low logical 0)
Vana1	LDO	1.5, 1.8, 2.5, 2.8 V Vana1_sel[1:0] pads 150 mA	0.5 mA	pdn_vana1 bit, or en_vana1 bit
Vana2	LDO	1.8, 2.8, 3.0, 3.3V Vana2_sel[1:0] pads 150 mA		pdn_vana2 bit, or en_vana2 bit
Vana3	LDO	1.8, 2.8, 3.0, 3.3V Vana3_sel[1:0] pads 150 mA		pdn_vana3 bit, or en_vana3 bit
Vdig	LDO	1, 1.2, 1.5 V Vdig_sel[1:0] pads 250 mA	No	en_vdig bit
Vmmc	LDO	1.8, 2.5, 2.85, 3 V sel_vmmc[1:0] bits 150 mA	No	pdn_vmmc

3.3.2 Vsdc1 step-down DC/DC converter

Vsdc1 step down DC/DC converter is suitable to supply the core of the processor. **Vsdc1** generates the regulated power supply with a very high efficiency. The 15 voltage levels enable dynamic voltage suitable for any supply voltage of CMOS process. The regulated output voltage levels are adjustable by the power control registers (*Power control register @ 05h*) via I2C interface. The power up and down is controlled by the signal **Pwren**.

The step down DC/DC converter runs on the internal RC oscillator.

Main features:

- Programmable output voltage:
  - **Vsdc1_sel [1:0]** pads is fixed to 00 (directly connected to ground)
  - 15 levels from 1.0 V to 1.5 V (vsdc1_prg [3:0] bits of power control register - *Power control register @ 05h*)
- Fixed voltage can also be selected with Vsdc1_sel[1:0] (feature only available on the die and on the 6 mm x 6 mm package):
  - 01: fixed output voltage1.5V
  - 10: fixed output voltage1.3V
  - 11: fixed output voltage1.4V
- 2 power domains:
  - High power mode (HPM), 600 mA full load
  - Power down mode when step down DC/DC converter is switched off, no consumption. The switch ON/OFF is controlled by the **Pwren** signal. **VddOK** signal indicates to the processor that **Vsdc1** supply is in the specified range.
- Soft start circuitry from power off to high power mode
- Specification guaranteed with input voltage from 2.7 V up to 5.5 V

Note: High voltage level changes can be performed according to the device monitoring constraints. Please refer to the application note AN2537 which explains how to change VCORE value with high steps.

3.3.3 Vsdc2 step down DC/DC converter

The **Vsdc2** step down DC/DC converter is designed to supply the IOs of the processor and its peripherals (memories DDR-SDRAM for example).

Vsdc2 output has a fixed 1.8V output voltage.

The step down DC/DC converter runs on the internal RC oscillator.

Main features

- Fixed 1.8 V output voltage
- Three power domains:
  - High power mode - 600 mA full load
  - Sleep mode with a 10 mA low current capability. (*Table 19: Vsdc2 DC/DC step-down converter*)
    Fast switching from sleep mode (low current output capability) to high power mode. The step down DC/DC converter is in sleep mode when the portable processor controls the **Pwren** signal to 0 indicating that the portable processor is able to switch to sleep mode. **VddOK** signal indicates to the processor that Vsdc2 supply is in the specified range.
  - Power down mode when step down DC/DC converter is switched off, no consumption. The ON/OFF sequence is controlled by **Pon**; **Pon** signal is set to 0 and Vsdc1 is switched off.
- Soft start circuitry from power off to high power mode
- Specification guaranteed with input voltage from 2.7 V up to 5.5 V

Note: The definition of sleep mode is given in Section 3.2.3.

3.3.4 Vana1

This LDO is dedicated, for example, to supply an analog part of a peripheral associated to a processor.

Main features

- Programmable output voltage: **Vana1_sel[1:0]** pads - 1.5, 1.8, 2.5, 2.8 V (to be fixed in the application by routing to Vbat or ground). On the 4 mm x 4 mm package the selection of output voltage values is limited to Sel[0] and the available voltage values are 2.5 V and 2.8 V.
- Three power domains:
  - High power mode, 150 mA full load
  - Sleep mode with a low current capability of 0.5 mA full load (*Table 20*)
  - Power down mode when regulator is switched off and there is no power consumption (pdn-vana1 bit of application control register (*Application control register 2*) or en_vana1 bit of power control register - (*Power control register @ 06h*), it is recommended to use only the pdn_vana1 control bit.
- Default setting defined by start-up device configuration
- Specification guaranteed with battery voltages from 2.7 V up to 5.5 V (battery voltage of 3.5 V for a LDO output of 3.3V with full characteristics available).

Note: The definition of sleep mode is given in Section 3.2.3.

3.3.5 Vana2

This LDO is dedicated, for example, to supply an analog part of a peripheral associated to a processor.

Main features

- Programmable output voltage: **Vana2_sel[1:0]** pads 1.8 V, 2.8 V, 3.0 V, 3.3 V (to be fixed in the application by routing to Vbat or ground). On the 4 mm x 4 mm package the selection of output voltage values is limited to Sel[0] and the available voltage values are 3.0 V and 3.3 V”
- Three power domains:
  - High power mode, 150 mA full load
  - Sleep mode with a low current capability of 0.5 mA full load (*Table 21*)
  - Power down mode when regulator is switched off and there is no power consumption (pdn-vana2 bit of application control register (*Application control register 1*) or en_vana2 bit of power control register - (*Power control register @ 08h*), it is recommended to use only the pdn_vana2 control bit.
- Default setting defined by start-up device configuration
- Specification guaranteed with battery voltages from 2.7 V up to 5.5 V (with a minimum battery voltage of 3.0 V for a LDO output of 2.8 V)

Note: The definition of sleep mode is given in Section 3.2.3.

3.3.6 Vana3

This LDO is dedicated, for example, to supply a critical stage like a PLL of a processor or an analog part of a peripheral associated to a processor

Main features

- Programmable output voltage: **Vana3_sel[1:0]** pads - 1.8 V, 2.8 V, 3.0 V, 3.3 V (to be fixed in the application by routing to Vbat or ground). ground. On the 4 mm x 4 mm package the selection of output voltage values has been limited to Sel[0] and the available voltage values are 3.0 V and 3.3 V.
- Three power domains:
  - High power mode, 150 mA full load
  - Sleep mode with a low current capability of 0.5 mA full load (*Table 21*)
  - Power down mode when regulator is switched off and there is no power consumption (pdn-vana3 bit of application control register (*Application control register 1*) or en_vana3 bit of power control register - *Power control register @ 07h*), it is recommended to use only the pdn_vana3 control bit.
- Default setting defined by start-up configuration
- Specification guaranteed with battery voltages from 2.7 V up to 5.5 V (with a minimum battery voltage of 3.5V for a LDO output of 3.3 V with the full characteristics available)

Note: The definition of sleep mode is given in Section 3.2.3.

3.3.7 Vdig

This LDO is dedicated, for example, to supply a alive digital part of peripherals associated to a processor.

Main features

- Programmable output voltage: **Vdig_sel[1:0]** pads - 1 V, 1.2 V, 1.5 V (to be fixed in the application by internal routing to Vbat or ground)
- Two power domains:
  - High power mode, 100mA full load when 1V output voltage selected, otherwise 250 mA full load.
  - Power down mode when regulator is switched off and there is no power consumption. Switch on and off is controlled by **Pon** signal. **Pon** is set to “0” and **Vdig** is switched off. **Vdig** has its voltage output available once **Pon** is set to “1” and the start-up sequence has ended.
- Default setting defined by start-up device configuration.
- Positive supply could be generated by Vsdc2 step down DC/DC converter.

3.3.8 Vmmc power supply

This block provides the power supply (1.8 V, 2.5 V, 2.85 V or 3 V) requested for MultiMedia Cards applications. This LDO can also be used for any other feature in the application.

Main features

- Programmable output voltage by I2C (1.8 V, 2.5 V, 2.85 V or 3 V)
- 2 power domains:
  - High power mode, 150 mA full load
  - Power down mode when regulator is switched off via I2C and there is no power consumption. Leakage is reduce to 1 µA.
- Specification guaranteed with battery voltages from 2.7 V up to 5.5 V (minimum Vbat values are indicated in *Table 23*).

3.3.9 Power supply monitoring

This block monitors the Vsdc1 and Vsdc2 output voltage. If Vsdc1 or Vsdc2 drop below the threshold the processor is reset.

This feature can be desactivated by setting en_monitoring bit of Power control register (*Power control register @ 08h*) to “0”.

3.3.10 Thermal shut-down

A thermal sensor is used to monitor die temperature. As soon as the die temperature exceeds the thermal threshold, the supplies are turned off via an internal ‘thermal_id” signal. The IC turns the default supply back on after around 10 ms. Only the voltages present at start-up are switched on again and the device temperature can decrease. The device is ready to be controlled by I2C to supply the application again.

Table 14. Thermal shutdown threshold

Description	Min	Typ	Max	Unit
Threshold		150		°C

4 Electrical and timing characteristics

Otherwise specified typical parameters are defined for ambient T = 25 °C, Vbat = 3.6 V.

4.1 Absolute maximum ratings

Table 15. STw4510 absolute maximum ratings

Symbol	Description	Min.	Typ.	Max.	Units
	Maximum power supply	-0.5		7	V
Ta	Maximum operating ambient temperature	-30		85	°C
Tj	Maximum junction temperature	-30		150	°C
	Recommended operating junction temperature			125	°C
Vesd	ESD - HBM model(1)	- 2(2)		2	kV
Vesd	ESD - CDM model(3)	- 300		500	V

1. Human Body Model: Standard JEDEC: JESD22-A114D
2. Except for the configuration when ESD is measured versus Vbat-Dig -1.8kV
3. Charged Device Model: Standard JEDEC: JESD22-C101C

4.2 Power supply

Note: STw4510 sleep mode is only active with the presence of the 32 kHz clock on pin Clk32_in and *STw4510 has different ways to go in sleep mode.*

In all the following tables:

- High power mode is defined as “SLEEP = ‘0’”,
- “Sleep mode” is defined as “SLEEP = ‘1’

4.2.1 Operating conditions

Table 16. Operating conditions

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
V_{BAT}	Power supply		2.7		5.5	V
I_{QSLEEP}	Quiescent current	Sleep mode		170	250	µA
I_{QSTDBY}		Off mode (T = 25°C)			5	µA

4.2.2 Vref18

Table 17. Vref18

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
V_{BAT}	Supply voltage		2.7		5.5	V
V_{REF_18}	Output voltage		1.78	1.8	1.84	V
PSRR	Power supply rejection ratio	f ≤100 kHz		60		dB
	Noise	100Hz ≤f ≤100 kHz		30		µV
t_S	Settling time(1)			7.8	10	ms

1. Delay until Pon rises at high level and 1.8 V is available on Vref18 pin.

4.2.3 Vsdc1 DC/DC step-down converter

Table 18. Vsdc1 DC/DC step-down converter

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vsdc1 regulator in high power mode						
V_{BAT}	Input power supply		2.7	3.6	5.5	V
V_{OUT}	Programmable output voltage	Vsdc1_sel[1:0] = 00 * vsdc1_prg[3:0] 1111 1110 1101 1100 1011 1010 1001 1000 0111 0110 0101 0100 (default) 0011 0010 0001 0000	 -5% -5% -5%	 1.50 1.40 1.38 1.36 1.34 1.32 1.30 1.28 1.26 1.24 1.22 1.20 1.15 1.10 1.05 1.00	 +5% +5% + 5%	V
V_{RIPPLE}	Output voltage ripple	Vsdc1 = 1.2 V I_{OUT} = 200 mA		10		mVpp
I_{OUT}	Output current				600	mA
P_{EFF}	Power efficiency	Vsdc1 = 1.2 V I_{OUT} = 200 mA		86		%
I_{SHORT}(1)	Short circuit current limitation		0.9	1.2	1.4	A
$I^{(2)}_{Q}$	Quiescent current	I_{OUT} = 0 mA			5	µA
I_{LKG}	Power-down current	en_vsdc1 = 0			1.5	µA
PSRR(1)	Power supply rejection	Vsdc1 = 1.2 V I_{OUT} = 200 mA Vpp = 0.3 V, F: [0; 20] kHz	40			dB
S_R	Rising slope	I_{OUT} = 10 mA		0.55		ms/V
Lir	Line regulation	V_{BAT}: [2.7; 5.5] V			10	mV
Ldr	Load regulation	I_{OUT}: [0.1; 600] mA			10	mV

Table 18. Vsdc1 DC/DC step-down converter (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Lirt	Transient line regulation	Vsdc1 = 1.2 V I_{OUT} = 200 mA ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		7		mV
Ldrt	Transient load regulation	Vsdc1 = 1.2 V I_{OUT}: [1; 400] mA $t_R = t_F$ = 100ns		70		mV

1. Guaranteed by design
2. Quiescent current defined is the current measured on the power supply dedicated to the voltage Vsdc1

4.2.4 Vsdc2 DC/DC step-down converter

Table 19. Vsdc2 DC/DC step-down converter

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vsdc2 regulator in high power mode (SLEEP = '0')						
V_{BAT}	Input power supply		2.7	3.6	5.5	V
V_{OUT}	Output voltage(1)		-3%	1.8	+3%	V
V_{RIPPLE}	Output ripple	I_{OUT} = 200 mA		10		mVpp
I_{OUT}	Output current				600	mA
P_{EFF}	Power efficiency	I_{OUT} = 200 mA		90		%
I_{SHORT}(2)	Short circuit current limitation		0.9	1.2	1.4	A
I_Q(3)	Quiescent current	I_{OUT} = 0 mA			5	µA
I_{LKG}	Power-down current	en_vsdc2 = 0			1.5	µA
PSRR(2)	Power supply rejection	I_{OUT} = 200 mA Vpp = 0.3 V, F: [0; 20] kHz	40			dB
T_R	Rising time (10 % to 90 %)			1		ms
Lir	Line regulation	V_{BAT}: [2.7; 5.5] V			10	mV
Ldr	Load regulation	I_{OUT}: [0.1; 600] mA			10	mV
Lirt	Transient line regulation	I_{OUT} = 200 mA ΔV_{BAT}= 300 mV $t_R = t_F$ = 10 µs		7		mV
Ldrt	Transient load regulation	I_{OUT}= [1; 400] mA $t_R = t_F$ = 100 ns		70		mV

Table 19. Vsdc2 DC/DC step-down converter (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vsdc2 regulator in sleep mode (SLEEP='1')						
V_{BAT}	Input power supply		2.7	3.6	5.5	V
V_{OUT}	Output voltage(1)		-3 %	1.8	+3 %	V
V_{RIPPLE}	Output ripple	I_{OUT} = 5 mA		10		mV
I_{OUT}	Output current				10	mA
P_{EFF}	Power efficiency	I_{OUT} = 5 mA		90		%
$I^{(3)}_{Q}$	Quiescent current	I_{OUT} = 0 mA			2	µA
Lir	Line regulation	[V_{BAT} [2.7; 5.5] V			10	mV
Ldr	Load regulation	I_{OUT}: [0.1; 10] mA			10	mV
Lirt	Transient line regulation	I_{OUT} = 5 mA ΔV_{BAT}= 300 mV $t_R = t_F$ = 10 µs		2		mV

1. Including output voltage temperature coefficient, DC line and load regulations, voltage reference accuracy, industrial manufacturing tolerances and ripple voltage due to switching.
2. Guaranteed by design
3. Quiescent current defined is the current measured on the power supply dedicated to the voltage Vsdc2

4.2.5 LDO regulators

Vana1 and Vana3 low drop regulators have the same characteristics, the parameters given in *Table 20* are applicable to both regulators, in *Table 20*, Vana(i) stands for Vana3 with the new design to reach 3.3V maximum voltage output.

Vana1

Table 20. LDO regulators - Vana 1

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vana(i) regulator in high power mode (pdn_vana1 = 1, SLEEP = '0')						
V_{BAT}	Input power supply	Vana1 = 1.5 V/1.8 V/ 2.5 V	2.7	3.6	5.5	V
		Vana1 = 2.8 V	3	3.6	5.5	
V_{OUT}	Output voltage	Vana1_sel[1:0]pads 00 01 10 11	-3 %	 1.5 1.8 2.5 2.8	+3 %	V
I_{OUT}	Output current				150	mA
I_{SHORT}(1)	Short-circuit limitation		230	340	550	mA
I_Q(2)	Quiescent current	I_{OUT} = 0 mA			30	µA
I_{LKG}	Power-down current				1	µA
PSRR(1)	Power supply rejection	Vana1 = 2.8 V I_{OUT} = 150 mA Vpp = 0.3 V, F: [0; 20] kHz		50		dB
		Vana1 = 2.8 V I_{OUT} = 10 mA Vpp = 0.3 V, F: [0; 10] kHz F: [10; 100] kHz		 50 45		dB
T_R	Rising time (10 % to 90 %)	Vana1 = 2.8 V I_{OUT} = 10 mA		1.5		ms
Lir	Line regulation	V_{BAT}: [2.7; 5.5] V			5	mV
Ldr	Load regulation	I_{OUT}= [0.1; 150] mA			10	mV
Lirt	Transient line regulation	Vana1 = 2.8 V I_{OUT} = 150 mA V_{BAT}= [3.0; 3.3] V $t_R = t_F$ = 10 µs		2		mV
Ldrt	Transient load regulation	Vana1 = 2.8 V I_{OUT}= [1; 150] mA $t_R = t_F$ = 1 µs		20		mV

Table 20. LDO regulators - Vana 1

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vana(i) regulator in sleep mode (pdn_vana1 = 1, SLEEP ='1')						
V_{BAT}	Input power supply	Vana1 = 1.5 V/1.8 V/2.5 V	2.7	3.6	5.5	V
		Vana1 = 2.8 V	3	3.6	5.5	
V_{OUT}	Output Voltage	Vana1_sel[1:0] pads 00 01 10 11	-3 %	 1.5 1.8 2.5 2.8	+3 %	V
I_{OUT}	Output current				500	µA
$I^{(2)}_Q$	Quiescent current	I_{OUT} = 0 mA			26	µA
PSRR((1)	Power supply rejection	Vana1 = 2.8 V I_{OUT} = 0.5 mA Vpp = 0.3 V, F: [0; 20] kHz	40			dB
Lir	Line regulation	V_{BAT}: [2.7; 5.5] V			5	mV
Ldr	Load regulation	I_{OUT}: [0.1; 0.5] mA			10	mV
Lirt	Transient line regulation	Vana1 = 2.8 V I_{OUT} = 0.5 mA V_{BAT}:[3; 3.3] V $t_R = t_F$ = 10 µs		2		mV
Ldrt	Transient load regulation	Vana1 = 2.8 V I_{OUT}= [0.1; 0.5] mA $t_R = t_F$ = 1 µs		20		mV

1. Guaranteed by design
2. Quiescent current defined is the current measured on the power supply voltage dedicated to the Vana(i) with only one Vana(i) on at the same time

Vana(i) (vana(i) with i = 2 or 3)

Table 21. LDO regulator - Vana(i) with i=2 or 3

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vana3 regulator in high power mode (en_vana3 = 1, SLEEP = '0')						
V_{BAT}	Input power supply	Vana(i) = 1.8 V, 2.8 V, 3 V, 3.3 V	Max (Vana(i)_out + 0.2, Vbat_min)	3.6	5.5	V
V_{OUT}	Output voltage	Vana(i)_sel[1:0]pads 00 01 10 11	-3 %	1.8 2.8 3.0 3.3	+3 %	V
I_{OUT}(1)	Output current				150	mA
I_{SHORT}(1)	Short-circuit limitation		230	340	550	mA
I_Q(2)	Quiescent current	I_{OUT} = 0 mA			30	µA
I_{LKG}	Power-down current				1	µA
PSRR(1)	Power supply rejection	Vana(i) = 2.8 V I_{OUT} = 150 mA Vpp = 0.3 V, F: [0; 20] kHz		50		dB
		Vana(i) = 2.8 V I_{OUT} = 10 mA Vpp = 0.3 V, F: [0; 10] kHz F: [10; 100] kHz		50 45		dB
T_R	Rising time	Vana(i) = 2.8 V I_{OUT} = 10 mA		1.5		ms
Lir	Line regulation	V_{BAT}: [2.7; 5.5] V			5	mV
Ldr	Load regulation	I_{OUT}= [0.1; 150] mA			10	mV
Lirt	Transient line regulation	Vana(i) = 2.8 V I_{OUT} = 150 mA V_{BAT}= [3.0; 3.3] V $t_R = t_F$ = 10 µs		2		mV
Ldrt	Transient load regulation	Vana(i) = 2.8 V I_{OUT}= [1; 150] mA $t_R = t_F$ = 1 µs		20		mV

Table 21. LDO regulator - Vana(i) with i=2 or 3 (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vana(i) regulator in sleep mode (en_vana3 = 1, SLEEP ='1')						
V_{BAT}	Input power supply	Vana(i) = 1.8 V, 2.8 V, 3.0 V, 3.3 V	MAX (Vana(i)_out+0.2, Vbat_min)	3.6	5.5	V
V_{OUT}	Output voltage	Vana(i)_sel[1:0] pads 00 01 10 11	-3 %	1.8 2.8 3.0 3.3	+3 %	V
I_{OUT}	Output current				500	µA
$I^{(1)}_Q$	Quiescent current	I_{OUT} = 0 mA			26	µA
PSRR(1)	Power supply rejection	Vana(i) = 2.8 V I_{OUT} = 5 mA Vpp = 0.3 V, F: [0; 20] kHz	40			dB
Lir	Line regulation	V_{BAT}: [2.7; 5.5] V			5	mV
Ldr	Load regulation	I_{OUT}: [0.1; 0.5] mA			10	mV
Lirt	Transient line regulation	Vana(i) = 2.8 V I_{OUT} = 0.5 mA V_{BAT}:[3; 3.3] V $t_R = t_F$ = 10 µs		2		mV
Ldrt	Transient load regulation	Vana(i) = 2.8 V I_{OUT}= [0.1; 0.5] mA $t_R = t_F$ = 1 µs		20		mV

1. Guaranteed by design
2. Quiescent current defined is the current measured on the power supply voltage dedicated to the Vana(i) with only one Vana(i) on at the same time

Vdig

Table 22. LDO regulator - Vdig

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vdig regulator in high power mode (pdn_vdig = 1); Otherwise specified Vin = Vsdc2 (1.8 V)						
V_{IN}	Vsdc2 input power supply	Vdig = 1 V/1.2 V	-3%	1.8	+3%	V
	V_{BAT} input power supply	Vdig = 1.5 V	2.7	3.6	5.5	V
V_{OUT}	Output voltage	Vdig_sel[1:0] pads 00 01 10	-3 %	 1.0 1.2 1.5	+3 %	V
I_{OUT}(1)	Output current	Vdig: 1 V			100	mA
		Vdig: 1.2 V/1.5 V			250	mA
I_{SHORT}(1)	Short-circuit limitation		330	800		mA
I_Q(2)	Quiescent current	I_{OUT} = 0 mA			43	µA
I_{LKG}	Power-down current				1.5	µA
T_R	Rising time (10 % to 90 %)	Vdig = 1.2 V I_{OUT} = 10 mA			0.7	ms
Lir	Line regulation	V_{BAT}: [2.7; 5.5] V			10	mV
Ldr	Load regulation	I_{OUT}: [0.1; 250] mA			10	mV
Lirt	Transient line regulation	Vdig = 1.2 V I_{OUT} = 150 mA ΔV_{BAT}= 300 mV $t_R = t_F$ = 10 µs		1		mV
Ldrt	Transient load regulation	Vdig = 1.2 V I_{OUT}= [1; 250] mA $t_R = t_F$ = 1 µs		40		mV

1. Guaranteed by design
2. Quiescent current defined is the current measured on the power supply voltage dedicated to the Vdig

Vmmc

Table 23. LDO regulator - Vmmc

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VMMC regulator specifications (PDN_VMMC = 1)						
V_{BAT}	Input voltage	V_{OUT} = 3 V V_{OUT} = 2.85 V V_{OUT} = 2.5 V V_{OUT} = 1.8 V	3.25 3.1 2.75 2.7	3.6	5.5	V
V_{OUT}	Output voltage		-3%	3 2.85 2.5 1.8	+3%	V
I_{OUT}(1)	Output current				150	mA
I_{SHORT}(1)	Short circuit current limitation		240	360	600	mA
I_Q(2)	Quiescent current	I_{OUT} = 0 mA			26	µA
I_{LKG}	Power-down current				1	µA
PSRR	Power supply rejection	I_{OUT} = 150 mA Vpp = 0.3 V f < 20 kHz	40			dB
L_{IR}	Line regulation	V_{BAT}: [3.1; 5.5]V			10	mV
L_{DR}	Load regulation	I_{OUT}= [1; 150] mA			10	mV
L_{IRT}	Transient line regulation	V_{OUT}=2.85 V V_{BAT}: 3.1 to 3.4V $t_R = t_F$ = 10 µs.		2		mV
L_{DRT}	Transient load regulation	I_{OUT} = [1; 150] mA $t_R = t_F$ = 1 µs		25		mV
t_S	Settling time OFF->ON	I_{OUT} = 0 mA			100	µs
t_D	Discharge time ON>OFF	I_{OUT} = 0 mA			1	ms

1. Guaranteed by design
2. Quiescent current defined is the current measured on the power supply voltage dedicated to the Vmmc

4.2.6 Power supply monitoring

This block monitors the Vsdc1 and Vsdc2 output voltage. If Vsdc1 or Vsdc2 drops below the threshold, the processor is reset.

Table 24. Power supply monitoring

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Threshold						
T_{HCORE}	Threshold Vsdc1	Vsdc1 = 1.2 V or 1.5 V	-3%	Vsdc1-150	+3%	mV
		Vsdc1 = 1 V	-3%	Vsdc1-100	+3%	mV
T_{HVIO}	Threshold Vsdc2		-3%	1.65	+3%	V

4.3 Digital specifications

All electrical specifications having the VddIO voltage as reference will be able to sustain 1.8 V or 2.8 V ± 5 % for VddIO voltage supply.

VddIO ball could be connected to Vsdc2 at 1.8 V or to external voltage at 1.8 V or at a maximum voltage of 2.8 V ± 5 %

4.3.1 CMOS input/output static characteristics: I²C interface

Table 25. CMOS input/output static characteristics: I²C interface

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
I²C interface						
V_{IL}	Low level input voltage				0.3*VddIO	V
V_{IH}	High level input voltage		0.7*VddIO			V
I_{IL}	Low level input current		-1.0		1.0	µA
I_{IH}	High level input current		-1.0		1.0	µA
V_{OL}	Low level output voltage	IOL = 3mA (with open drain or open collector)			0.2*VddIO	
V_{OH}	High level output voltage	IOL = 3mA (with open drain or open collector)	0.8*VddIO			

4.3.2 CMOS input/output dynamic characteristics: I2C interface

Table 26. CMOS input/output dynamic characteristics: I²C interface

Symbol	Description	Min.	Typ.	Max.	Units
I²C interface (*Figure 5*)					
Fscl	Clock frequency			400	kHz
thigh	Clock pulse width high	600			ns
tlow	Clock pulse width low	1300			ns
tr	SDA, SCL, USBSDA, USBSCL rise time	20+0.1Cb(1)		300	ns
tf	SDA, SCL, USBSDA, USBSCL fall time	20+0.1Cb(1)		300	ns
thd_sta	Start condition hold time	600			ns
tsu_sta	Start condition set up time	600			ns
thd_dat	Data input hold time	0			ns
tsu_dat	Data input set up time	100			ns
tsu_sto	Stop condition set up time	600			ns
tbuf	Bus free time	1300			ns
Cb	Capacitive load for each bus line			400	pF

1. Cb = total capacitance of one bus line in pF.

4.3.3 CMOS input/output static characteristics: VddIO level

Table 27. VddIO level: Control I/Os

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Sw_resetn, VddOK, Res_pro, Pwren, Clk32k_in						
V_{IL}	Low level input voltage				0.3*VddIO	V
V_{IH}	High level input voltage		0.7*VddIO			V
I_{IL}	Low level input current		-1.0		1.5	µA
I_{IH}	High level input current		-1.0		1.5	µA
C_{IN}	Input capacitance				10	pF
V_{OL}	Low level output voltage	I_{OL} = TBD			0.2*VddIO	V
V_{OH}	High level output voltage	I_{OH} = TBD	0.8*VddIO			V
	Output fall time	Capacitance 10pF			1	ns
	Output rise time	Capacitance 10pF			1	ns
$C_{I/O}$	Driving capability				100	pF

4.3.4 CMOS input static characteristics: Vbat level

Table 28. CMOS input static characteristics: Vbat level

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Vana1_sel[0:1], Vana2_sel[0:1], Vana3_sel[0:1], Vdig_sel[0:1], Vsdc1_sel[0:1]						
V_{IL}	Low level input voltage				0.3*Vbat	V
V_{IH}	High level input voltage		0.7*Vbat			V
I_{IL}	Low level input current		-1.0		1.5	µA
I_{IH}	High Level Input Current		-1.0		1.5	µA
C_{IN}	Input capacitance				10	pF

4.3.5 NMOS input: Pon

Table 29. Pon input static characteristics

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Pon						
V_{IL}	Low level input voltage				0.5	V
V_{IH}	High level input voltage		1		Vbat	V
I_{IL}	Low level input current		-1.0		1.5	µA
I_{IH}	High Level Input Current		-1.0		1.5	µA

5 Test disclaimer

5.1 Guaranteed by design

These parameters are measured during STMicroelectronics internal qualification (voltage range, temperature, etc....) which includes full characterization on standard and corner batches of the process. These parameters are partially measured or not measured at all during production testing.

5.2 Fully tested on package only

These parameters are measured during STMicroelectronics internal qualification (voltage range, temperature, etc....) which includes full characterization on standard and corner batches of the process. These parameters are fully tested on package only and partial tests are performed on wafers.

6 Application information

6.1 Components list

Table 30. Components list

Name	Value	Comments	Function
C1	10µF	In the complete system application, the sum of the capacitors connected on each STw4510 ball must never be less than 30% of the value indicated in the typical value column of this table. This includes all capacitor parameters: – production dispersion – DC bias voltage applied – temperature range of the complete system application – aging	Vbat_Vsdc1 decoupling
C6			Vbat_Vsdc2 decoupling
C9			Vbat_ana decoupling
C2	22µF		Vsdc1 output filter
C7			Vsdc2 output filter
C4	1 µF		Vbat_osc output filter
C5			VddIO output filter
C11			Vbat_dig output filter
C13			Vbat_Vana1_Vana3 output filter
C16			Vbat_Vana2 output filter
C18			Vbat_Vmmc output filter
C10	2.2µF		Vref output filter
C12			Vdig output filter
C14			Vana3 output filter
C15			Vana1output filter
C17			Vana2 output filter
C19			Vmmc output filter
L1	4.7µH	see: *Table 31*	Coil Vsdc2 DC/DC
L2			Coil Vsdc1 DC/DC

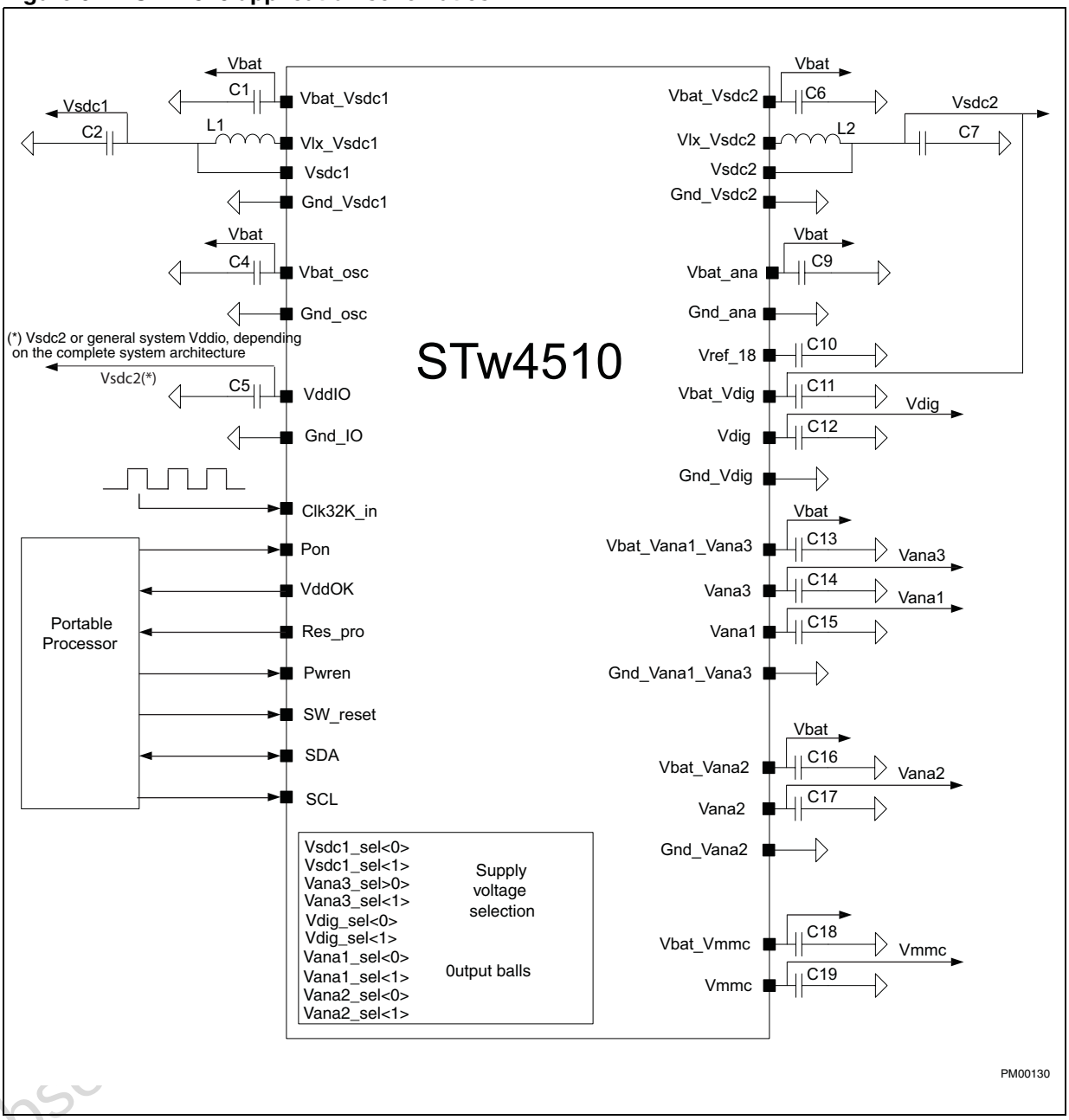
Table 31. List of 4.7 µH coils

Supplier	Part number	DCR (Ω)	Irms[1] (A)	L x l x h (mm x mm x mm)
TDK	VLF3010AT-4R7MR70	0.28	0.7	2.8 * 2.6 * 1.0
	VLF3012AT-4R7MR74	0.16	0.74	2.8 * 2.6 * 1.2
	VLF4012AT-4R7M1R1	0.14	1.1	3.7 * 3.5 * 1.2
	MLP2520S4R7L	0.11	1.1	2.5 * 2 * 0.85
MURATA	LQH2MC-2 series	0.46	0.5	2.0 * 1.6 * 0.9
	LQM31P_N4R7M00	0.3	0.7	3.2 * 1.6 * 0.85
	LQM2HP_GO series	0.11	1.1	2.5 * 2 * 0.9

1. Irms: 30% decrease of initial value

6.2 Application schematics

Figure 9. STw4510 application schematics



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

7.1 TFBGA 84 balls 6 mm x 6 mm x 1.2 mm

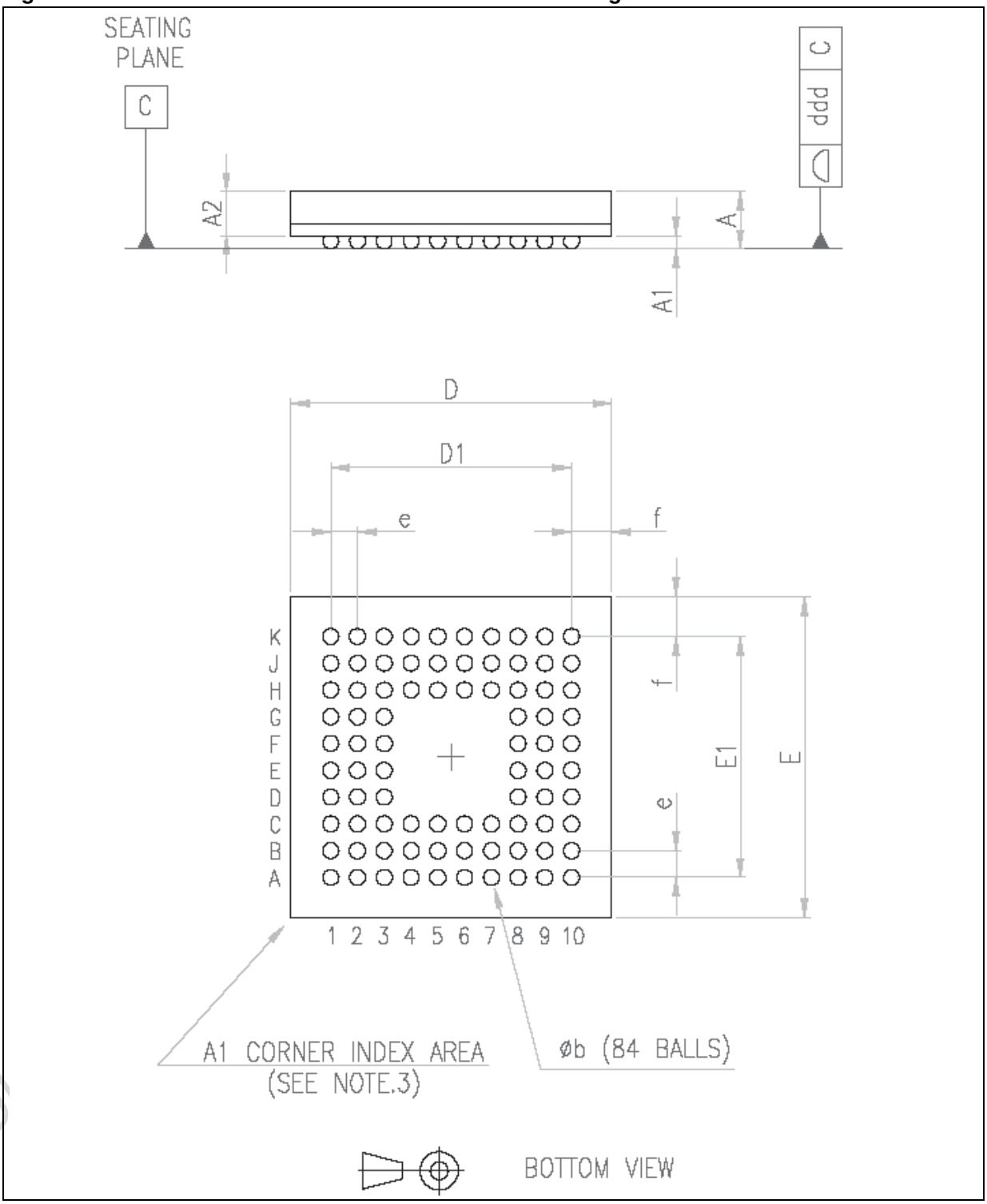
See *Figure 10: TFBGA84 6 mm x 6 mm x 1.2 mm outline drawing*.

Table 32. TFBGA84 6 mm x 6 mm x 1.2 mm - 0.5mm ball pitch (1) (2)

Parameter	Min.	Typ.	Max.	Unit
A			1.16	mm
A1	0.20	0.25	0.30	mm
A2		0.82		mm
b	0.25	0.30	0.35	mm
D	5.90	6.00	6.10	mm
D1		4.50		mm
E	5.90	6.00	6.10	mm
E1		4.50		mm
e	0.45	0.50	0.55	mm
f	0.65	0.75	0.85	mm
ddd			0.08	mm

1. These measurements conform to JEDEC standards
2. Drawing dimensions

Figure 10. TFBGA84 6 mm x 6 mm x 1.2 mm outline drawing



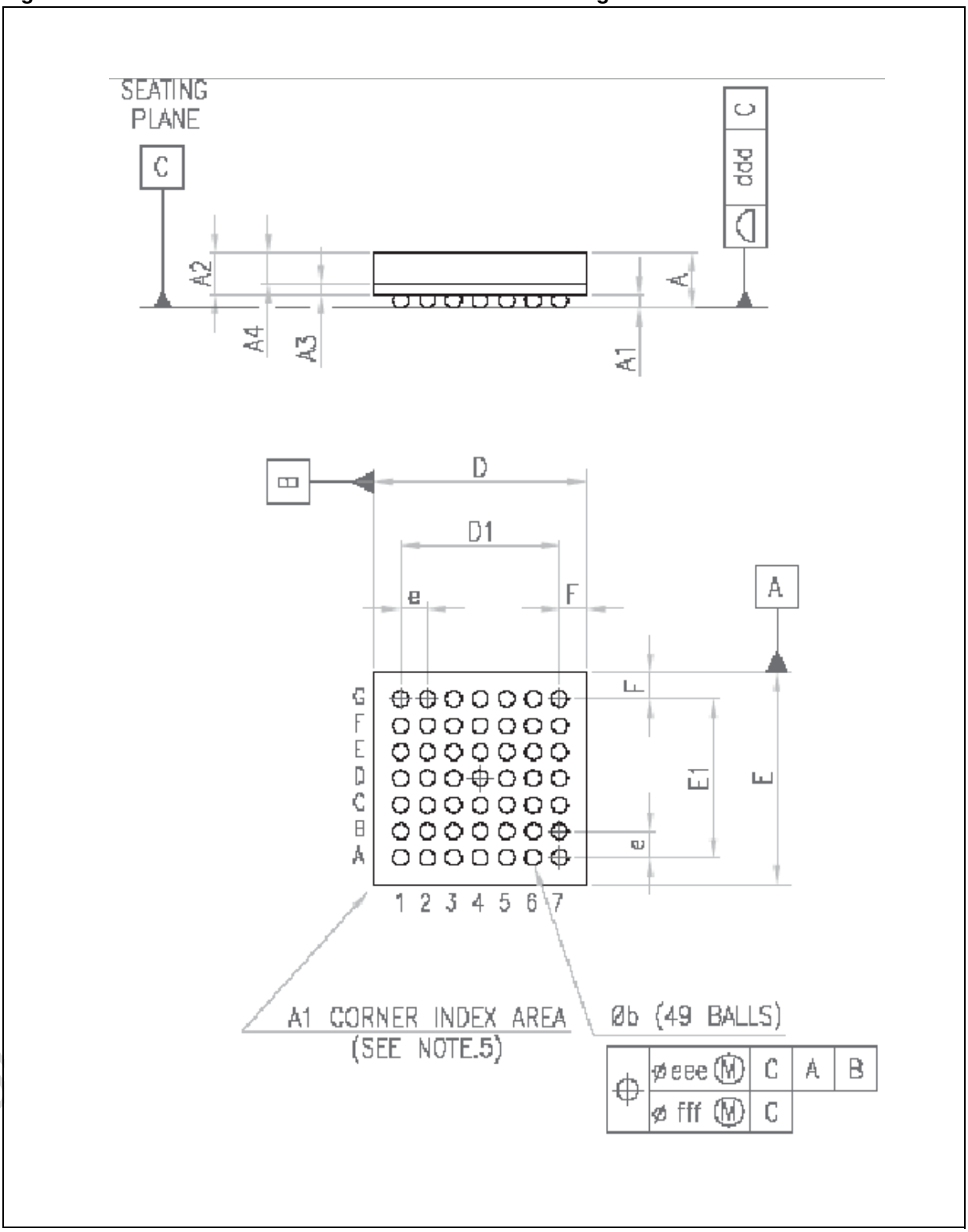
Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

7.2 TFBGA 49 balls 4 mm x 4 mm x 1.2 mm

Table 33. TFBGA49 4 mm x 4 mm x 1.2 mm, 0.5mm pitch

Reference	Min.	Typ.	Max.	Unit
A			1.2	mm
A1	0.15			mm
A2		0.8		mm
A3		0.2		mm
A4			0.6	mm
b	0.25	0.3	0.35	mm
D	3.85	4.00	4.15	mm
D1		3.00		mm
E	3.85	4.00	4.15	mm
E1		3.00		mm
e		0.50		mm
F		0.5		mm
ddd			0.08	mm
eee			0.15	mm
fff			0.05	mm

Figure 11. TFBGA49 4 mm x 4 mm x 1.2 mm outline drawing



8 Ordering information

Table 34. Order codes

Order codes	Package	Packing
STW4510AET	TFBGA84 6 mm x 6 mm x 1.2 mm	Tape and reel
STW4510AE	TFBGA84 6 mm x 6 mm x 1.2 mm	Tray
STW451027T/HF	TFBGA49 4 mm x 4 mm x 1.2 mm	Tape and reel
STW451027/HF	TFBGA49 4 mm x 4 mm x 1.2 mm	Tray

9 Revision history

Table 35. Document revision history

Date	Revision	Changes
21-Mar-2008	1	Initial release.

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