

Designer's Data Sheet

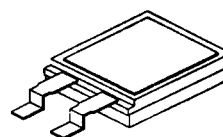
FEATURES:

- Rugged construction with poly silicon gate
- Low RDS(on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- Low inductance package
- TX, TXV and Space Level screening available
- Replaces: IRF230 Types

SFF230G

**9 AMP
200 VOLTS
0.40Ω
N-CHANNEL
POWER MOSFET**

CERPACK

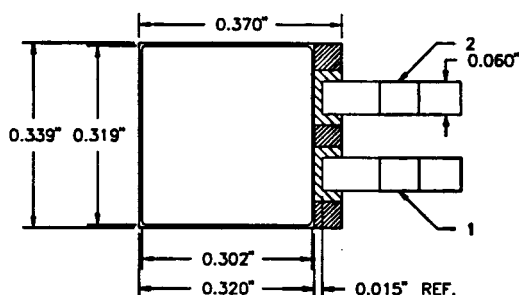
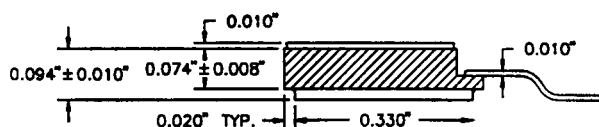


MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V _{DS}	200	Volts
Gate to Source Voltage	V _{GS}	±20	Volts
Continuous Drain Current	I _D	9	Amps
Operating and Storage Temperature	T _{op} & T _{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case	R _{θJC}	2.8	°C/W
Total Device Dissipation @ TC=25°C Total Device Dissipation @ TC=55°C	P _D	45 34	Watts

PACKAGE OUTLINE: CERPACK

PIN OUT:
PIN 1: SOURCE
PIN 2: GATE
CASE: DRAIN



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00007 B

MED

SFF230G

PRELIMINARY



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ELECTRICAL CHARACTERISTICS @ $T_J=25^\circ\text{C}$ (Unless Otherwise Specified)

RATING	SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage ($V_{GS}=0\text{ V}$, $I_D=250\mu\text{A}$)	BV_{DSS}	200	---	---	V
Drain to Source on State Resistance ($V_{GS}=10\text{ V}$, $I_D=5\text{ A}$)	$R_{DS(on)}$	---	0.25	0.4	Ω
On State Drain Current ($V_{DS}>I_D(on) \times R_{DS(on)}$ Max, $V_{GS}=10\text{ V}$)	$I_D(on)$	9	---	---	A
Gate Threshold Voltage ($V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$)	$V_{GS(th)}$	2	---	4	V
Forward Transconductance ($V_{DS}>I_D(on) \times R_{DS(on)}$ Max, $I_{DS}=5\text{ A}$)	g_{fs}	3.0	6	---	S(Ω)
Zero Gate Voltage Drain Current ($V_{DS}=\text{max rated voltage}$, $V_{GS}=0\text{ V}$) ($V_{DS}=80\%$ rated V_{DS} , $V_{GS}=0\text{ V}$, $T_A=125^\circ\text{C}$)	I_{DSS}	---	---	250 1000	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V_{GS} I_{GSS}	---	---	100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	$V_{GS}=10\text{ Volts}$ 80% rated V_{DS} $I_D=12\text{ A}$ Q_g Q_{gs} Q_{gd}	---	30 10 9	39 ---	nC
Turn on Delay Time Rise Time Turn Off Delay Time Fall Time	$V_{DD}=50\%$ rated V_{DS} 50% rated I_D $R_G=15\Omega$ $t_d(on)$ t_r $t_d(off)$ t_f	---	---	30 50 50 40	nsec
Diode Forward Voltage ($I_S=\text{rated } I_D$, $V_{GS}=0\text{ V}$, $T_J=25^\circ\text{C}$)	V_{SD}	---	---	2.0	V
Diode Reverse Recovery Time Reverse Recovery Charge	$T_J=150^\circ\text{C}$ $I_F=\text{rated } I_D$ $di/dt=100\text{ A}/\mu\text{sec}$ t_{rr} Q_{RR}	---	450 3.0	---	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{GS}=0\text{ Volts}$ $V_{DS}=25\text{ Volts}$ $f=1\text{ MHz}$ C_{iss} C_{oss} C_{rss}	---	600 250 80	800 450 150	pF

SAFE OPERATING AREA (S.O.A.)
 $T_C=25^\circ\text{C}$, D.C. CONDITION