Si535/536

REVISION D

ULTRA LOW JITTER CRYSTAL OSCILLATOR (XO)

Features

- Available with select frequencies from 100 MHz to 312.5 MHz
- 3rd generation DSPLL® with superior jitter performance and high-power supply noise rejection
- 3x better frequency stability than SAW-based oscillators
- Available with LVPECL and LVDS outputs
- 3.3 and 2.5 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

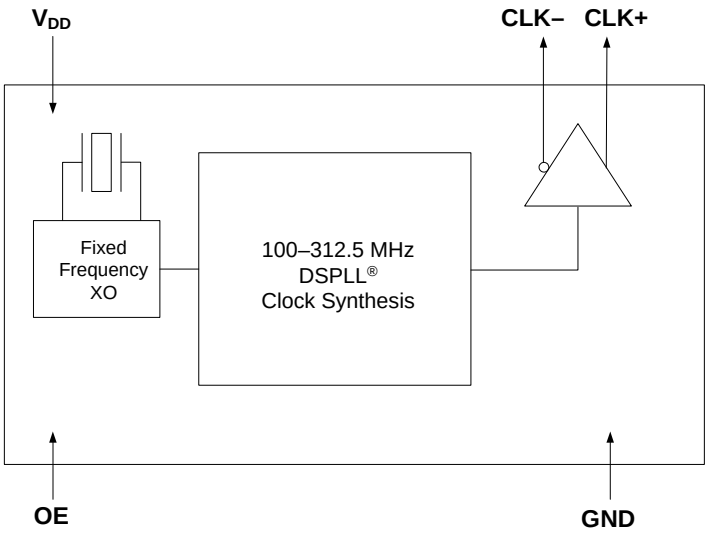
Applications

- 10/40/100G data centers
- 10G Ethernet switches/routers
- Fibre channel/SAS/storage
- Enterprise servers
- Networking
- Telecommunications

Description

The Si535/536 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide an ultra low jitter clock at high-speed differential frequencies. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si535/536 uses one fixed crystal to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si535/536 IC based XO is factory programmed at time of shipment, thereby eliminating long lead times associated with custom oscillators.

Functional Block Diagram



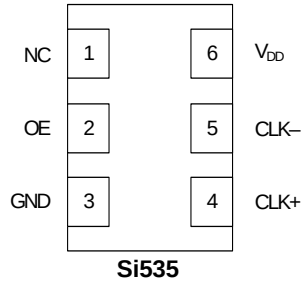
Ordering Information:

See page 7.

Pin Assignments:

See page 6.

(Top View)



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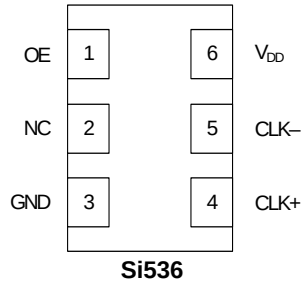

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
Supply Current	I_{DD}	Output enabled LVPECL LVDS	 — —	 111 90	 121 98	mA
		Tristate mode	—	60	75	mA
Output Enable (OE)[2]		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	V
Operating Temperature Range	T_A		–40	—	85	°C

Notes:
1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 7 for further details.
2. OE pin includes a 17 kΩ pullup resistor to V_{DD}.

Table 2. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Frequency[1]	f_O	LVPECL/LVDS	100	—	312.5	MHz
Initial Accuracy	f_i	Measured at +25 °C at time of shipping	—	±1.5	—	ppm
Temperature Stability[1,2]			–7 –20	— —	+7 +20	ppm
Aging	f_a	Frequency drift over first year	—	—	±3	ppm
		Frequency drift over 20 year life	—	—	±10	ppm
Total Stability[2]		Temp stability = ±20 ppm	—	—	±31.5	ppm
		Temp stability = ±7 ppm	—	—	20	
Powerup Time[3]	t_{OSC}		—	—	10	ms

Notes:
1. See Section 3. "Ordering Information" on page 7 for the list of available frequencies.
2. Selectable parameter specified by part number.
3. Time from powerup or tristate mode to f_O.

Table 3. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVPECL Output Option[1]	V_O	Mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	Swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	Swing (Single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	Mid-level	1.125	1.20	1.275	V
	V_{OD}	Swing (diff)	0.5	0.7	0.9	V_{PP}
Rise/Fall time (20/80%)	t_R, t_F		—	—	350	ps
Symmetry (duty cycle)	SYM	Differential	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).

Table 4. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVPECL/LVDS Phase Jitter* (RMS)	ϕ_J	10 kHz to 1 MHz (data center)	—	0.19	—	ps
		12 kHz to 20 MHz (OC-48)	—	0.25	—	ps
***Note:** Applies to output frequencies: 156.25 MHz.						

Table 5. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVPECL/LVDS Period Jitter*	J_{PER}	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	ps
***Note:** N = 1000 cycles.						

Figure 1. Si535/536 Typical Phase Noise at 156.25 MHz

Table 6. Environmental Compliance

The Si535/536 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross & Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	J-STD-020, MSL1
Contact Pads	Gold over Nickel

Table 7. Thermal Characteristics

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	84.6	—	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	38.8	—	°C/W
Ambient Temperature	T_A		–40	—	85	°C
Junction Temperature	T_J		—	—	125	°C

Table 8. Absolute Maximum Ratings[1]

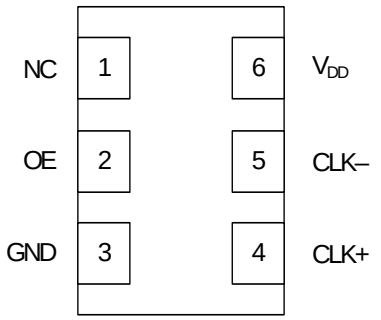
Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	T_{AMAX}	85	°C
Supply Voltage, 2.5/3.3 V Option	V_{DD}	–0.5 to +3.8	V
Input Voltage (any input pin)	V_I	–0.5 to V_{DD} + 0.3	V
Storage Temperature	T_S	–55 to +125	°C
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	°C
Soldering Temperature Time @ T_{PEAK} (Pb-free profile)[2]	t_P	20–40	seconds

Notes:

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at www.silabs.com/VCXO for further information, including soldering profiles.

2. Pin Descriptions

(Top View)



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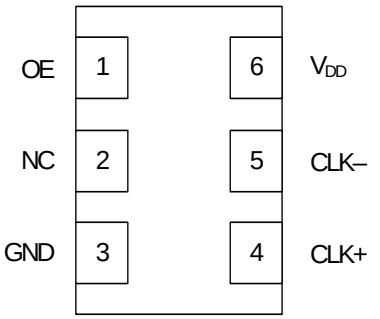

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Table 9. Pinout for Si535 Series

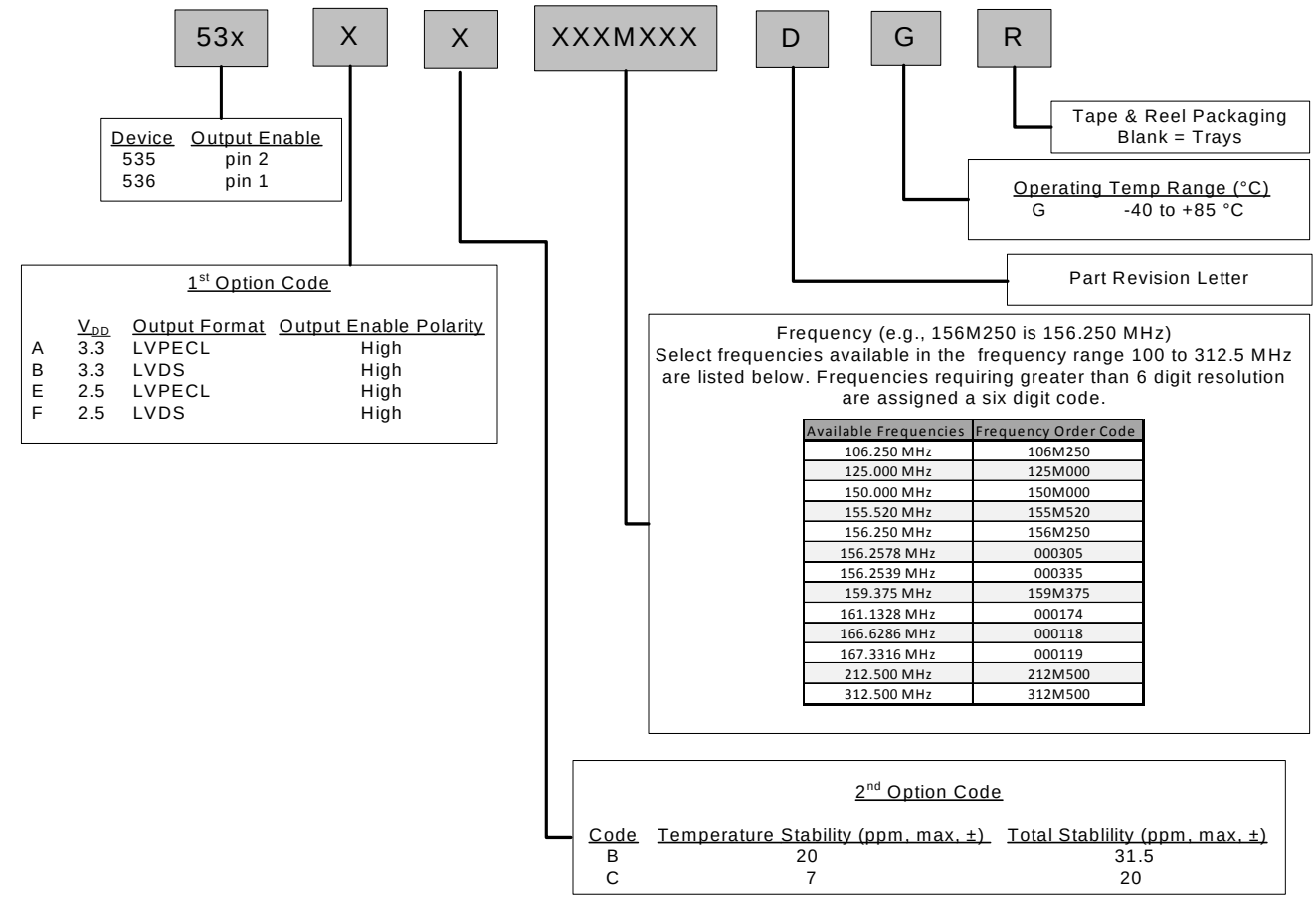
Pin	Symbol	Function
1	NC	No connection
2	OE	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled
3	GND	Electrical and Case Ground
4	CLK+	Oscillator Output
5	CLK–	Complementary Output
6	V_{DD}	Power Supply Voltage
***Note:** OE includes a 17 kΩ pullup resistor to V_{DD}.		

Table 10. Pinout for Si536 Series

Pin	Symbol	Function
1	OE	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled
2	No connection	No connection
3	GND	Electrical and Case Ground
4	CLK+	Oscillator Output
5	CLK–	Complementary output
6	V_{DD}	Power Supply Voltage
***Note:** OE includes a 17 kΩ pullup resistor to V_{DD}.		

3. Ordering Information

The Si535/536 XO supports a variety of options including frequency, temperature stability, output format, and V_{DD}. The Si535 and Si536 XO series are supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm package. The Si536 Series supports an alternate OE pinout (pin #1) for the LVPECL and LVDS output formats. See Tables 9 and 10 for the pinout differences between the Si535 and Si536 series.



Example P/N: 535AB156M250DGR is a 5 x 7 XO in a 6 pad package. The frequency is 156.250 MHz, with a 3.3 V supply, LVPECL output, and Output Enable active high polarity. Temperature stability is specifed as ±20 ppm. The part is specified for –40 to +85 °C ambient temperature range operation and is shipped in tape and reel format.

Figure 2. Part Number Convention

4. Package Outline

Figure 3 illustrates the package details for the Si535/536. Table 11 lists the values for the dimensions shown in the illustration.

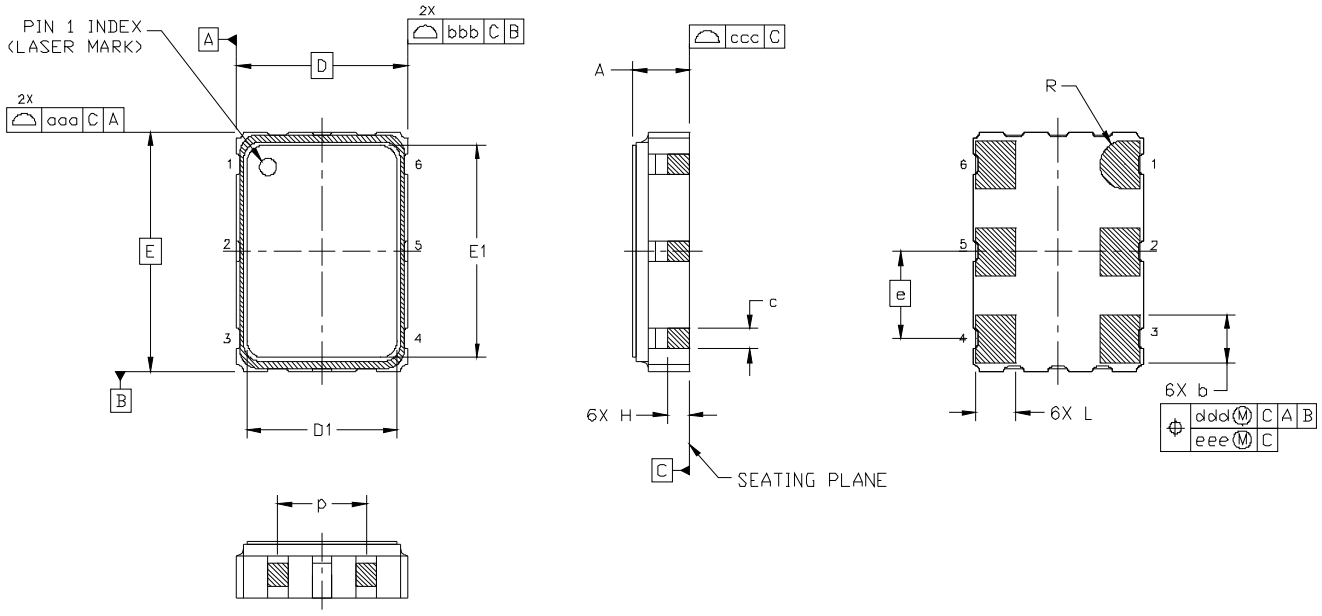


Figure 3. Si535/536 Outline Diagram

Table 11. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D		5.00 BSC	
D1	4.30	4.40	4.50
e		2.54 BSC	
E		7.00 BSC	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
p	1.80	—	2.60
R		0.70 REF	
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.05	

5. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the Si535/536. Table 12 lists the values for the dimensions shown in the illustration.

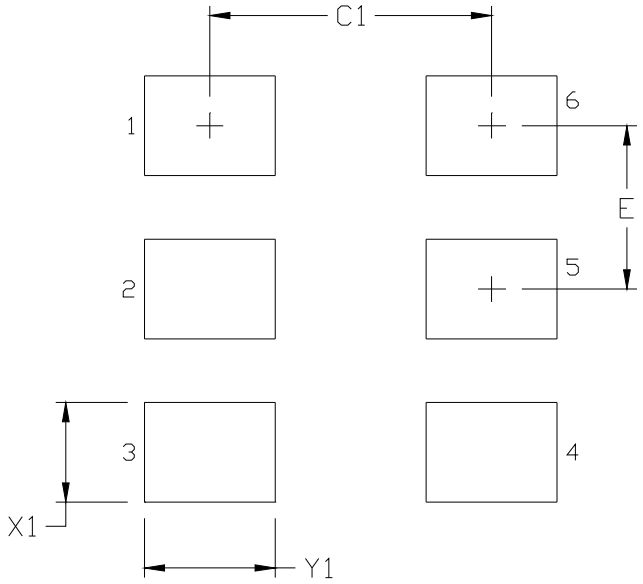


Figure 4. Si535/536 PCB Land Pattern

Table 12. PCB Land Pattern Dimensions (mm)

Dimension	Min
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

6. Si535/Si536 Mark Specification

Figure 5 illustrates the mark specification for the Si535/Si536. Table 13 lists the line information.

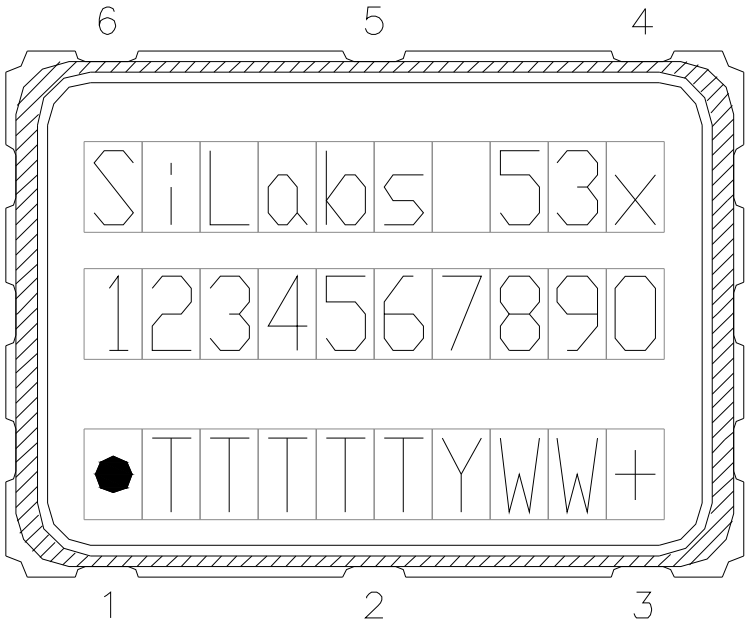


Figure 5. Mark Specification

Table 13. Si53x Top Mark Description

Line	Position	Description
1	1–10	"SiLabs"+ Part Family Number, 53x (First 3 characters in part number where x = 5 indicates a 535 device and x = 6 indicates a 536 device).
2	1–10	Si535, Si536: Option1 + Option2 + Freq(7) + Temp Si535/Si536 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6) + Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2013 = 3)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	"+" to indicate Pb-Free and RoHS-compliant

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Updated Table 7 on page 5.

Revision 0.3 to Revision 0.5

- Updated Note 1 in Table 2 on page 2.
- Updated Symmetry Test Condition in Table 3 on page 3.
- Updated Table 4 on page 4.
- Updated Table 5 on page 4.
- Updated XXXMXXX text in Figure 2 on page 7.
- Updated 4. "Package Outline" on page 8.

Revision 0.5 to Revision 0.6

- Updated Figure 2 on page 7.
- Updated Land Pattern information on page 10.

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