

Low Vcesat NPN Epitaxial Planar Transistor

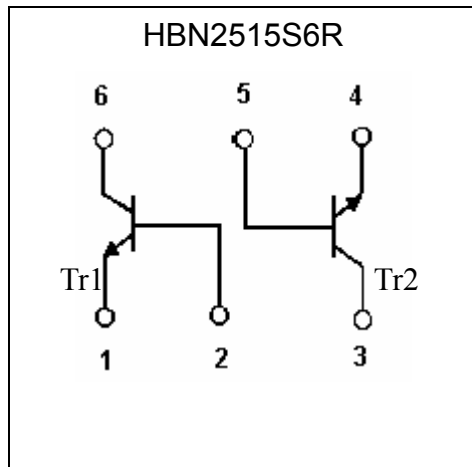
HBN2515S6R

(Dual Transistors)

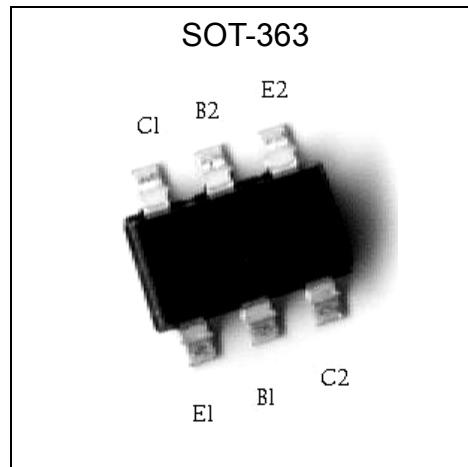
Features

- Two BTD2515 chips in a SOT-363 package.
- Mounting possible with SOT-323 automatic mounting machines.
- Transistor elements are independent, eliminating interference.
- Mounting cost and area can be cut in half.
- Low $V_{CE(sat)}$, $V_{CE(sat)}=25mV$ (max), at $I_C / I_B = 10mA / 0.5mA$.
- Weight : 9.1mg, approximately.
- Pb-free package.

Equivalent Circuit



Outline



The following characteristics apply to both Tr1 and Tr2

Absolute Maximum Ratings ($T_a=25^{\circ}C$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	20	V
Collector-Emitter Voltage	V_{CEO}	15	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current (DC)	I_C	800	mA
Collector Current (Pulse)	I_{CP}	1.5 (Note 1)	A
Power Dissipation	P_d	200 (total) (Note 2)	mW
Junction Temperature	T_j	150	$^{\circ}C$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}C$

Note : 1.Single pulse, $P_w=10ms$
 2.150mW per element must not be exceeded.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	20	-	-	V	I _C =100μA, I _E =0
BV _{CEO}	15	-	-	V	I _C =2mA, I _B =0
BV _{EBO}	6	-	-	V	I _E =100μA, I _C =0
I _{CBO}	-	-	100	nA	V _{CB} =15V, I _E =0
I _{EBO}	-	-	100	nA	V _{EB} =6V, I _C =0
*V _{CE(sat)1}	-	-	25	mV	I _C =10mA, I _B =0.5mA
*V _{CE(sat)2}	-	-	150	mV	I _C =200mA, I _B =10mA
*V _{CE(sat)3}	-	-	250	mV	I _C =500mA, I _B =50mA
*R _{CE(sat)}	-	-	500	mΩ	I _C =500mA, I _B =50mA
*V _{BE(sat)}	-	-	1.1	V	I _C =500mA, I _B =50mA
*V _{BE(on)}	-	-	0.9	V	V _{CE} =2V, I _C =100mA
*h _{FE1}	160	-	-	-	V _{CE} =1V, I _C =10mA
*h _{FE2}	180	-	560	-	V _{CE} =1V, I _C =100mA
*h _{FE3}	150	-	-	-	V _{CE} =1V, I _C =500mA
f _T	100	300	-	MHz	V _{CE} =10V, I _C =50mA, f=100MHz
Cob	-	6.5	-	pF	V _{CB} =10V, f=1MHz

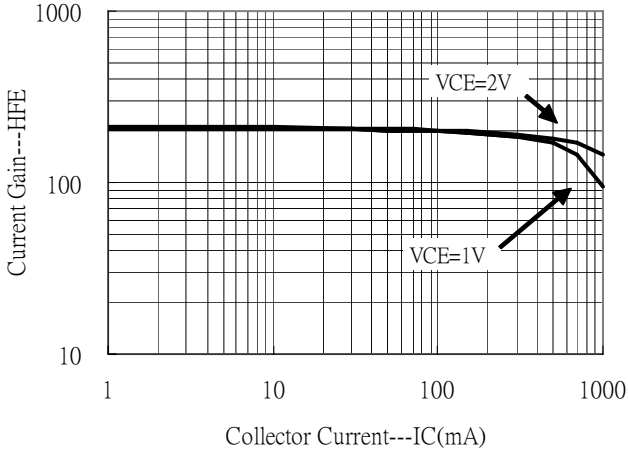
*Pulse Test : Pulse Width ≤380μs, Duty Cycle ≤2%

Ordering Information

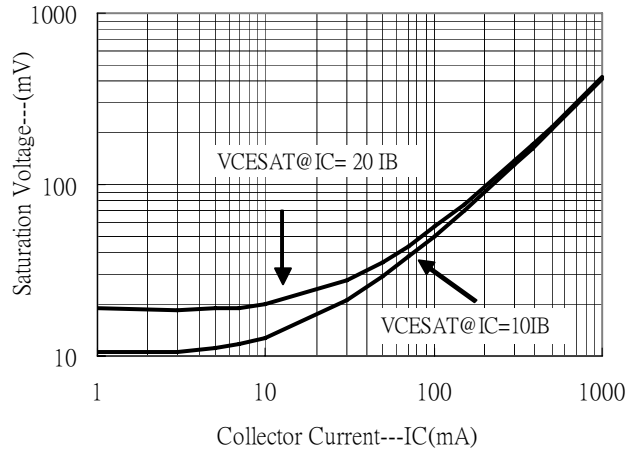
Device	Package	Shipping	Marking
HBN2515S6R	SOT-363 (Pb-free)	3000 pcs / Tape & Reel	BS

Characteristic Curves

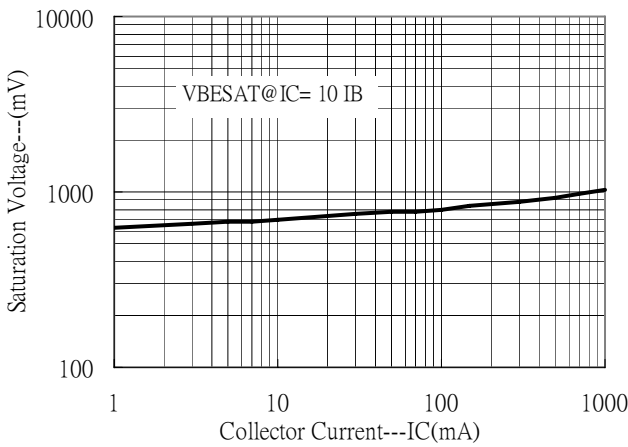
Current Gain vs Collector Current



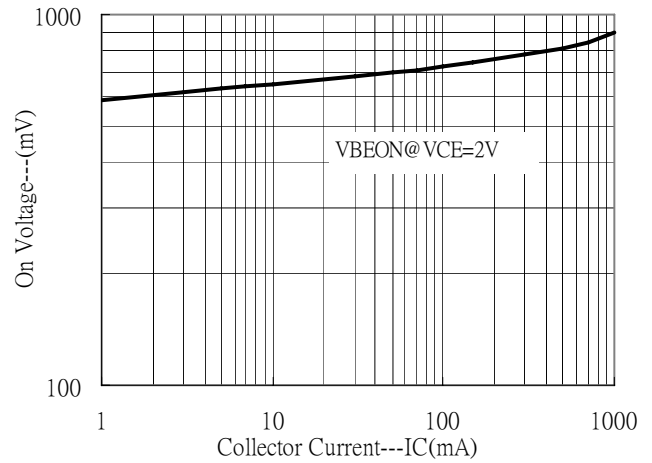
Saturation Voltage vs Collector Current



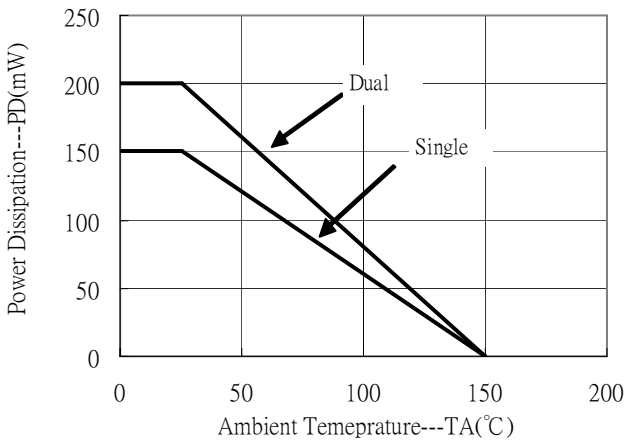
Saturation Voltage vs Collector Current



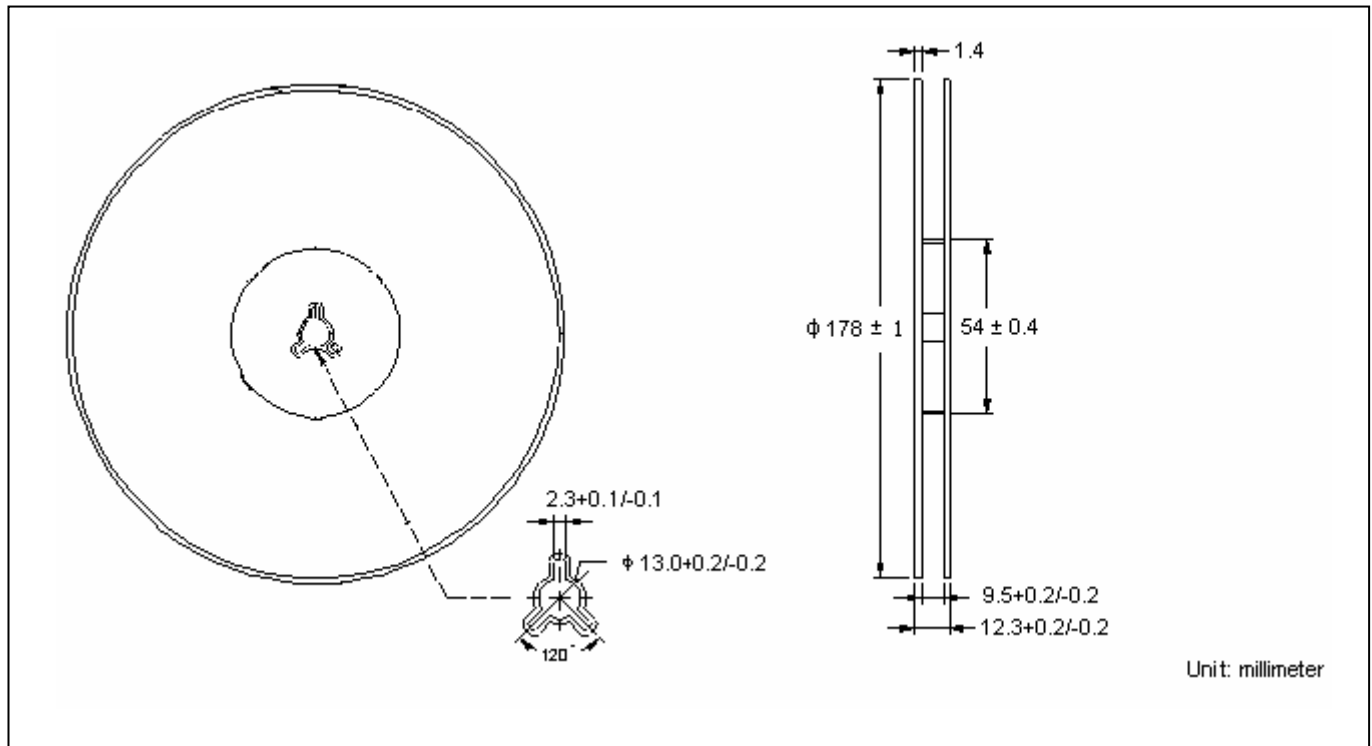
On Voltage vs Collector Current



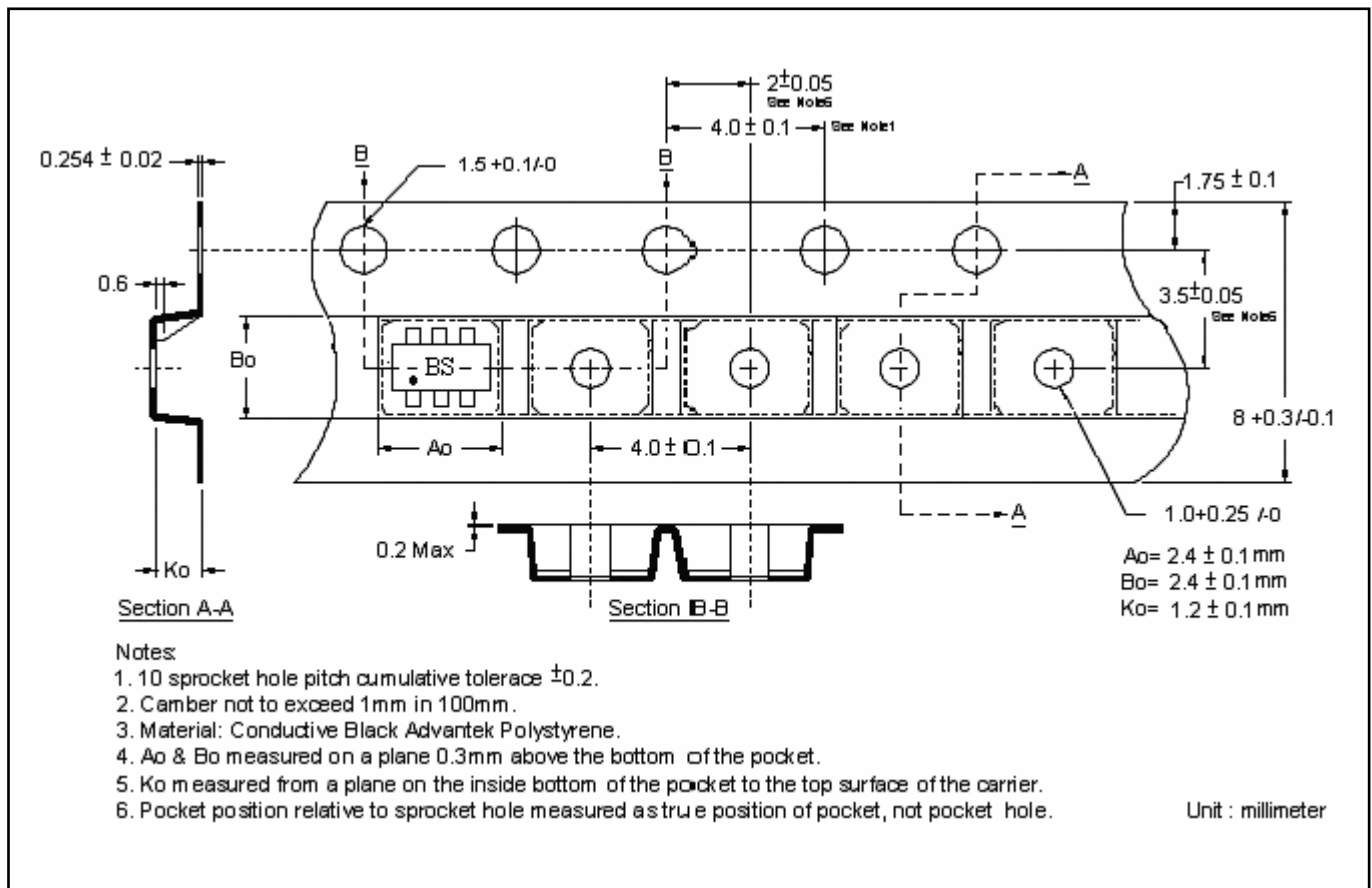
Power Derating Curve



Reel Dimension



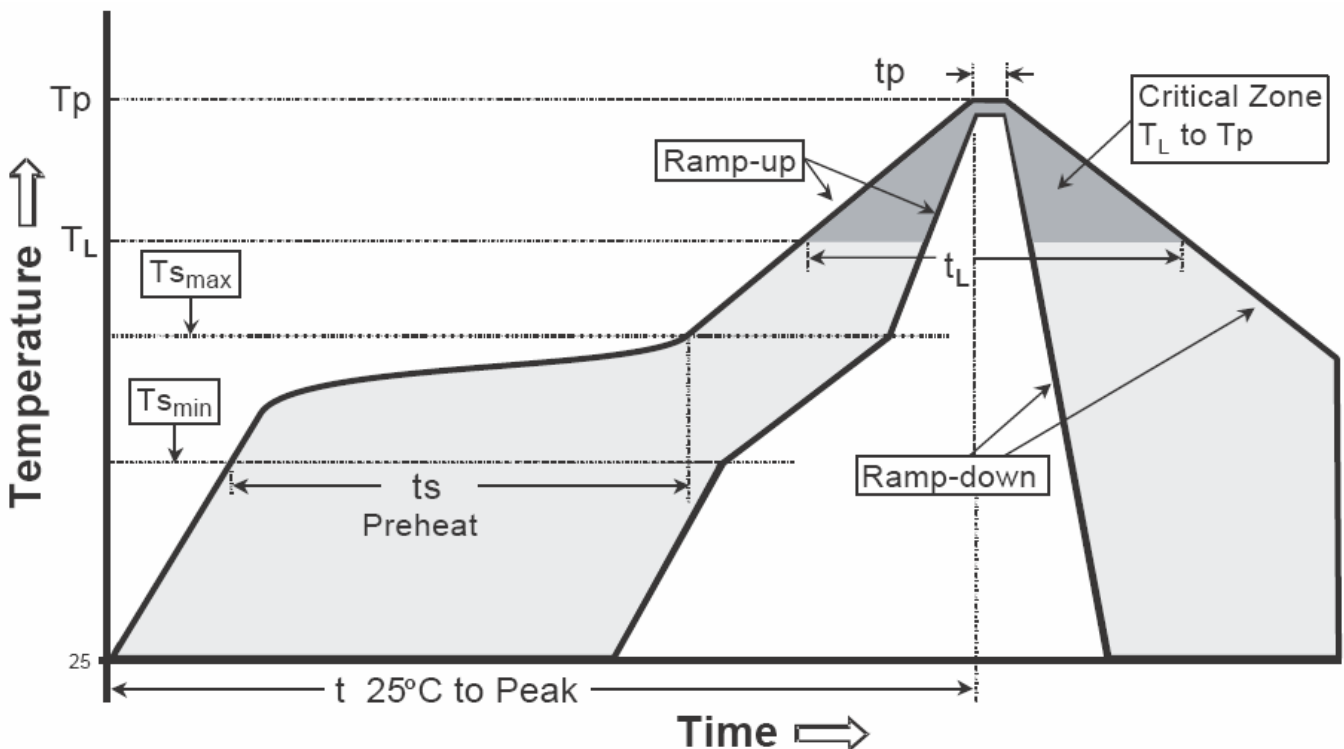
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

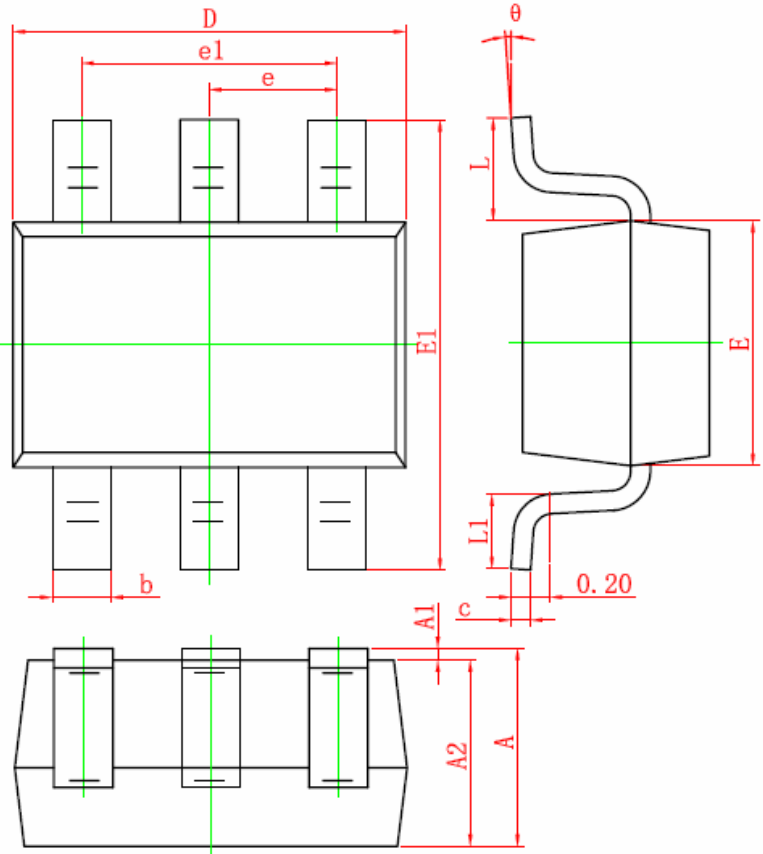
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

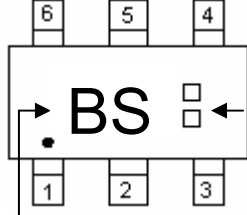
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



The diagram shows three views of the SOT-363R package: a top view, a side view, and a bottom view. Dimensions are labeled with letters and numbers: D (total width), e1 (lead pitch), e (lead width), E1 (package height), E (package height), L (lead length), L1 (lead thickness), A1 (lead height), c (lead thickness), A2 (package height), and A (package height). A lead thickness of 0.20 is also indicated.

Marking:



Date Code:
 Year + Month
 Year : 6→2006,
 7→2007, ..., etc
 Month : 1→Jan
 2→Feb, ..., 9→
 Sep, A→Oct, B
 →Nov, C→Dec

Device Code

6-Lead SOT-363R Plastic Surface Mounted Package
 CYStek Package Code: S6R

Style:
 Pin 1. Emitter1 (E1)
 Pin 2. Base1 (B1)
 Pin 3. Collector2 (C2)
 Pin 4. Emitter2 (E2)
 Pin 5. Base2 (B2)
 Pin 6. Collector1 (C1)

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650	TYP	0.026	TYP
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.150	0.350	0.006	0.014	L	0.525	REF	0.021	REF
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes : 1. Controlling dimension : millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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