September 1993
Edition 2.0

FUJITSU

DATA SHEET

MB85323A-60/-70/-80

CMOS 1M x 36 Fast Page Mode DRAM Module

CMOS 1,024,576 x 32 Bit Fast Page Mode DRAM Module

The Fujitsu MB85323-A is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of eight MB814400A devices and four MB81C1000A devices. The MB85323A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85323A are the same as the MB814400A which features fast page mode operation. For ease of memory expansion, the MB85323-A is offered on a 72-pad Single In-Line Memory Module package (SIMM).

PRELIMINARY

See page 6
MSS-72P-P37
See page 7
MSS-72P-P57

PRODUCT LINE AND FEATURES

Parameter	MB85323A-60	MB85323A-70	MB85323A-80
$\overline{RAS}$ Access Time	60ns max.	70ns max.	80ns. max
Random Cycle Time	110ns min.	125ns min.	140ns min.
Address Access Time	30ns max.	35ns max.	40ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	20ns max.
Fast Page Mode Cycle Time	40ns max.	45ns max.	45ns max.
Power Dissipation	6468mW max.	5896mW max.	5324mW max.
• Operating mode • Standby mode	132mW max. (TTL level) /66mW max. (CMOS level)		

- Organization: 1,024,576 word x 32 bit
- Memory: MB814400A, 8 pcs.
  MB81C1000A, 4 pcs.
- Decoupler Capacitor: 0.22 µF, 8 pcs.
- Package and Ordering Information: 72-pad SIMM, order as
  MB85323A-xxPJPBK
  (PJPBK = Gold Pad) or
  MB85323A-xxPJPB
  (PJPB = Gold Solder Pad)

DQ0	2	1	VSS
DQ1	4	3	DQ18
DQ2	6	5	DQ19
DQ3	8	7	DQ20
VCC	10	9	DQ21
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
DQ4	20	19	NC
DQ5	22	21	DQ22
DQ6	24	23	DQ23
DQ7	26	25	DQ24
A7	28	27	DQ25
VCC	30	29	NC
A9	32	31	A8
$\overline{RAS2}$	34	33	NC
DQ8	36	35	DQ26
DQ35	38	37	DQ17
$\overline{CAS0}$	40	39	VSS
$\overline{CAS3}$	42	41	$\overline{CAS2}$
$\overline{RAS0}$	44	43	$\overline{CAS1}$
NC	46	45	NC
NC	48	47	$\overline{WE}$
DQ27	50	49	DQ9
DQ28	52	51	DQ10
DQ29	54	53	DQ11
DQ30	56	55	DQ12
DQ31	58	57	DQ13
DQ32	60	59	VCC
DQ33	62	61	DQ14
DQ34	64	63	DQ15
NC	66	65	DQ16
PD2	68	67	PD1
PD4	70	69	PD3
VSS	72	71	NC

PIN	SYMBOL	-60	-70	-80
67	PD1	VSS	VSS	VSS
68	PD2	VSS	VSS	VSS
69	PD3	NC	VSS	NC
70	PD4	NC	NC	VSS

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1.0 to +7.0	V
Input Voltage	V_{IN}	−1.0 to +7.0	V
Output Voltage	V_{OUT}	−1.0 to +7.0	V
Short Circuit Output Current	I_{OUT}	5.0	mA
Power Dissipation	PD	8.0	W
Storage Temperature	T_{STG}	−5.5 to +125	°C

Note: Permanentdevice damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

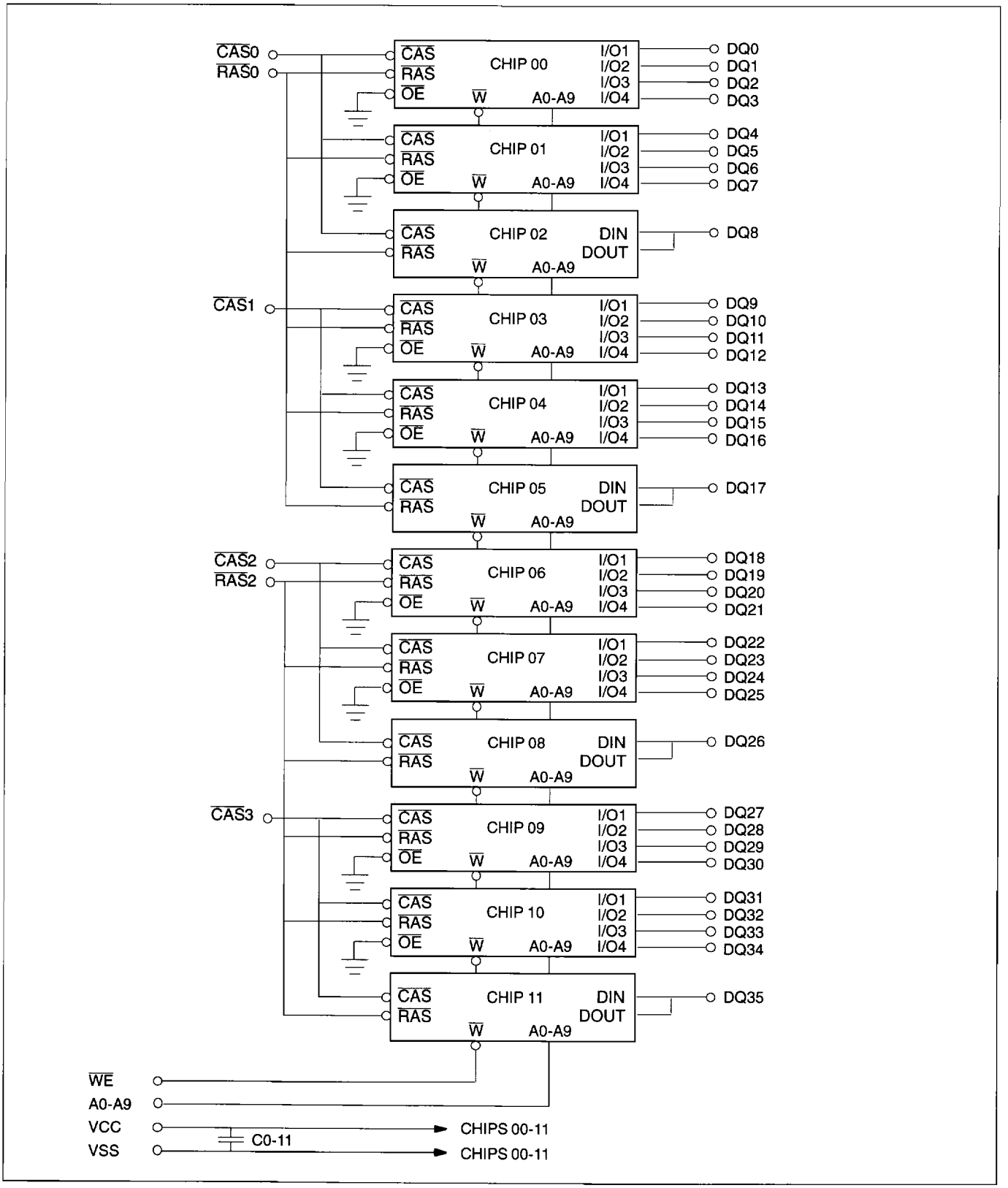


Figure 1. Function Block Library

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage		V_{OH}	I_{OH} = –5mA	2.4	—	—	V
Output Low Voltage		V_{OL}	I_{OL} = –4.2mA	—	—	0.4	V
Input Leakage Current	$\overline{RAS}$	$I_{I(L)}$	0V ≤ V_{IN} ≤ 5.5 V 4.5V ≤ V_{CC} ≤ 5.5V V_{SS} = 0V; all other pins not under test = 0V	–40	—	30	µA
	$\overline{CAS}$			–30	—	20	
	ADD, WE			–80	—	60	
Output Leakage		$I_{O(L)}$	0V ≤ V_{OUT} ≤ 5.5V Data out disabled	–20	—	20	µA
Operating Current (Average power supply current) [1]	MB85323A-60	I_{CC1}	RAS & CAS cycling; tRC = min.	—	—	1176	mA
	MB85323A-70					1072	
	MB85323A-80					968	
Standby Current (Power supply current)	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	24	mA
	CMOS		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			12	
Refresh Current #1 (Average power supply current) [1]	MB85323A-60	I_{CC3}	$\overline{CAS}$ = V_{IH}; $\overline{RAS}$ = cycling; tRC = min.	—	—	1176	mA
	MB85323A-70					1072	
	MB85323A-80					968	
Fast Page Mode Current [1]	MB85323A-60	I_{CC4}	RAS = V_{IL}; $\overline{CAS}$ = cycling; tPC = min.	—	—	684	mA
	MB85323A-70					624	
	MB85323A-80					584	
Refresh Current #2 (Average power supply current) [1]	MB85323A-60	I_{CC5}	RAS = cycling; $\overline{CAS}$-before-$\overline{RAS}$ tRC = min.	—	—	1016	mA
	MB85323A-70					912	
	MB85323A-80					808	

Note: 1. I_{CC} depends on the output load conditions and cycles rate; the specified values are obtained with the output open.
2. I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} >–0.5V.
3. I_{CC1}, I_{CC3} and I_{CC5} are specified at three time address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
4. I_{CC4} is specified at one time of address change during one Page cycle.

CAPACITANCE (T_A = 25°C, F = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	60	pF
Input Capacitance, $\overline{RAS}$0 and $\overline{RAS}$2	C_{IN2}	—	34	pF
Input Capacitance, $\overline{CAS}$0 and $\overline{CAS}$3	C_{IN3}	—	19	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	51	pF
I/O Capacitance, (DQ0-7, DQ9-16, DQ18-25, DQ27-34)	C_{DQ1}	—	10	pF
I/O Capacitance, (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	13	pF

AC CHARACTERISTICS

(At recommended operating conditions unless other noted) [3, 4, 5]

No.	Parameter	Symbol	MB85323A-60		MB85323A-70		MB85323A-80		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	Time Between Refresh [17]	t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time	t_{RC}	110	—	125	—	140	—	ns
3	Access Time from $\overline{RAS}$ [4, 7]	t_{RAC}	—	60	—	70	—	80	ns
4	Access Time from $\overline{CAS}$ [5, 7]	t_{CAC}	—	15	—	20	—	20	ns
5	Column Address Access Time [6, 7]	t_{AA}	—	30	—	35	—	40	ns
6	Output Hold Time	t_{OH}	0	—	0	—	0	—	ns
7	Output Buffer Turn On Delay Time	t_{ON}	0	—	0	—	0	—	ns
8	Output Buffer Turn Off Delay Time [8]	t_{OFF}	—	15	—	15	—	20	ns
9	Transition Time	t_T	2	50	2	50	2	50	ns
10	$\overline{RAS}$ Precharge Time	t_{RP}	40	—	45	—	50	—	ns
11	$\overline{RAS}$ Pulse Width	t_{RAS}	60	100000	70	100000	80	100000	ns
12	$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	ns
13	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	ns
14	$\overline{RAS}$ to $\overline{CAS}$ Delay Time [9, 10]	t_{RCD}	20	45	20	50	20	60	ns
15	$\overline{CAS}$ Pulse Width	t_{CAS}	15	—	20	—	20	—	ns
16	$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	ns
17	$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh) [15]	t_{CPN}	10	—	10	—	10	—	ns
18	Row Address Set Up Time	t_{ASR}	0	—	0	—	0	—	ns
19	Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns
20	Column Address Set Up Time	t_{ASC}	0	—	0	—	0	—	ns
21	Column Address Hold Time	t_{CAH}	12	—	12	—	15	—	ns
22	$\overline{RAS}$ to Column Address Delay Time [11]	t_{RAD}	15	30	15	35	15	40	ns
23	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	ns
24	Column Address to $\overline{CAS}$ Read Time	t_{CAL}	30	—	35	—	40	—	ns
25	Read Command Set Up Time	t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$ [12]	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$ [12]	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time [13]	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time	t_{WCH}	10	—	10	—	12	—	ns
30	$\overline{WE}$ Pulse Width	t_{WP}	10	—	10	—	12	—	ns
31	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	ns
32	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	ns
33	DIN Set Up Time	t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time	t_{DH}	10	—	10	—	12	—	ns
35	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycle)	t_{RPC}	0	—	0	—	0	—	ns

AC CHARACTERISTICS

(At recommended operating conditions unless other noted) [3, 4, 5]

No.	Parameter	Symbol	MB85323A-60		MB85323A-70		MB85323A-80		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
36	$\overline{CAS}$ Set Up Time for ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	t_{CSR}	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	10	—	10	—	12	—	ns
38	$\overline{WE}$ Set Up Time from $\overline{RAS}$ [16]	t_{WSR}	0	—	0	—	0	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$ [16]	t_{WHR}	10	—	10	—	10	—	ns
40	DIN to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns
41	Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASF}	—	100000	—	100000	—	100000	ns
42	Fast Page Mode Read/Write Cycle Time	t_{PC}	40	—	45	—	45	—	ns
43	Access Time from $\overline{CAS}$ Precharge [7, 14]	t_{CPA}	—	35	—	40	—	40	ns
44	Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns
45	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	40	—	ns

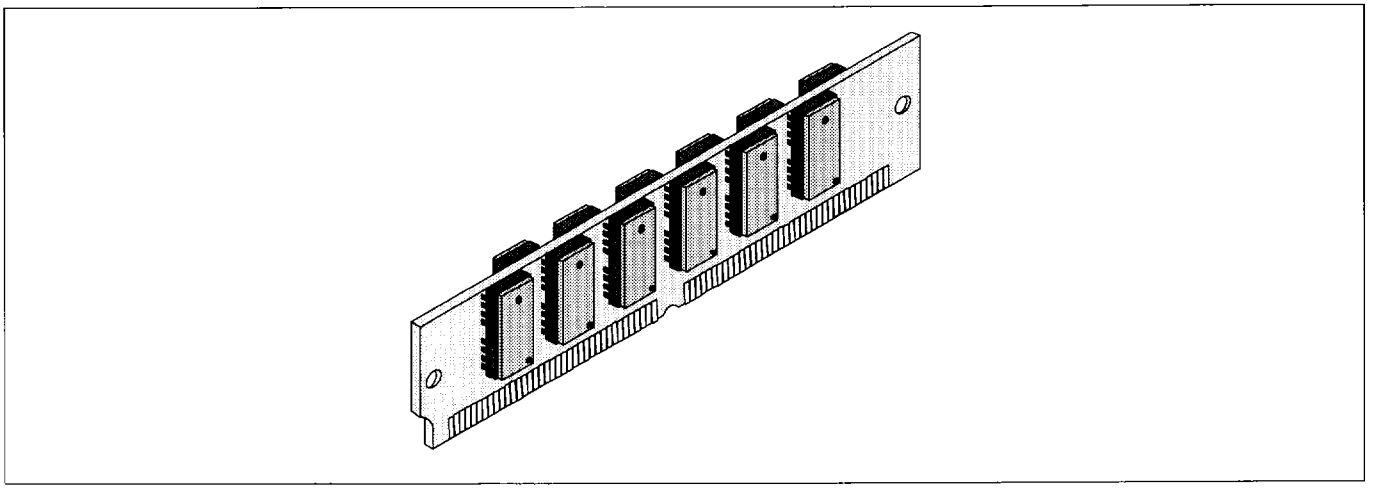
Notes:

1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200µs is required after power–up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greaterthan the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAD} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ABO} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100pF.
8. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} is specified as a reference point only; is t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} of t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greaterthan the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
14. t_{CPA} is access time form the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
15. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
16. Assumes that test mode function for non-parity bit..
17. t_{REF} is for distributed refresh (1024 refresh cycles/16.4 ms). For burst refresh, t_{REF} = 8.2 ms (1024 refresh cycles/8.2 ms).

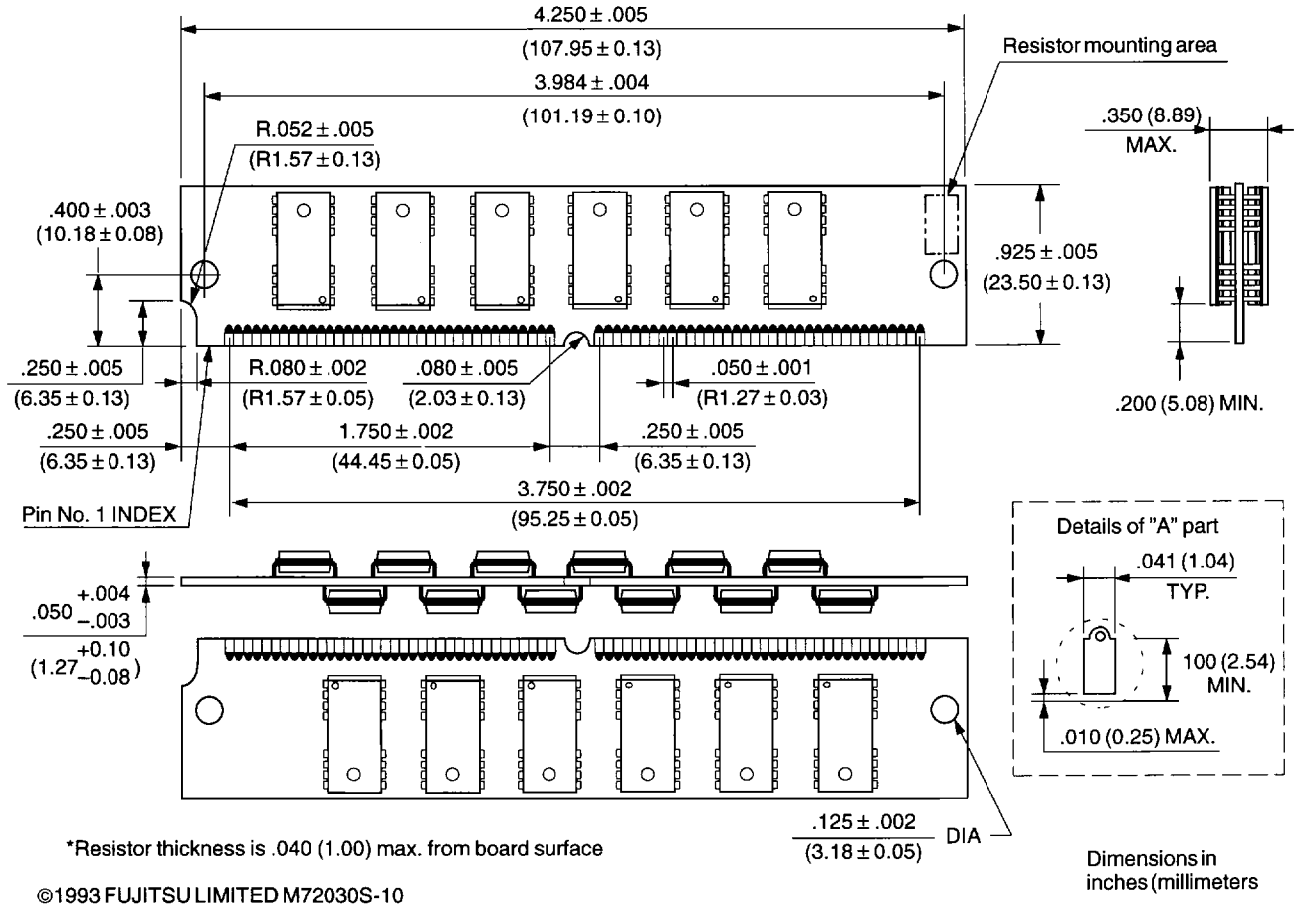
* Source: See MB814400A Data Sheet for details on the electricals.

PACKAGE DIMENSIONS

(Suffix: PJPBK)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P37)

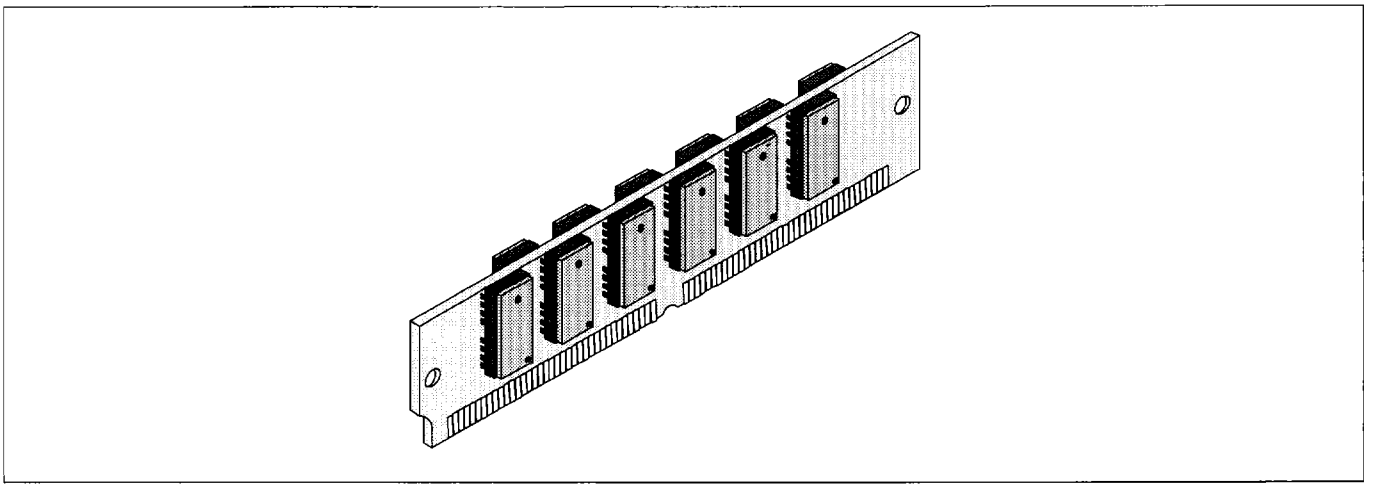


*Resistor thickness is .040 (1.00) max. from board surface

Dimensions in inches (millimeters

PACKAGE DIMENSIONS

(Suffix: PJPB)



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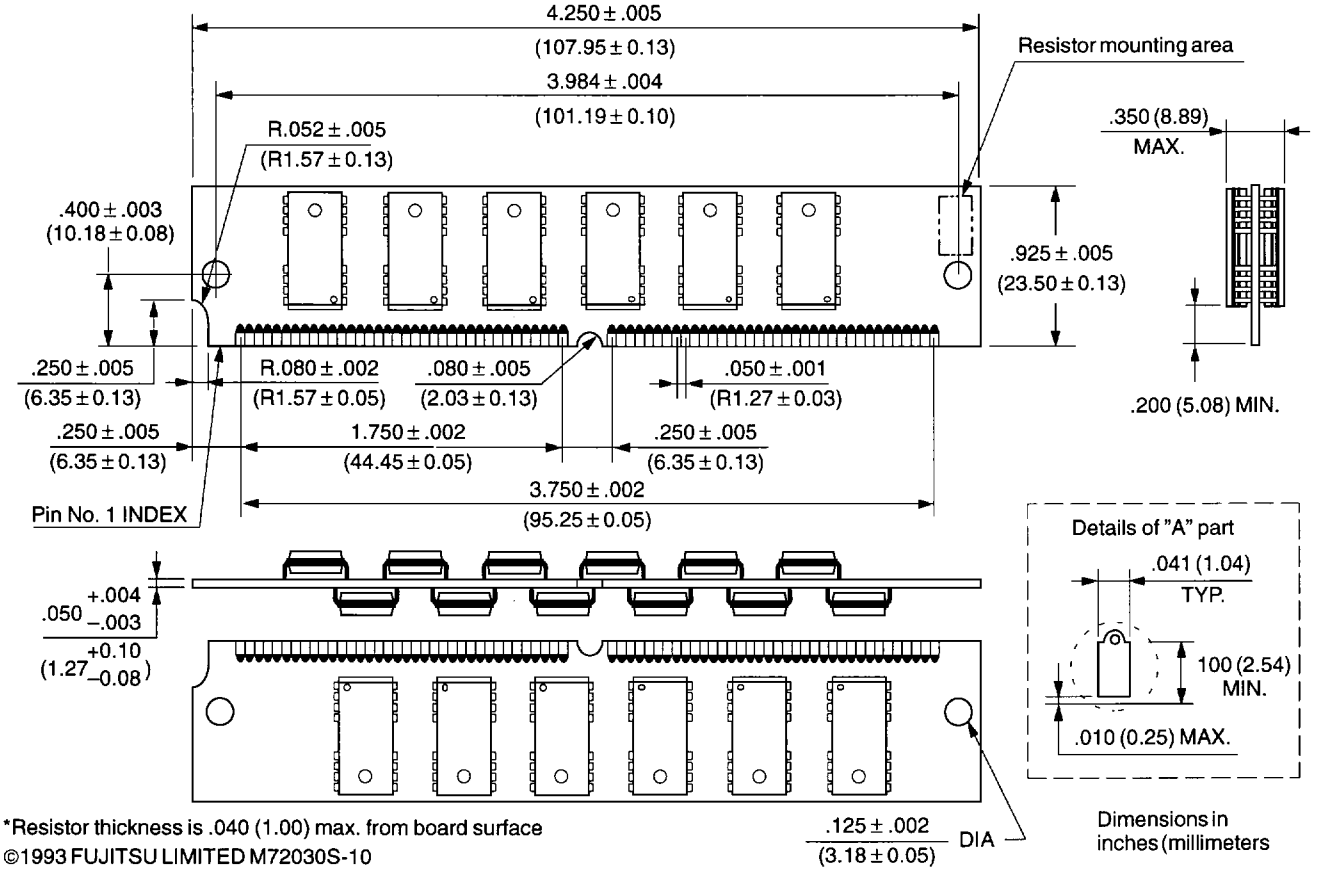

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FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
International Marketing Div.
Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Tel: (03) 3216-3211
Telex: 781-2224361
FAX: (03) 3215-0662

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: 408 -922-9000
FAX: 408-428-0640

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10,
6072 Dreieich-Buchschlag,
Germany
Tel: (06103) 690-0
Telex: 411963 fmg d
FAX: (06103) 690-122

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#06-04 to #06-07
Plaza By The Park,
No.51 Bras Basah Road,
Singapore 0719
Tel: 336-1600
Telex: 55573
FAX: 336-1609

Printed in Japan JV0050–939J2