



## Features

- AC offline input range from 80 to 277 VAC
- Constant current control with primary-side feedback
- Energy star compliant for LED lighting
- Up to 30W output power range for universal inputs
- High efficiency (typically > 85%)
- Tight LED current regulation (typically  $< \pm 2.5\%$ )
- Supports up to 130 kHz switching frequency
- Primary-side sensing eliminates opto-isolators
- Quasi-resonant operation for highest efficiency and low EMI
- No external compensation components required
- Low startup current (typically 10  $\mu$ A)
- Built-in soft start
- Multiple protection features
  - Current-sense resistor short protection (CSSP)
  - Over-temperature protection (OTP)
  - Output over-voltage protection (OVP)
  - Peak current limit protection (PCLP)
  - Output short circuit protection (OSCP)
  - Single-point fault protection
- Applications
  - Offline LED driver
  - LED replacement lamps
  - LED luminaires
  - Pre-regulator for intelligent DC-to-DC LED controllers

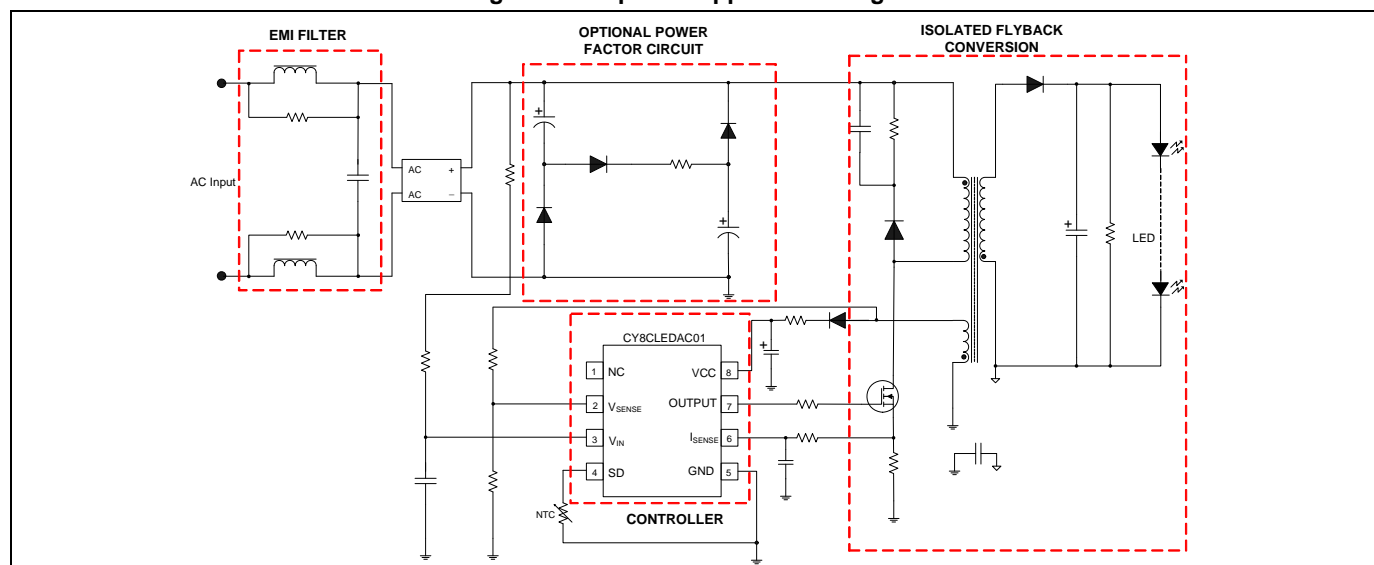
### Description

The CY8CLEDAC01 uses an advance digital control algorithm to reduce system design time and improve reliability. The control algorithm has cycle-by-cycle adaptive digital regulation; this enables accurate secondary-side constant-current operation without the need for secondary-side sense and control circuits. The cycle-by-cycle adaptive digital regulation features fast dynamic response and tight output regulation using critical discontinuous conduction mode (CDCM) when driving LED loads. The control algorithm for cycle-by-cycle regulation has internal compensation for guaranteed system phase and gain margins; requiring no external components for loop compensation.

The CY8CLEDAC01 has full featured circuit protection not normally available with other primary-side control solutions. The built-in protection features include over-voltage protection (OVP), output short circuit protection (OSCP), peak current limit protection (PCLP), and current-sense resistor short protection (CSSP), over-temperature protection (OTP).

The CY8CLEDAC01 also operates as a voltage-mode controller with all the current-mode controller features, allowing it to operate as a AC-to-DC front-end for intelligent LED controllers such as Cypress's PowerPSoC<sup>®</sup> family.

### Figure 1. Simplified Application Diagram





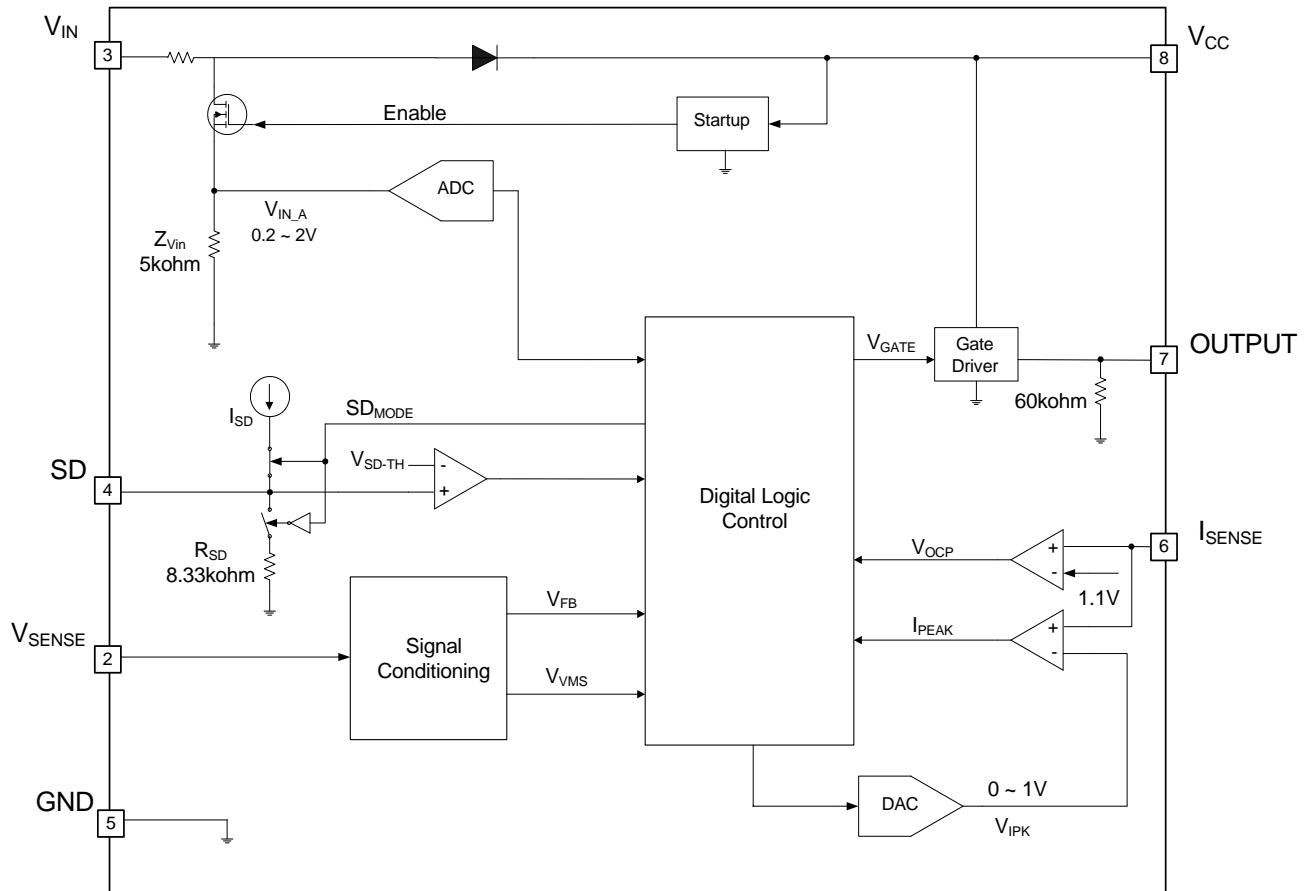
## Contents

<b>FEATURES .....</b>	<b>1</b>	<b>PIN INFORMATION .....</b>	<b>7</b>
<b>DESCRIPTION .....</b>	<b>1</b>	<b>ELECTRICAL SPECIFICATIONS .....</b>	<b>8</b>
<b>CONTENTS .....</b>	<b>2</b>	Absolute Maximum Ratings .....	8
<b>LOGIC BLOCK DIAGRAM .....</b>	<b>3</b>	<b>ELECTRICAL CHARACTERISTICS .....</b>	<b>9</b>
<b>FUNCTIONAL DESCRIPTION .....</b>	<b>3</b>	<b>TYPICAL PERFORMANCE CHARACTERISTICS .....</b>	<b>10</b>
Overview .....	3	<b>ORDERING INFORMATION .....</b>	<b>12</b>
Constant Current Operation .....	4	<b>ORDERING CODE DEFINITIONS .....</b>	<b>12</b>
Valley Mode Switching .....	4	<b>PACKAGING INFORMATION .....</b>	<b>13</b>
Protection Features .....	4	Physical Package Dimensions .....	13
Understanding Primary Feedback .....	5	<b>DOCUMENT HISTORY PAGE .....</b>	<b>14</b>
Constant Voltage Operation .....	6	<b>SALES, SOLUTIONS, AND LEGAL INFORMATION .....</b>	<b>14</b>
Dynamic Load Transient .....	6	Worldwide Sales and Design Support .....	14
Variable Frequency Operation .....	6		
Internal Loop Compensation .....	6		
PFM Mode at Light Load .....	6		



## Logic Block Diagram

Figure 2. Logic Block Diagram



## Functional Description

### Overview

The digital logic control block is the main block. All other blocks are inputs or outputs for the control block.

The control block receives signals to determine the input voltage ( $V_{IN}$ ), output voltage ( $V_{SENSE}$ ), temperature ( $SD$ ), output operation ( $V_{CC}$ ), and output current ( $I_{SENSE}$ ).

The control block has three output controls;  $SD_{MODE}$  (shutdown mode control), DAC  $V_{IPK}$  (current control), and  $V_{GATE}$  (gate drive control).

The control block does not start operation until  $V_{CC}$  has charged to the startup threshold ( $V_{CCST}$ ) as shown in Figure 3.  $V_{CC}$  is charged through a diode connection from  $V_{IN}$ .  $V_{IN}$  receives a voltage from a rectified main power input. When  $V_{CC}$  is charged to  $V_{CCST}$ , the startup block enables the  $V_{IN}$  scaling resistance ( $Z_{VIN}$ ) and the control block. The startup block also monitors the  $V_{CC}$  level and resets the system when  $V_{CC}$  decreases to a brown-out level ( $V_{CCUVL}$ ). The reset initiates a startup sequence where  $V_{CC}$  is charged to  $V_{CCST}$  level through a diode connection from  $V_{IN}$ .

When the  $Z_{VIN}$  resistor is enabled, a voltage  $V_{IN\_A}$  is measurable by an ADC. The output of the ADC is provided to the control block for auto-calculation of the  $V_{IN}t_{ON}$  product where  $t_{ON}$  is the on time for the flyback MOSFET. After the voltage on  $V_{IN\_A}$  is above the startup low voltage threshold ( $V_{INSTLOW}$ ), the CY8CLEDAC01 commences an adaptive soft start function. The soft start control algorithm is applied at startup, during which the initial output pulses are small and gradually increase until the full pulse width is achieved.

The  $V_{SENSE}$  pin connects to the Signal Conditioning block. The Signal Conditioning block provides two inputs to the control block:  $V_{FB}$  (Voltage Feed Back) and  $V_{VMS}$  (Voltage Valley Mode Switch).  $V_{FB}$  provides over-voltage protection and  $V_{CC}$  measurement.  $V_{VMS}$  is the valley switch detection.  $V_{FB}$  is monitored by the control block to determine if the output is over-voltage. When the control block detects an over-voltage condition, it enters a shutdown mode and wait for POR to re-initialize the system.  $V_{VMS}$  is monitored by the control block to determine when the power in the flyback MOSFET is at a minimum or in a 'valley'. The control block starts the next cycle at the 'valley' for maximum efficiency and minimum switching EMI.

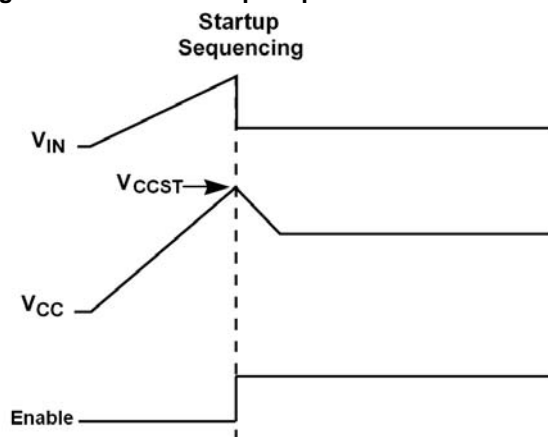


The SD pin connects to two blocks; a switched current source ( $I_{SD}$ ) and an analog comparator. These two blocks work together for OTP and optional OVP. For an OTP implementation, the SD pin can be connected to an external NTC component. The current source causes a voltage to be developed at the SD pin which causes the analog comparator's output to be high or low depending upon a 1V comparator reference. If the voltage across the NTC is less than 1V, the control block enters a shutdown mode and wait for POR to reinitialize the system.

The  $I_{SENSE}$  pin connects to circuitry composed of three blocks: DAC  $V_{IPK}$ ,  $I_{PEAK}$  comparator, and  $V_{OCP}$  comparator. These three blocks work together for soft-start control, peak current detection, and over-current protection. The DAC  $V_{IPK}$  controls soft-start, minimizing stress associated with system startup. The  $I_{PEAK}$  comparator monitors the voltage at the  $I_{SENSE}$  pin. The voltage is generated by current flowing through a small external resistor ( $R_{ISENSE}$  - not shown). When the  $I_{SENSE}$  voltage reaches 1V, the  $I_{PEAK}$  comparator asserts a high to the control block. The control block shuts off the output and waits for  $V_{VMS}$  detection; it then starts the next cycle. The  $V_{OCP}$  comparator provides primary side over-current protection. When the voltage on  $I_{SENSE}$  reaches 1.1V, the  $V_{OCP}$  signal gets asserted. When over-current is detected, the control block enters a shutdown mode and waits for POR to re initialize the system.

The OUTPUT pin connects to the Gate Driver block. The Gate Driver connects to the OUTPUT pin that in turn connects to the flyback MOSFET gate pin (not shown). The OUTPUT pin is a digital control pin that switches between a high level (approximately  $V_{CC}$ ) and a low level (approximately ground). The duration for high ( $t_{ON}$ ) and low ( $t_{OFF}$ ) of the Gate Driver is a function of the control block operating upon its inputs:  $V_{IN}$ ,  $t_{ON}$ ,  $V_{FB}$ ,  $V_{VMS}$ , SD,  $I_{PEAK}$ ,  $V_{OCP}$ , and  $V_{CC}$ .

**Figure 3. Device Startup Sequence**



### Constant Current Operation

Constant current (CC) mode is the normal operating mode for LED lighting applications. CY8CLEDAC01 operates in CC mode when  $V_{SENSE}$  is set below  $V_{SENSENOM}$ . During this mode, the CY8CLEDAC01 regulates the output current at a constant level regardless of the output voltage. It operates in critical discontinuous conduction mode (CDCM) while in CC mode.

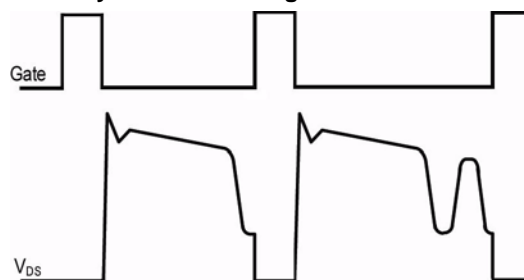
To achieve CC regulation, the CY8CLEDAC01 senses the load current indirectly through the primary current. The primary

current is detected by the  $I_{SENSE}$  pin through a resistor from the MOSFET source to ground.

### Valley Mode Switching

To reduce EMI and switching losses in the MOSFET, the CY8CLEDAC01 employs valley mode switching when operating in CDCM by switching at the lowest MOSFET  $V_{DS}$  (see Figure 4). It detects valleys in the MOSFET drain voltage indirectly through the  $V_{SENSE}$  pin. This voltage is provided by the auxiliary winding of the flyback transformer and represents a copy of the secondary side characteristics (see Figure 7 on page 6).

**Figure 4. Valley Mode Switching**



Turning on at the lowest  $V_{DS}$  generates lowest  $dV/dt$ ; thus valley mode switching minimizes switching losses and reduces EMI. To limit the switching frequency range, the CY8CLEDAC01 can skip valleys (second cycle in Figure 4) when the switching frequency becomes too high.

The CY8CLEDAC01 supports valley mode switching in both CC and constant voltage (CV) modes of operation. This feature is superior to other quasi-resonant technologies which only support valley mode switching during constant voltage operation.

### Protection Features

The CY8CLEDAC01 has full featured circuit protection not normally available with other primary-side control solutions.

The built-in protection features include over-voltage protection (OVP), output short circuit protection (OSCP), peak current limit protection (PCLP), and current-sense resistor short protection (CSSP), over-temperature protection (OTP).

In an event a protection is triggered,  $V_{CC}$  discharges below  $V_{CCUVL}$  and causes a POR except in case of PCLP. The controller now initiates a new soft start cycle and continues to attempt start-up. It is unable to start up until the fault condition is removed.

#### Current Sense Resistor Short Protection (CSSP)

If the  $I_{SENSE}$  sense resistor is shorted, there is a potential danger of an over-current condition not being detected. The CY8CLEDAC01 has a separate circuit to detect this fault. This protection mode is triggered if the  $I_{SENSE}$  voltage is below 0.15V in CC mode and only at heavy loads in CV mode.

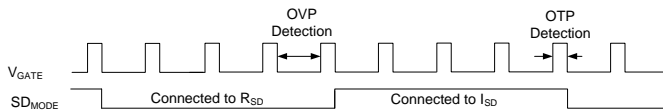
#### Over-Temperature Protection (OTP) and/or Output Over-Voltage Protection (OVP)

The shutdown (SD) pin along with an external NTC provides over-temperature protection. The SD pin also provides optional over-voltage protection by sensing a scaled auxiliary winding



voltage from the flyback transformer using external components. The CY8CLEDAC01 switches between monitoring an over-temperature fault and an over-voltage fault on the SD pin by using the SD<sub>MODE</sub> control signal (shown in Figure 2 on page 3). For an over-temperature fault the voltage on the NTC is detected by connecting an internal current source to the pin. For an over-voltage fault the voltage on the SD pin is checked using an internal pulldown resistance R<sub>SD</sub>. The measurements are made during the last V<sub>GATE</sub> cycle in the measurement window to allow transients to settle.(shown in Figure 5)

**Figure 5. SD Detection**



When SD<sub>MODE</sub> is high and the voltage across the NTC is lower than 1V during normal operation or 1.2V during start-up an OTP is triggered. When SD<sub>MODE</sub> is low and the sensed voltage on the SD pin is higher than 1V an OVP fault is triggered.

#### Output Over-Voltage Protection (OVP)

The CY8CLEDAC01 includes a function that protects against an output over-voltage. The output voltage is monitored by the V<sub>SENSE</sub> pin. The protection is triggered if the voltage at this pin exceeds the over-voltage threshold V<sub>SENSEMAX</sub>.

#### Peak Current Limit Protection (PCLP)

The I<sub>SENSE</sub> pin of the CY8CLEDAC01 monitors the primary peak current. This enables cycle-by-cycle peak current control and limiting. When the primary peak current multiplied by the sense resistor value is greater than 1.1V, an over-current condition is detected and the IC immediately turns off the MOSFET driver. During the next switching cycle, the driver sends out a regular switching pulse and turns off again if the OCP threshold is still reached. Normal switching resumes if the fault is removed and the OCP threshold is not reached.

#### Output Short Circuit Protection (OSCP)

The CY8CLEDAC01 includes a function that protects against an output short circuit. The output voltage is monitored by the V<sub>SENSE</sub> pin. The protection is triggered if the voltage at this pin is below 0.22V.

**Note** When the V<sub>SENSE</sub> is at this level, the controller is by default operating in CC mode and hence an over current condition cannot happen.

#### Single Point Fault Protection

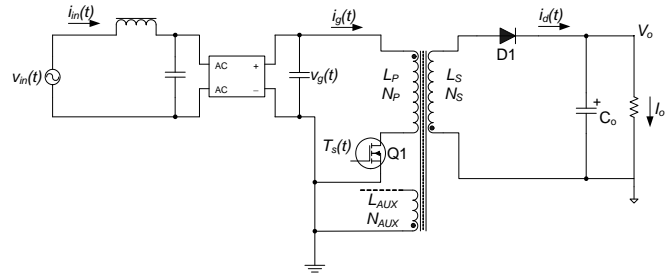
The CY8CLEDAC01 detect a short on any of the following pins I<sub>SENSE</sub>, V<sub>SENSE</sub>, V<sub>CC</sub>, OUTPUT, and SD. Therefore, any single point fault is protected against.

### Understanding Primary Feedback

Figure 6 illustrates a simplified flyback converter. When the switch Q1 conducts during t<sub>ON</sub>(t), the current i<sub>g</sub>(t) is directly drawn from rectified sinusoid v<sub>g</sub>(t). The energy E<sub>g</sub>(t) is stored in the magnetizing inductance L<sub>p</sub>. The rectifying diode D1 is reverse biased and the load current I<sub>O</sub> is supplied by the

secondary capacitor C<sub>O</sub>. When Q1 turns off, D1 conducts and the stored energy E<sub>g</sub>(t) is delivered to the output.

**Figure 6. Simplified Flyback Converter**



When operating in CC mode, to tightly regulate output current, information about the load current needs to be accurately sensed. To achieve CC regulation, this information can be derived indirectly by sensing the primary current.

When operating in CV mode, to tightly regulate output voltage, information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read through the auxiliary winding.

During the Q1 on time, the load current is supplied from the output filter capacitor C<sub>O</sub>. The voltage across L<sub>p</sub> is v<sub>g</sub>(t), assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

#### Equation 1

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_p}$$

At the end of on time, the current has ramped up to:

#### Equation 2

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_p}$$

This current represents a stored energy of:

#### Equation 3

$$E_g = \frac{L_p}{2} \times i_{g\_peak}(t)^2$$

When Q1 turns off, i<sub>g</sub>(t) in L<sub>p</sub> forces a reversal of polarities on all windings. Ignoring the commutation time caused by the leakage inductance L<sub>KP</sub> at the instant of turn-off, the primary current transfers to the secondary at a peak amplitude of:

#### Equation 4

$$i_d(t) = \frac{N_p}{N_s} \times i_{g\_peak}(t)$$

Assuming the secondary winding is master and the auxiliary winding is slave, the auxiliary voltage is given by:

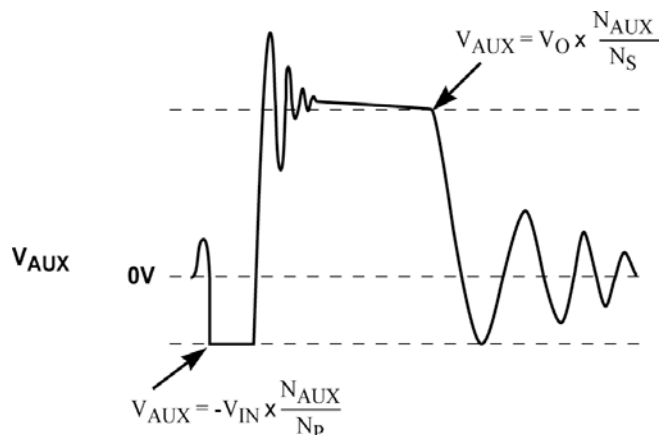


**Equation 5**

$$V_{AUX} = \frac{N_{AUX}}{N_S} (V_O + \Delta V)$$

and reflects the output voltage as shown in [Figure 7](#).

**Figure 7. Auxiliary Voltage Waveforms**



The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed  $\Delta V$ . Further, if the voltage can be read when the secondary current is small; for example, at the knee of the auxiliary waveform (see [Figure 7](#)), then  $\Delta V$  is also small. With the CY8CLEDAC01,  $\Delta V$  can be ignored.

The real time waveform analyzer in the CY8CLEDAC01 reads the auxiliary waveform information cycle by cycle. The part then generates a feedback voltage  $V_{FB}$ . The  $V_{FB}$  signal precisely represents the output voltage and is used to regulate the output voltage.

**Constant Voltage Operation**

The CY8CLEDAC01 also features a constant voltage (CV) mode. It operates in CV mode when  $V_{SENSE}$  is set between  $V_{SENSE(NOM)}$  and  $V_{SENSE(MAX)}$ . After soft start is completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or a heavy load. It uses CDCM or pulse width modulation (PWM) at high output power levels and switches to pulse frequency modulation (PFM) at light loads to minimize power dissipation. The PWM switching frequency is between 30 kHz and 130 kHz, depending on the line and load conditions.

**Dynamic Load Transient**

There are two components that compose the voltage drop during a load transient event.

$V_{DROP(SENSE)}$  is the drop in voltage before the  $V_{SENSE}$  signal is able to show a significant drop in output voltage. This is determined by  $V_{min}$  or the reference voltage at which a load transient is detected. The smaller the  $V_{min}$  is, the smaller is the drop in voltage.

**Equation 6**

$$V_{DROP(SENSE)} = (V_{SENSE(NOM)} - V_{SENSE(MIN)}) \times \frac{V_{OUT(DESIGN)}}{V_{SENSE(NOM)}}$$

Remember that a smaller  $V_{min}$  is less tolerant of noise and can lead to signal distortion in  $V_{SENSE}$ .

The final drop in voltage is due to the time from when  $V_{SENSE}$  drops  $V_{min}$  to when the next  $V_{SENSE}$  signal appears. In the worst case condition this is how much voltage drops during the longest switching period.

**Equation 7**

$$V_{DROP(IC)} = \frac{I_{OUT} \times T_{P(NoLoad)}}{C_{OUT}}$$

A larger output capacitance in this case greatly reduces the  $V_{DROP(IC)}$ .

**Variable Frequency Operation**

An internal circuit checks for the falling edge of  $V_{SENSE}$  on every switching cycle. If the falling edge of  $V_{SENSE}$  is not detected, the off-time is extended until the falling edge of  $V_{SENSE}$  is detected. The maximum allowed transformer reset time for the CY8CLEDAC01 is 75  $\mu s$ .

**Internal Loop Compensation**

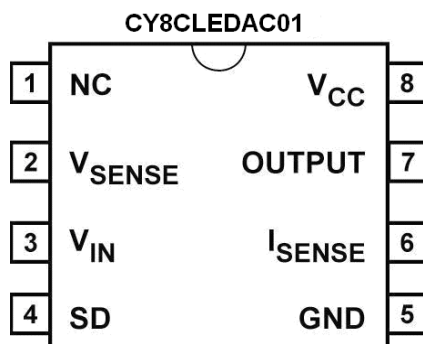
The CY8CLEDAC01 incorporates an internal digital error amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20 dB of gain margin.

**PFM Mode at Light Load**

The CY8CLEDAC01 normally operates in a fixed frequency PWM or Critical Discontinuous Conduction Mode when  $I_{OUT}$  is greater than approximately 10 percent of the specified maximum load current. As the output load  $I_{OUT}$  is reduced, the on-time  $t_{ON}$  is decreased. The moment the load current drops below 10 percent of nominal, the controller transitions to pulse frequency modulation (PFM) mode. Thereafter, the on-time is modulated by the line voltage and the off-time is modulated by the load current. The device automatically returns to PWM mode when the load current increases.



## Pin Information



Pin No.	Name	Type	Description
1	NC	-	No connection
2	$V_{SENSE}$	Analog Input	Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.
3	$V_{IN}$	Analog Input	Sense signal input from the rectified line voltage. $V_{IN}$ is used for line regulation. The input line voltage is scaled down using a resistor network, and is used for input under-voltage and over-voltage protection. This pin also provides the supply current to the IC during startup.
4	SD	Analog Input	External shutdown control. This pin should be pulled down to GND using a 20k $\Omega$ resistor if shutdown control is not required.
5	GND	Ground	Ground
6	$I_{SENSE}$	Analog Input	Primary current sense. Used for cycle by cycle peak current control.
7	OUTPUT	Output	Gate drive for external MOSFET switch
8	$V_{CC}$	Power Input	Power supply for the controller during normal operation. The controller starts up when $V_{CC}$ reaches 12V (typical) and shuts down when the $V_{CC}$ voltage is below 6V (typical). A decoupling capacitor should be connected between the $V_{CC}$ pin and GND.



## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLEDAC01, of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com/powerpsoc>. Specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  and  $T_J \leq 125^{\circ}\text{C}$ , except where noted. Table 1 lists the units of measure that are used in this section.

**Table 1. Units of Measure**

Symbol	Unit of Measure	Symbol	Unit of Measure	Symbol	Unit of Measure
$^{\circ}\text{C}$	degrees Celsius	kbit	1024 bits	mA	milliampere
dB	decibels	kHz	kilohertz	ms	millisecond
Hz	Hertz	$\text{k}\Omega$	kilohms	mV	millivolts
pp	peak-to-peak	MHz	megahertz	mA	milliwatts
$\sigma$	sigma:one standard deviation	$\text{M}\Omega$	megaohms	nA	nanoamperes
V	volts	$\mu\text{A}$	microamperes	ns	nanoseconds
$\Omega$	ohms	$\mu\text{F}$	microfarads	nV	nanovolts
KB	1024 bytes	$\mu\text{H}$	microhenrys	pA	picoamperes
ppm	parts per million	$\mu\text{s}$	microseconds	pF	picofarads
sps	samples per second	$\mu\text{V}$	microvolts	ps	picoseconds
W	watts	$\mu\text{V}_{\text{rms}}$	microvolts root-mean-square	fF	femtofarads
A	amperes	$\mu\text{W}$	microwatts		

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{\text{CC}}$	DC supply voltage range	-0.3	-	18	V	pin 8, $I_{\text{CC}} = 20 \text{ mA max}$
$I_{\text{CC}}$	DC supply current at $V_{\text{CC}}$ pin	-	-	20	mA	pin 8
	Output pin voltage	-0.3	-	18	V	pin 7
	$V_{\text{SENSE}}$ pin voltage	-0.7	-	4.0	V	pin 2, $I_{\text{SENSE}} \leq 10 \text{ mA}$
	$V_{\text{IN}}$ pin voltage	-0.3	-	18	V	pin 3
	$I_{\text{SENSE}}$ pin voltage	-0.3	-	4.0	V	pin 6
	SD pin voltage	-0.3	-	18	V	pin 4
$P_D$	Power Dissipation	-	-	526	mW	$T_A \leq 25^{\circ}\text{C}$
$T_{\text{J,max}}$	Maximum Junction Temperature	-	-	125	$^{\circ}\text{C}$	
$T_{\text{STG}}$	Storage Temperature	-65	-	150	$^{\circ}\text{C}$	
$T_{\text{LEAD}}$	Lead Temperature	-	-	260	$^{\circ}\text{C}$	During IR reflow for $\leq 15$ seconds
$\theta_{\text{JA}}$	Thermal Resistance Junction-to-ambient	-	-	160	$^{\circ}\text{C/W}$	
$V_{\text{ESD}}$	ESD Voltage Rating	-	-	2000	V	as per JEDEC JESD22-A114
$I_{\text{LU}}$	Latch Up Current	-100	-	100	mA	as per JEDEC JESD78



## Electrical Characteristics

$V_{CC}=12V$ ;  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$  unless otherwise specified<sup>[1]</sup>

Symbol	Description	Min	Typ	Max	Units	Notes
<b>V<sub>IN</sub> Section (pin 3)</b>						
V <sub>INSTLOW</sub>	Startup low voltage threshold	335	369	406	mV	T <sub>A</sub> = 25°C Positive Edge
I <sub>INST</sub>	Startup current	-	10	15	μA	V <sub>IN</sub> = 10V, C <sub>VCC</sub> = 10 μF
Z <sub>IN</sub>	Input impedance	-	5	-	kΩ	After Startup
<b>V<sub>SENSE</sub> Section (pin 2)</b>						
I <sub>BVS</sub>	Input leakage current	-	-	1	μA	V <sub>SENSE</sub> = 2V
V <sub>SENSE</sub> NOM	Nominal voltage threshold	1.523	1.538	1.553	V	T <sub>A</sub> = 25°C Negative Edge
V <sub>SENSE</sub> MAX	Output OVP threshold	1.790	1.846	1.900	V	T <sub>A</sub> = 25°C Negative Edge
<b>OUTPUT Section (pin 7)</b>						
R <sub>DS(ON)LO</sub>	Output low level ON-resistance	-	40	-	Ω	I <sub>SINK</sub> = 5 mA
R <sub>DS(ON)HP</sub>	Output high level ON-resistance	-	102	-	Ω	I <sub>SOURCE</sub> = 5 mA
t <sub>R</sub>	Rise time <sup>[2]</sup>	-	200	300	ns	T <sub>A</sub> = 25°C; CL = 330 pF; 10% to 90%
t <sub>F</sub>	Fall time <sup>[2]</sup>	-	40	60	ns	T <sub>A</sub> = 25°C; CL = 330 pF; 10% to 90%
F <sub>SWMAX</sub>	Maximum switching frequency <sup>[3]</sup>	-	130	140	kHz	Any Combination of Line and Loads
<b>V<sub>CC</sub> Section (pin 8)</b>						
V <sub>CCMAX</sub>	Maximum operating voltage	-	-	16	V	
V <sub>CCST</sub>	Startup threshold	10.8	12	13.2	V	V <sub>CC</sub> Rising
V <sub>CCUVL</sub>	Under-voltage lockout threshold	5.5	6.0	6.6	V	V <sub>CC</sub> Falling
I <sub>CC</sub>	Operating current	-	3.5	-	mA	C <sub>L</sub> = 330 pF; V <sub>SENSE</sub> = 1.5V
<b>I<sub>SENSE</sub> Section (pin 6)</b>						
V <sub>PEAK</sub>	Peak limit threshold		1.1		V	
V <sub>RSNS</sub>	I <sub>SENSE</sub> short protection reference	-	0.15	-	V	
V <sub>REGTH</sub>	CC regulation threshold limit	-	1.0	-	V	
<b>SD Section (pin 4)</b>						
V <sub>SDTH</sub>	Shutdown threshold	0.95	1.0	1.05	V	
V <sub>SDTHST</sub>	Shutdown threshold in startup	-	1.2	-	V	
I <sub>BVSD</sub>	Input leakage current	-	-	1.0	μA	V <sub>SD</sub> = 1.0V
R <sub>SD</sub>	Pull down resistance	7.916	8.333	8.750	kΩ	
I <sub>SD</sub>	Pull up current source	96	107	118	μA	

### Notes

1. Adjust V<sub>CC</sub> above the startup threshold before setting at 12V.
2. These parameters are not 100% tested, guaranteed by design and characterization.
3. Operating frequency varies based on the line and load conditions, see [Functional Description](#) on page 3 for more details.



## Typical Performance Characteristics

Figure 8.  $V_{CC}$  Supply Current versus  $V_{CC}$

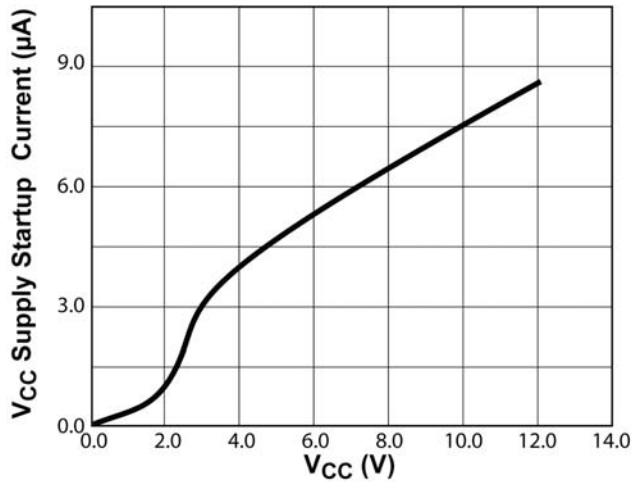


Figure 9. Switching Frequency% Change versus Temperature

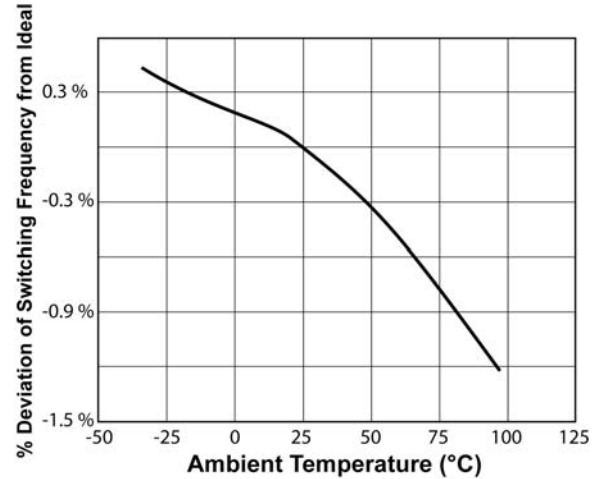


Figure 10. Startup Threshold versus Temperature

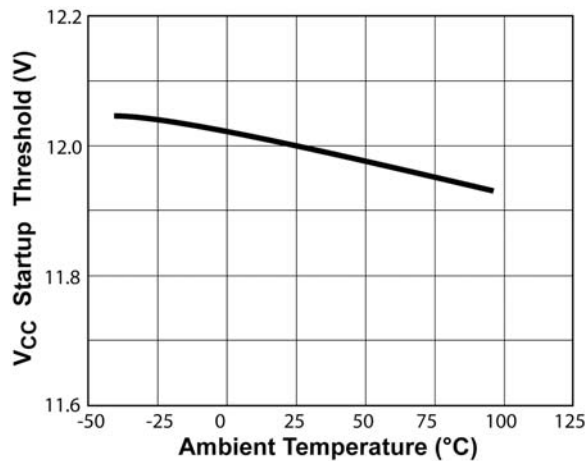


Figure 11. Internal Reference versus Temperature

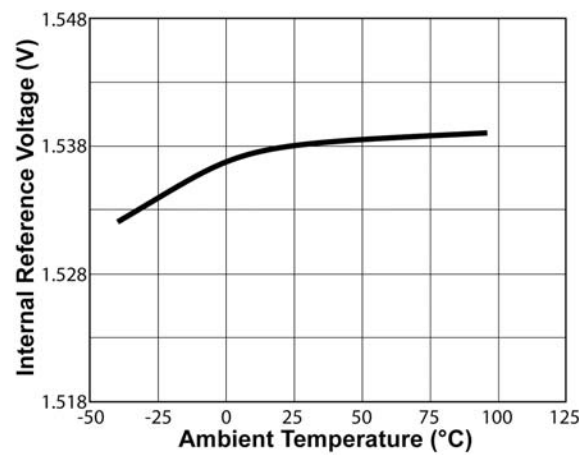
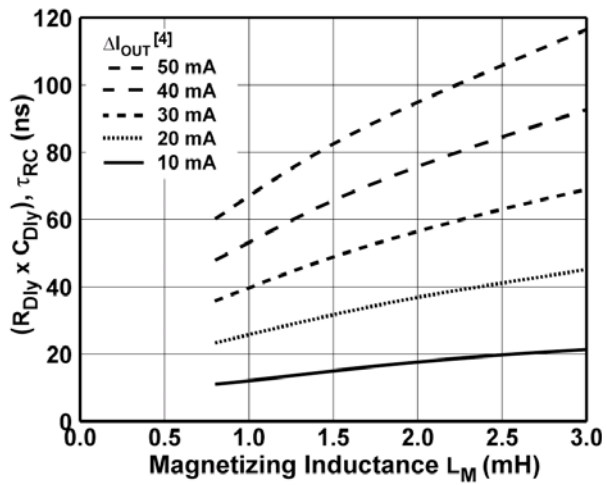




Figure 12.  $T_{ON}$  Compensation Chart



**Note**

4.  $\Delta I_{OUT}$  refers to the difference in constant current limit between 264 VAC and 90 VAC when no  $R_{DLY}$  and  $C_{DLY}$  are applied.

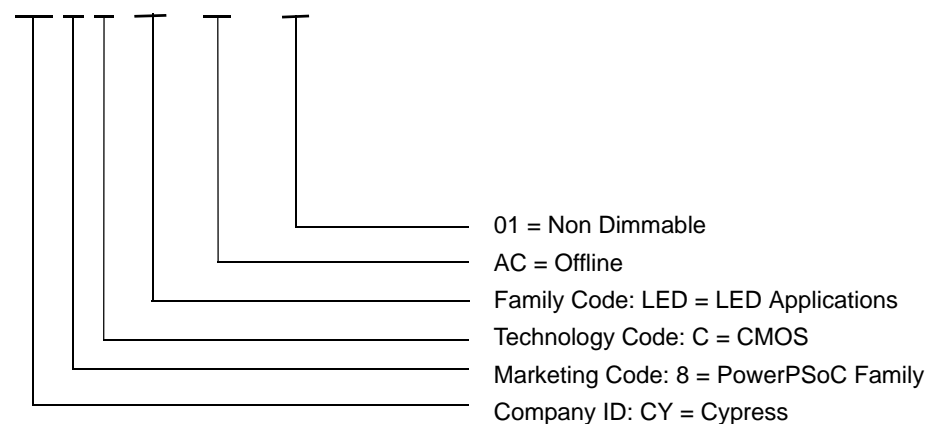


## Ordering Information

Ordering Code	No. of Pins	Package	Temperature Range
CY8CLEDAC01	8	SOIC	-40°C to 85°C

## Ordering Code Definitions

CY 8 C LED AC 01

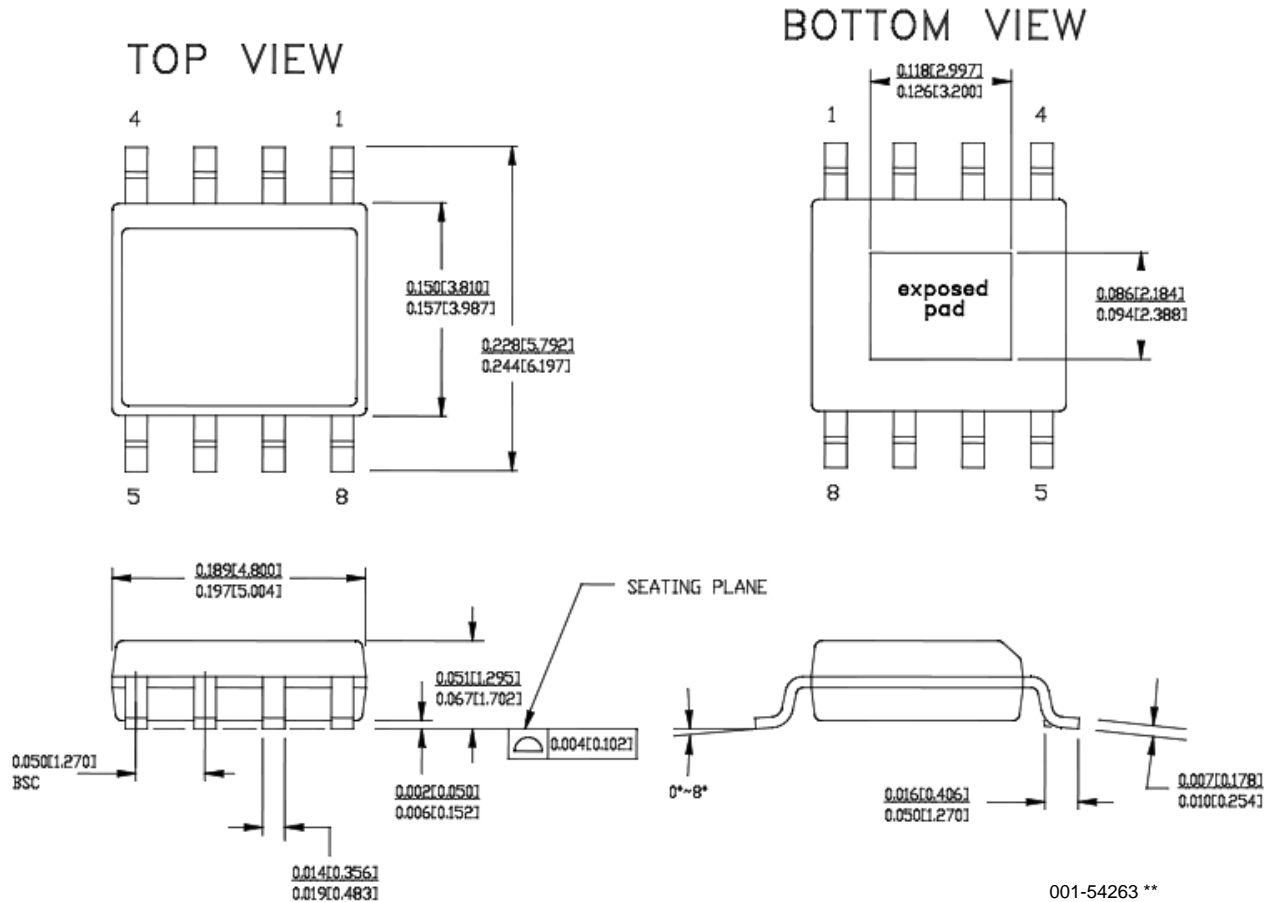




## Packaging Information

### Physical Package Dimensions

Figure 13. 8-Pin Small Outline (SOIC) Package





## Document History Page

Document Title: CY8CLEDAC01 AC/DC Digital Current-Mode Controller for LED Lighting Document Number: 001-54122				
Revision	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2721319	KJV/AESA	06/19/2009	New data sheet
*A	2829351	KJV/PYRS	12/16/2009	Added <a href="#">Contents</a> . Updated text in <a href="#">Features</a> , <a href="#">Description</a> , and <a href="#">Functional Description</a> sections. Updated <a href="#">Electrical Specifications</a>
*B	2901104	KJV/VED	03/29/2010	Release to web.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturers' representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

[Automotive](#)  
[Clocks & Buffers](#)  
[Interface](#)  
[Lighting & Power Control](#)  
[Memory](#)  
[Optical & Image Sensing](#)  
[PSoC](#)  
[Touch Sensing](#)  
[USB Controllers](#)  
[Wireless/RF](#)

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
[PSoC 1](#) | [PSoC 3](#) | [PSoC 5](#)

© Cypress Semiconductor Corporation, 2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.