FM28V102

1Mbit (64K×16)F-RAM Memory

FEATURES

1Mbit Ferroelectric Nonvolatile RAM

- Organized as 64Kx16
- Configurable as 128Kx8 Using /UB, /LB
- 10^{14} Read/Write Cycles
- NoDelay™ Writes
- Page Mode Operation to 33MHz
- Advanced High-Reliability Ferroelectric Process

SRAM Compatible

- Industry Std. 64Kx16 SRAM Pinout
- 60 ns Access Time, 90 ns Cycle Time

Superior to Battery-backed SRAM Modules

- No Battery Concerns
- Monolithic Reliability
- True Surface Mount Solution, No Rework Steps
- Superior for Moisture, Shock, and Vibration

Low Power Operation

- 2.0V – 3.6V Power Supply
- Standby Current 120 μA (typ)
- Active Current 7 mA (typ)

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 44-pin “Green”/RoHS TSOP-II package

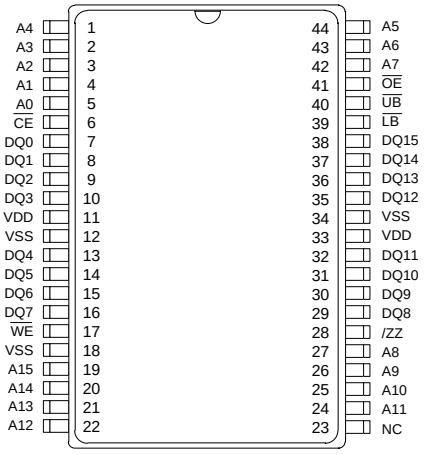
DESCRIPTION

The FM28V102 is a 64Kx16 nonvolatile memory that reads and writes like a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 10 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make the F-RAM superior to other types of memory.

In-system operation of the FM28V102 is very similar to other RAM devices and can be used as a drop-in replacement for standard SRAM. Read and write cycles may be triggered by /CE or simply by changing the address. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM28V102 ideal for nonvolatile memory applications requiring frequent or rapid writes in the form of an SRAM.

The device is available in a 400 mil 44-pin TSOP-II surface mount package. Device specifications are guaranteed over industrial temperature range –40°C to +85°C.

Pin Configuration



This is a product in the pre-production phase of development. Device characterization is complete and Ramtron does not expect to change the specifications. Ramtron will issue a Product Change Notice if any specification changes are made.

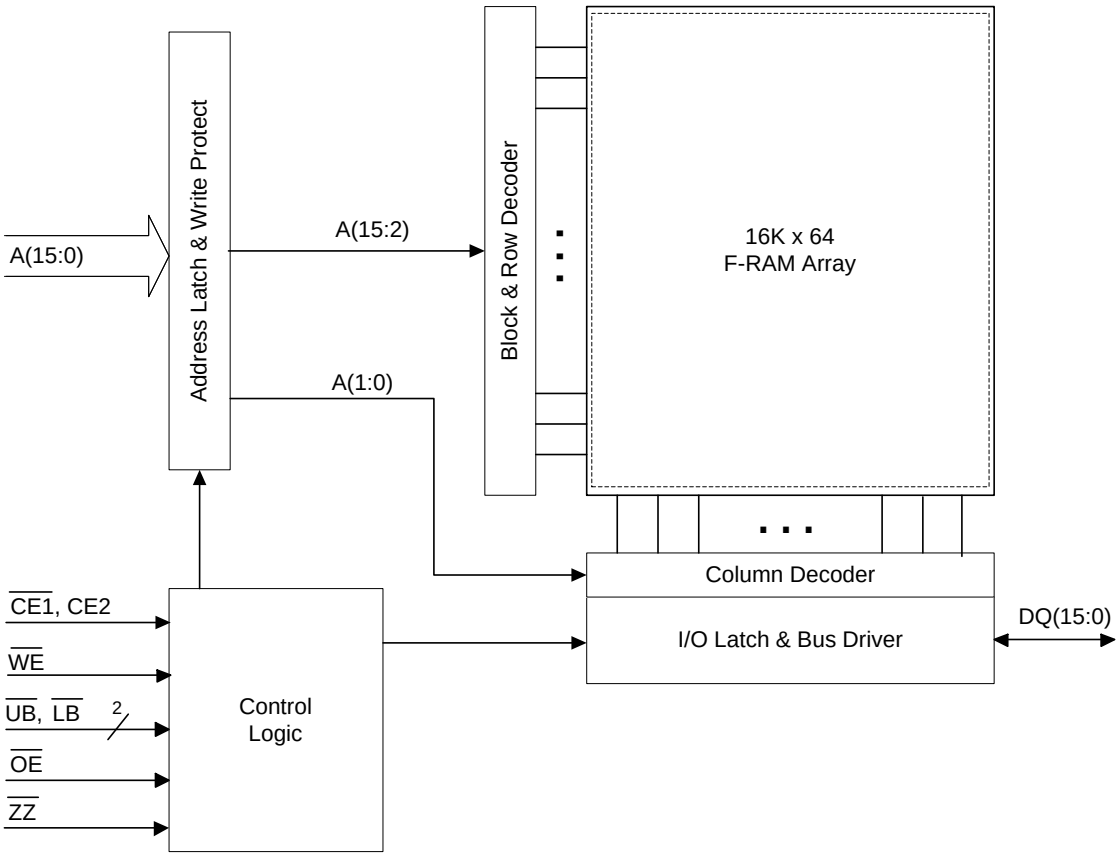


Figure 1. Block Diagram

PIN DESCRIPTION

Pin Name	Type	Pin Description
A(15:0)	Input	Address inputs: The 16 address lines select one of 64K words in the F-RAM array. The lowest two address lines A(1:0) may be used for page mode read and write operations.
/CE	Input	Chip Enable inputs: The device is selected and a new memory access begins on the falling edge of /CE. The entire address is latched internally at this point. Subsequent changes to the A(1:0) address inputs allow page mode operation.
/WE	Input	Write Enable: A write cycle begins when /WE is asserted. The rising edge causes the FM28V102 to write the data on the DQ bus to the F-RAM array. The falling edge of /WE latches a new column address for page mode write cycles.
/OE	Input	Output Enable: When /OE is low, the FM28V102 drives the data bus when valid read data is available. Deasserting /OE high tri-states the DQ pins.
/ZZ	Input	Sleep: When /ZZ is low, the device enters a low power sleep mode for the lowest supply current condition. Since this input is logically AND'd with /CE, /ZZ must be high for normal read/write operation. The /ZZ pin is internally pulled up.
DQ(15:0)	I/O	Data: 16-bit bi-directional data bus for accessing the F-RAM array.
/UB	Input	Upper Byte Select: Enables DQ(15:8) pins during reads and writes. These pins are hi-Z if /UB is high. If the user does not perform byte writes and the device is not configured as a 128Kx8, the /UB and /LB pins may be tied to ground.
/LB	Input	Lower Byte Select: Enables DQ(7:0) pins during reads and writes. These pins are hi-Z if /LB is high. If the user does not perform byte writes and the device is not configured as a 128Kx8, the /UB and /LB pins may be tied to ground.
VDD	Supply	Supply Voltage
VSS	Supply	Ground

Table 1. Functional Truth Table [1,2]

/CE	/WE	A(15:2)	A(1:0)	/ZZ	Operation
X	X	X	X	L	Sleep Mode
H	X	X	X	H	Standby/Idle
X	X	X	X		
↓	H	V	V	H	Read
L	H	V	V		
L	H	No Change	Change	H	Page Mode Read
L	H	Change	V	H	Random Read
↓	L	V	V	H	/CE-Controlled Write [2]
L	L	V	V		
L	↓	V	V	H	/WE-Controlled Write [2, 3]
L	↓	No Change	V	H	Page Mode Write [4]
↑	X	X	X	H	Starts Precharge
L	X	X	X		

Notes:

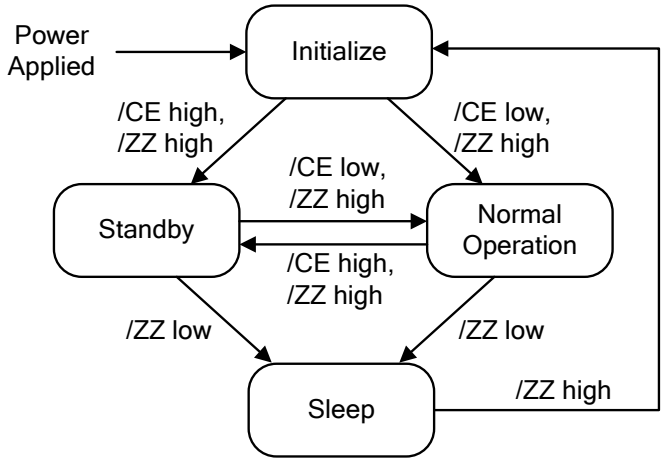
1) H=Logic High, L=Logic Low, V=Valid Data, X=Don't Care.
2) For write cycles, data-in is latched on the rising edge of /CE or /WE, whichever comes first.
3) /WE-controlled write cycle begins as a Read cycle and A(15:2) is latched then.
4) Addresses A(1:0) must remain stable for at least 15 ns during page mode operation.

Table 2. Byte Select Truth Table

/WE	/OE	/LB	/UB	Operation
H	H	X	X	Read; Outputs Disabled
	X	H	H	
H	L	H	L	Read upper byte; Hi-Z lower byte
		L	H	Read lower byte; Hi-Z upper byte
		L	L	Read both bytes
L	X	H	L	Write upper byte; Mask lower byte
		L	H	Write lower byte; Mask upper byte
		L	L	Write both bytes

The /UB and /LB pins may be grounded if 1) the system does not perform byte writes and 2) the device is not configured as a 128Kx8.

Simplified Sleep/Standby State Diagram



OVERVIEW

The FM28V102 is a wordwide F-RAM memory logically organized as 65,536 x 16 and accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation which provides higher speed access to addresses within a page (row). An access to a different page requires that either /CE transitions low or the upper address A(15:2) changes.

Memory Operation

Users access 65,536 memory locations, each with 16 data bits through a parallel interface. The F-RAM array is organized as 16,384 rows each having 64 bits. Each row has 4 column locations, which allows fast access in page mode operation. Once an initial address has been latched by the falling edge of /CE, subsequent column locations may be accessed without the need to toggle /CE. When /CE is deasserted high, a precharge operation begins. Writes occur immediately at the end of the access with no delay. The /WE pin must be toggled for each write operation. The write data is stored in the nonvolatile memory array immediately, which is a feature unique to F-RAM called NoDelay™ writes.

Read Operation

A read operation begins on the falling edge of /CE. The falling edge of /CE causes the address to be latched and starts a memory read cycle if /WE is high. Data becomes available on the bus after the access time has been satisfied. Once the address has been latched and the access completed, a new access to a random location (different row) may begin while /CE is still low. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the FM28V102's /CE-initiated access time is faster than the address cycle time.

The FM28V102 will drive the data bus when /OE and at least one of the byte enables (/UB, /LB) is asserted low. The upper data byte is driven when /UB is low, and the lower data byte is driven when /LB is low. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is deasserted high, the data bus will remain in a high-Z state.

Write Operation

Writes occur in the FM28V102 in the same time interval as reads. The FM28V102 supports both /CE- and /WE-controlled write cycles. In both cases, the address A(15:2) is latched on the falling edge of /CE.

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the device begins the memory cycle as a write. The FM28V102 will not drive the data bus regardless of the state of /OE as long as /WE is low. Input data must be valid when /CE is deasserted high. In a /WE-controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if /OE is low, however it will hi-Z once /WE is asserted low. The /CE- and /WE-controlled write timing cases are shown in the Electrical Specifications section.

Write access to the array begins on the falling edge of /WE after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever comes first. A valid write operation requires the user to meet the access time specification prior to deasserting /WE or /CE. Data setup time indicates the interval during which data cannot change prior to the end of the write access (rising edge of /WE or /CE).

Unlike other truly nonvolatile memory technologies, there is no write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Page Mode Operation

The F-RAM array is organized as 16,384 rows each having 64 bits. Each row has 4 column address locations. Address inputs A(1:0) define the column address to be accessed. An access can start on any column address, and other column locations may be accessed without the need to toggle the /CE pin. For fast access reads, once the first data byte is driven onto the bus, the column address inputs A(1:0) may be changed to a new value. A new data byte is then driven to the DQ pins no later than t_{AAP}, which is less than half the initial read access time. For fast access writes, the first write pulse defines the first write access. While /CE is low, a subsequent write pulse along with a new column address provides a page mode write access.

Precharge Operation

The precharge operation is an internal condition in which the state of the memory is being prepared for a new access. Precharge is user-initiated by driving the /CE signal high. It must remain high for at least the minimum precharge time t_{PC}.

Precharge is also activated by changing the upper addess A(15:2). The current row is first closed prior to accessing the new row. The device automatically detects an upper order address change which starts a precharge operation, the new address is latched, and the new read data is valid within the t_{AA} address access time. Refer to the *Read Cycle Timing 1* diagram. Likewise a similar sequence occurs for write cycles. Refer to the *Write Cycle Timing 3* diagram. The rate at which random addresses can be issued is t_{RC} and t_{WC}, respectively.

Sleep Mode

The device incorporates a sleep mode of operation which allows the user to achieve the lowest power supply current condition. It enters a low power sleep mode by asserting the /ZZ pin low. Read and write operations must complete prior to the /ZZ pin going low. Once /ZZ is low, all pins are ignored except the /ZZ pin. When /ZZ is deasserted high, there is some time delay (t_{ZZEX}) before the user can access the device.

If Sleep Mode is not used, the /ZZ pin may be floated (internal pullup) or tied to V_{DD}.

SRAM Drop-In Replacement

The FM28V102 has been designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require /CE to toggle for each new address. /CE may remain low indefinitely. While /CE is low, the device automatically detects address changes and a new access is begun. This functionality allows /CE to be grounded as you might with an SRAM. It also allows page mode operation at speeds up to 33MHz. **Note that if /CE is tied to ground, the user must be sure /WE is not low at powerup or powerdown events. If /CE and /WE are both low during power cycles, data corruption will occur. Figure 5 shows a pullup resistor on /WE which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /WE pin tracks V_{DD} yet a high enough value that the current drawn when /WE is low is not an issue. A 10Kohm resistor draws 330uA when /WE is low and V_{DD}=3.3V. Note that software write-protect is not available to the user if the chip enable pins are hardwired active.**

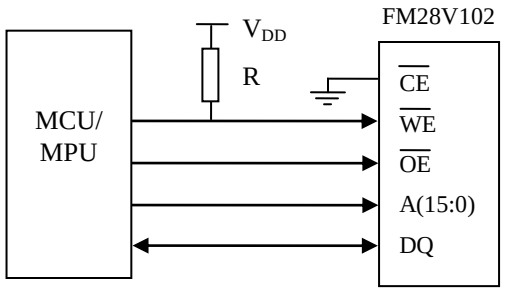


Figure 2. Use of Pullup Resistor on /WE

For applications that require the lowest power consumption, the /CE signal should be active (low) only during memory accesses. The FM28V102 draws supply current while /CE is low, even if addresses and control signals are static. While /CE is high, the device draws no more than the maximum standby current I_{SB}.

The FM28V102 is compatible with the 2Mbit FM28V202 device. There are some differences in the timing specifications. Please refer to the FM28V202 datasheet.

The /UB and /LB byte select pins are active for both read and write cycles. They may be used to allow the device to be wired as a 128Kx8 memory. The upper and lower data bytes can be tied together and controlled with the byte selects. Individual byte enables or the next higher address line A(16) may be available from the system processor.

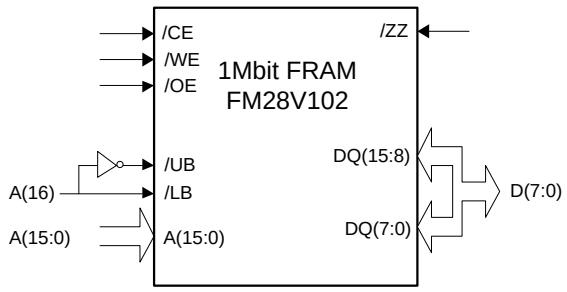


Figure 3. FM28V102 Wired as 128Kx8

PCB Layout Recommendations

A 0.1uF decoupling capacitor should be placed close to pin 11 (V_{DD}) and the ground side of the capacitor should be connected to either a ground plane or low impedance path back to pin 12 (V_{SS}). The same should be done to the other side at pins 33 and 34. This is especially important for the TSOP-II package due to the inductance of the leadframe. It is best to use a chip capacitor that has a low ESR and has good high frequency characteristics.

If the controller drives the address and chip enable from the same timing edge, it is best to keep the address routes short and of equal length. A simple RC circuit may be inserted in the chip enable path to provide some delay and timing margin for the FM28V102's address setup time t_{AS}.

As a general rule, the layout designer may need to add series termination resistors to controller outputs that have fast transitions or routes that are > 15cm in length. This is only necessary if the edge rate is less than or equal to the round trip trace delay. Signal overshoot and ringback may be large enough to cause erratic device behavior. It is best to add a 50 ohm resistor (30 – 60 ohms) near the output driver (controller) to reduce such transmission line effects.

ENDURANCE

The FM28V102 is capable of being accessed at least 10^{14} times – reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis. The F-RAM architecture is based on an array of rows and columns. Rows are defined by A15-A2 and column addresses by A1-A0. The array is organized as 16K rows of 4-words each. The entire row is internally accessed once whether a single 16-bit word or all four words are read or written. Each word in the row is counted only once in an endurance calculation.

The user may choose to write CPU instructions and run them from a certain address space. The table below shows endurance calculations for 256-byte repeating loop, which includes a starting address, 3 page mode accesses, and a CE precharge. The number of bus clocks needed to complete a 4-word transaction is 4+1 at lower bus speeds, but 5+2 at 33MHz due to initial read latency and an extra clock to satisfy the device's precharge timing constraint t_{PC}. The entire loop causes each byte to experience only one endurance cycle. F-RAM read and write endurance is virtually unlimited even at 33MHz system bus clock rate.

Table 3. Time to Reach 100 Trillion Cycles for Repeating 256-byte Loop

Bus Freq (MHz)	Bus Cycle Time (ns)	256-byte Transaction Time (µs)	Endurance Cycles/sec.	Endurance Cycles/year	Years to Reach 10^{14} Cycles
33	30	10.56	94,690	2.98×10^{12}	33.5
25	40	12.8	78,125	2.46×10^{12}	40.6
10	100	28.8	34,720	1.09×10^{12}	91.7
5	200	57.6	17,360	5.47×10^{11}	182.8

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +4.5V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +4.5V and $V_{IN} < V_{DD}+1V$
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (AEC-Q100-002 Rev. E) - Charged Device Model (AEC-Q100-011 Rev. B) - Machine Model (AEC-Q100-003 Rev. E)	 TBD TBD TBD
	Package Moisture Sensitivity Level	MSL-3

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.0V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	2.0	3.3	3.6	V	
I_{DD}	V_{DD} Supply Current		7	12	mA	1
I_{SB}	Standby Current @ T_A = 25°C @ T_A = 85°C		 120 -	 150 250	 µA µA	2
I_{ZZ}	Sleep Mode Current @ T_A = 25°C @ T_A = 85°C		 3 -	 5 8	 µA µA	3
I_{LI}	Input Leakage Current			±1	µA	4
I_{LO}	Output Leakage Current			±1	µA	4
V_{IH1}	Input High Voltage (V_{DD}=2.7V to 3.6V)	2.2		V_{DD} + 0.3	V	
V_{IH2}	Input High Voltage (V_{DD}=2.0V to 2.7V)	0.7*V_{DD}		-	V	
V_{IL1}	Input Low Voltage (V_{DD}=2.7V to 3.6V)	-0.3		0.8	V	
V_{IL2}	Input Low Voltage (V_{DD}=2.0V to 2.7V)	-0.3		0.3*V_{DD}	V	
V_{OH1}	Output High Voltage (I_{OH} = -1 mA, V_{DD}>2.7V)	2.4			V	
V_{OH2}	Output High Voltage (I_{OH} = -100 µA)	V_{DD}-0.2			V	
V_{OL1}	Output Low Voltage (I_{OL} = 2 mA, V_{DD}>2.7V)			0.4	V	
V_{OL2}	Output Low Voltage (I_{OL} = 150 µA)			0.2	V	
R_{IN}	Address Input Resistance (/ZZ) For V_{IN} = V_{IH} (min) For V_{IN} = V_{IL} (max)	 40 1			 KΩ MΩ	5

Notes

1. V_{DD} = 3.6V, /CE cycling at min. cycle time. All inputs toggling at CMOS levels (0.2V or V_{DD}-0.2V), all DQ pins unloaded.
2. V_{DD} = 3.6V, /CE at V_{DD}, All other pins are static and at CMOS levels (0.2V or V_{DD}-0.2V), /ZZ is high.
3. V_{DD} = 3.6V, /ZZ is low, all other inputs at CMOS levels (0.2V or V_{DD}-0.2V).
4. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.
5. The input pull-up circuit is stronger (>40KΩ) when the input voltage is above V_{IH} and weak (>1MΩ) when the input voltage is below V_{IL}.

Read Cycle AC Parameters (T_A = -40° C to + 85° C, unless otherwise specified)

Symbol	Parameter	V_{DD} 2.0 to 2.7V		V_{DD} 2.7 to 3.6V		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	105	-	90	-	ns	
t_{CE}	Chip Enable Access Time	-	70	-	60	ns	
t_{AA}	Address Access Time	-	105	-	90	ns	
t_{OH}	Output Hold Time	20	-	20	-	ns	
t_{AAP}	Page Mode Address Access Time	-	40	-	30	ns	
t_{OHP}	Page Mode Output Hold Time	3	-	3	-	ns	
t_{CA}	Chip Enable Active Time	70	-	60	-	ns	
t_{PC}	Precharge Time	35	-	30	-	ns	
t_{BA}	/UB, /LB Access Time	-	25	-	15	ns	
t_{AS}	Address Setup Time (to /CE low)	0	-	0	-	ns	
t_{AH}	Address Hold Time (/CE-controlled)	70	-	60	-	ns	
t_{OE}	Output Enable Access Time	-	25	-	15	ns	
t_{HZ}	Chip Enable to Output High-Z	-	15	-	10	ns	1
t_{OHZ}	Output Enable High to Output High-Z	-	15	-	10	ns	1
t_{BHZ}	/UB, /LB High to Output High-Z	-	15	-	10	ns	1

Write Cycle AC Parameters (T_A = -40° C to + 85° C, unless otherwise specified)

Symbol	Parameter	V_{DD} 2.0 to 2.7V		V_{DD} 2.7 to 3.6V		Units	Notes
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	105	-	90	-	ns	
t_{CA}	Chip Enable Active Time	70	-	60	-	ns	
t_{CW}	Chip Enable to Write Enable High	70	-	60	-	ns	
t_{PC}	Precharge Time	35	-	30	-	ns	
t_{PWC}	Page Mode Write Enable Cycle Time	40	-	30	-	ns	
t_{WP}	Write Enable Pulse Width	22	-	18	-	ns	
t_{WP2}	/UB, /LB Pulse Width	22	-	18	-	ns	
t_{WP3}	/WE Low to /UB, /LB High	22	-	18	-	ns	
t_{AS}	Address Setup Time (to /CE low)	0	-	0	-	ns	
t_{AH}	Address Hold Time (/CE-controlled)	70	-	60	-	ns	
t_{ASP}	Page Mode Address Setup Time (to /WE low)	8	-	5	-	ns	
t_{AHP}	Page Mode Address Hold Time (to /WE low)	20	-	15	-	ns	
t_{WLC}	Write Enable Low to Chip Disabled	30	-	25	-	ns	
t_{BLC}	/UB, /LB Low to Chip Disabled	30	-	25		ns	
t_{WLA}	Write Enable Low to A(15:2) Change	30	-	25	-	ns	
t_{AWH}	A(15:2) Change to Write Enable High	105	-	90	-	ns	
t_{DS}	Data Input Setup Time	20	-	15	-	ns	
t_{DH}	Data Input Hold Time	0	-	0	-	ns	
t_{WZ}	Write Enable Low to Output High Z	-	10	-	10	ns	1
t_{WX}	Write Enable High to Output Driven	8	-	5	-	ns	1
t_{BDS}	Byte Disable Setup Time (to /WE low)	8	-	5	-	ns	
t_{BDH}	Byte Disable Hold Time (to /WE high)	8	-	5	-	ns	

Notes

1. This parameter is characterized but not 100% tested.

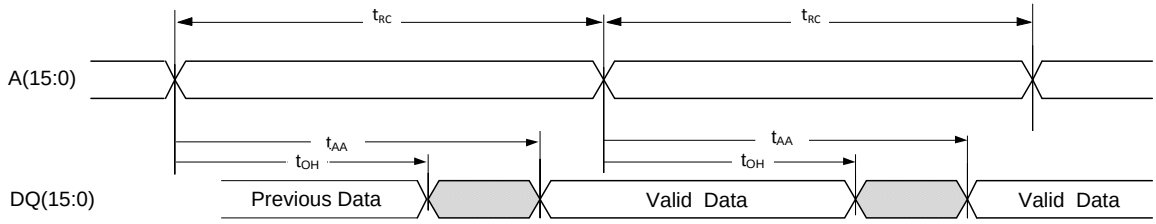
Capacitance (T_A = 25° C , f=1 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (DQ)	-	8	pF	
C_{IN}	Input Capacitance	-	6	pF	
C_{ZZ}	Input Capacitance of /ZZ pin	-	8	pF	

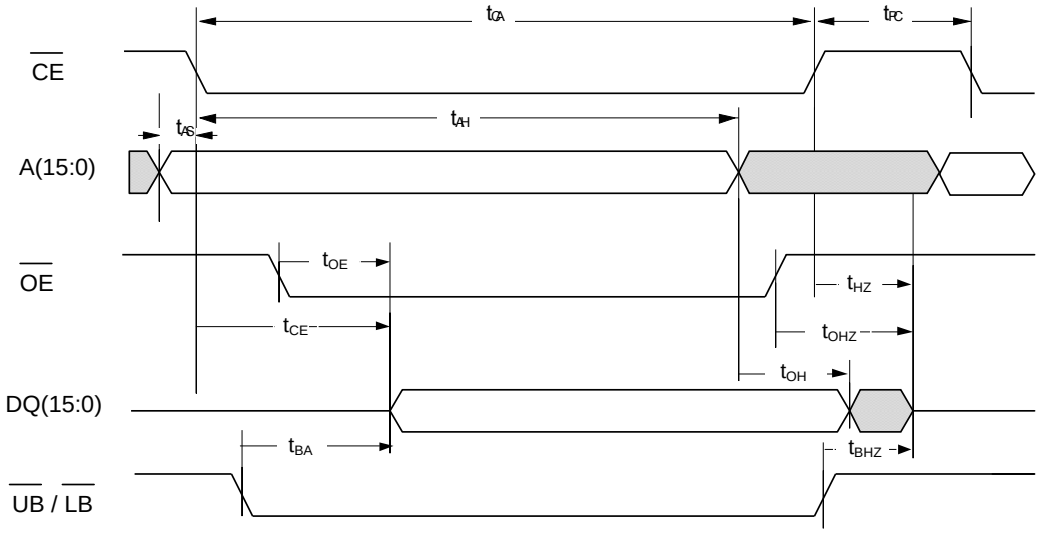
AC Test Conditions

Input Pulse Levels	0 to 3V	Input and Output Timing Levels	1.5V
Input Rise and Fall Times	3 ns	Output Load Capacitance	30pF

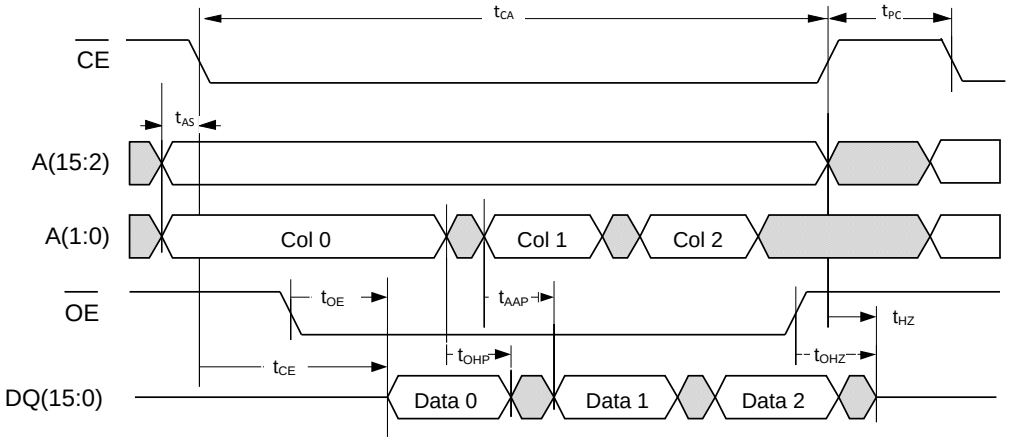
Read Cycle Timing 1 (/CE low, /OE low)



Read Cycle Timing 2 (/CE-controlled)

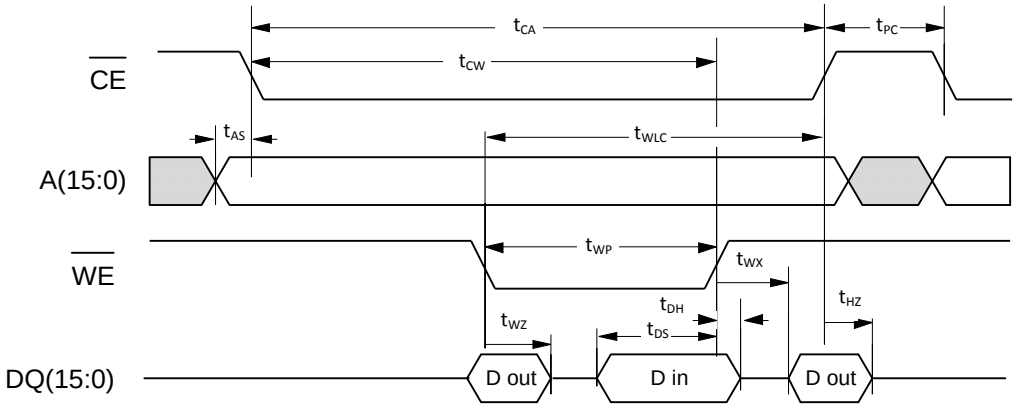


Page Mode Read Cycle Timing

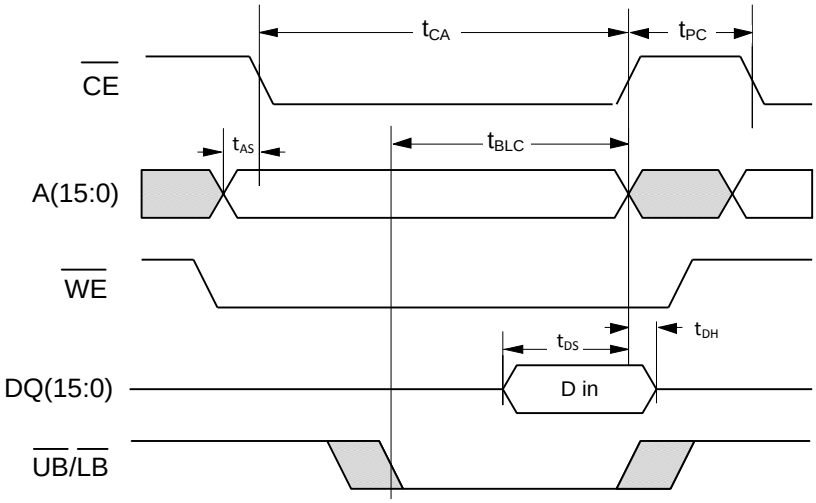


Although sequential column addressing is shown, it is not required.

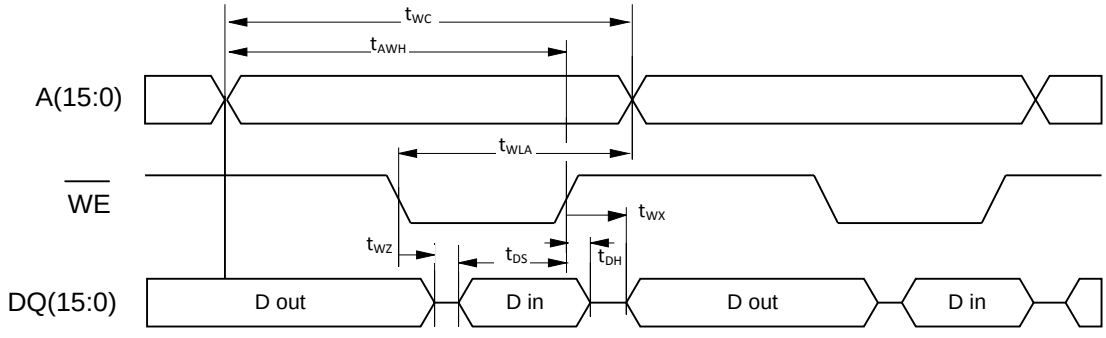
Write Cycle Timing 1 (/WE-Controlled) Note: /OE (not shown) is low only to show effect of /WE on DQ pins



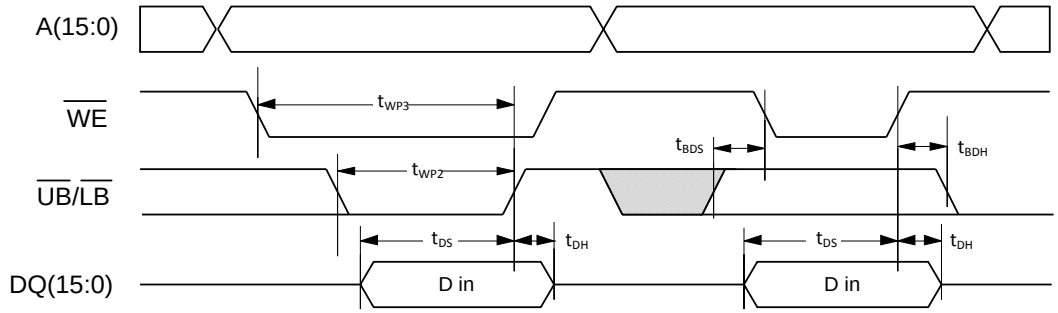
Write Cycle Timing 2 (/CE-Controlled)



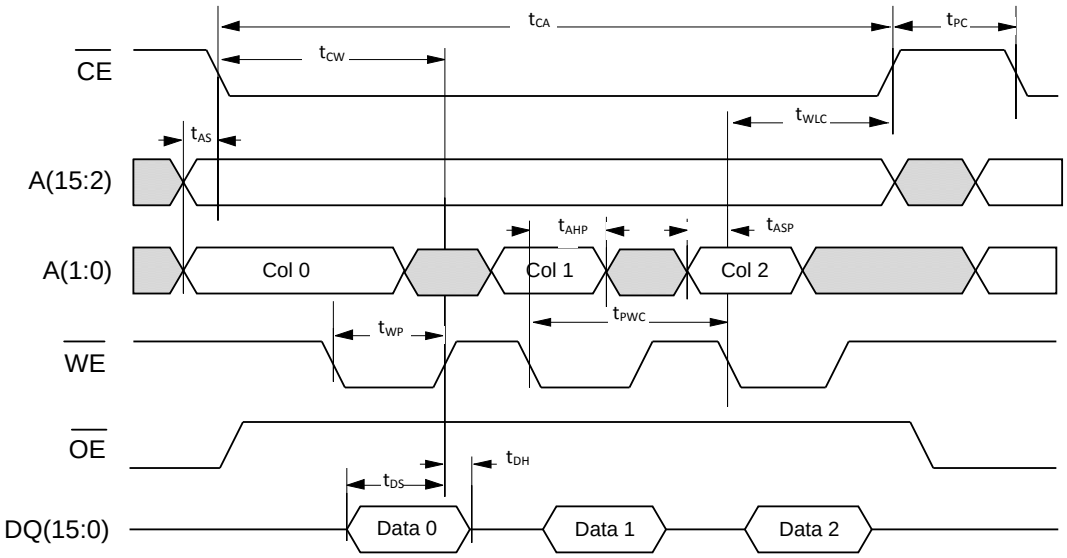
Write Cycle Timing 3 (/CE low) Note: /OE (not shown) is low only to show effect of /WE on DQ pins



Write Cycle Timing 4 (/CE low) Note: /UB and /LB to show byte enable and byte masking cases.

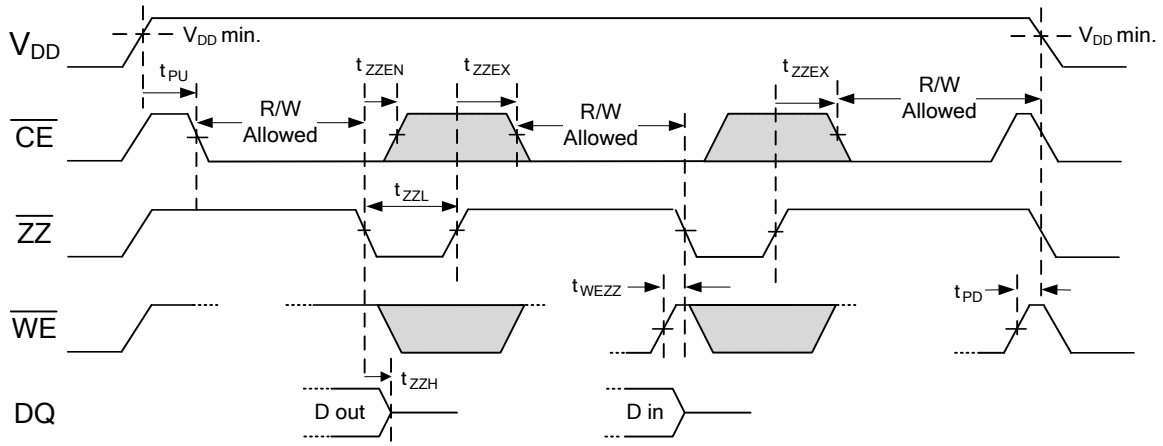


Page Mode Write Cycle Timing



Although sequential column addressing is shown, it is not required.

Power Cycle and Sleep Mode Enter/Exit Timing



Power Cycle and Sleep Mode Timing (T_A = -40° C to + 85° C, V_{DD} = 2.0V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	Power Up (after V_{DD} min. is reached) to First Access Time	1	-	ms	
t_{PD}	Last Write (/WE high) to Power Down Time	0	-	µs	
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1,2
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1,2
t_{ZZH}	/ZZ Active to DQ Hi-Z Time	-	20	ns	
t_{WEZZ}	Last Write to Sleep Mode Entry Time	0	-	µs	
t_{ZZL}	/ZZ Active Low Time	1	-	µs	
t_{ZZEN}	Sleep Mode Entry Time (/ZZ low to /CE don't care)	-	0	µs	
t_{ZZEX}	Sleep Mode Exit Time (/ZZ high to 1st access after wakeup)	-	450	µs	

Notes

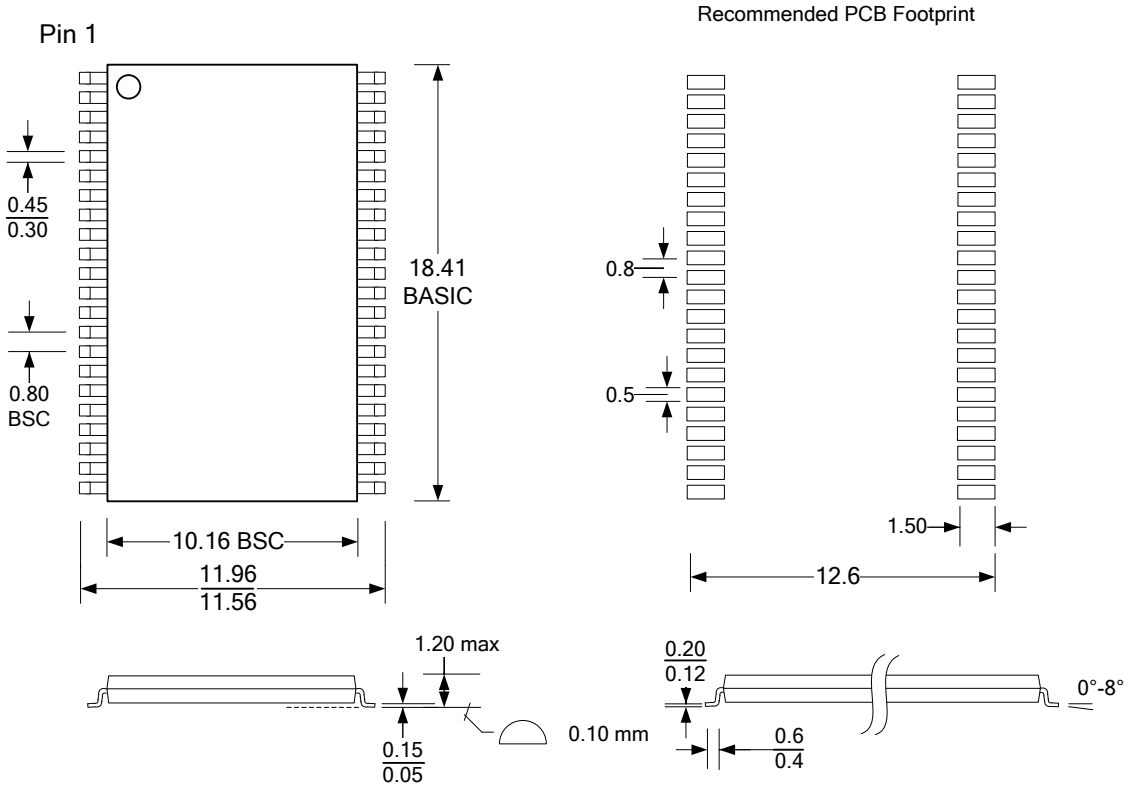
1. Slope measured at any point on V_{DD} waveform.

Data Retention (T_A = -40°C to + 85°C)

Parameter	Min	Units	Notes
Data Retention	10	Years	

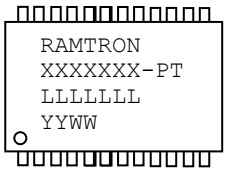
MECHANICAL DRAWING

44-pin TSOP-II (Complies with JEDEC Standard MS-024g Var. AC)



Note: All dimensions in millimeters.

TSOP-II Package Marking Scheme



Legend:
XXXXXX= part number, P=package, T=temperature (blank=ind., C=comm.)
R=rev code, LLLLLL= lot code, YY=year, WW=work week

Examples: FM28V102, "Green"/RoHS TSOP-II package,
Rev A, Lot 6340282, Year 2012, Work Week 25

```
RAMTRON
FM28V102-TG
A6340282TG
1225
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REVISION HISTORY

Revision	Date	Summary
1.0	6/12/2012	Initial release.

ORDERING INFORMATION

Part Number	Features	Operating Voltage	Operating Temp.	Package
FM28V102-TG	60 ns access, sleep mode	2.0-3.6V	-40C to +85C	44-pin “Green”/RoHS TSOP-II

Document History

Document Title: FM28V102 1Mbit (64K×16) F-RAM Memory
Document Number: 001-86601

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3930342	GVCH	03/12/2013	New Spec

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