Fast Turn-off Intelligent Controller

DESCRIPTION

The MP6902 is a Low-Drop Diode Emulator IC for Flyback converters which combined with an external switch replaces Schottky rectification diodes for high efficiency. The chip regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage becomes negative. MP6902 has a light-load sleep mode that reduces the quiescent current to <300uA.

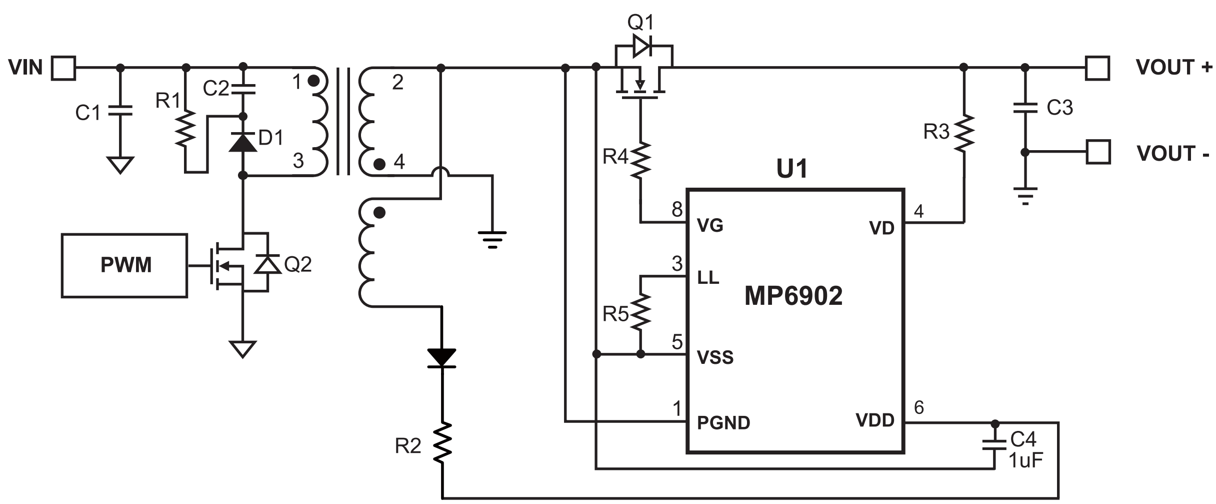
FEATURES

- Supports DCM and Quasi-Resonant Flyback Converters
- Works with 12V Standard and 5V Logic Level FETS
- Compatible with Energy Star, 1W Standby Requirements
- V_{DD} Range From 8V to 24V
- Fast Turn-off Total Delay of 20ns
- Max 400kHz Switching Frequency
- <300 μA Quiescent Current at Light Load Mode
- Supports High-side and Low-side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter

APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

TYPICAL APPLICATION

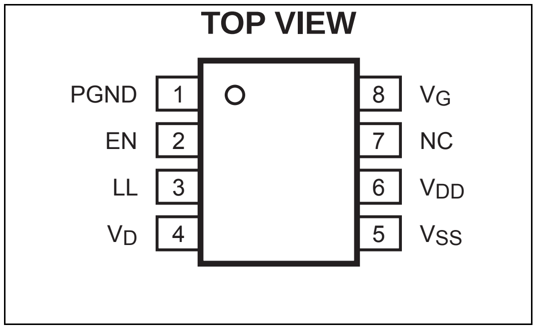


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6902DS	SOIC8	MP6902DS

* For Tape & Reel, add suffix –Z (e.g. MP6902DS–Z);
For RoHS Compliant Packaging, add suffix –LF; (e.g. MP6902DS–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} to V_{SS} ....-0.3V to +27V
PGND to V_{SS} ....-0.3V to +0.3V
V_G to V_{SS} .... -0.3V to V_{CC}
V_D to V_{SS} ....-0.7V to +180V
LL, EN to V_{SS} ....-0.3V to +6.5V
Maximum Operating Frequency............ 400 kHz
Continuous Power Dissipation (T_A=+25°C) (2)
.... 1.4W
Junction Temperature...............................150°C
Lead Temperature (Solder).......................260°C
Storage Temperature .... -55°C to +150°C

Recommended Operation Conditions (3)

V_{DD} to V_{SS}..8V to 24V
Operating Junction Temp. (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8 ....90 ...... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, T_A= +25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{DD} Voltage Range			8		24	V
V_{DD} UVLO Rising			5.0	6.0	7.0	V
V_{DD} UVLO Hysteresis			0.8	1	1.2	V
Operating Current	I_{CC}	C_{LOAD}=5nF, F_{SW}=100kHz	8		10	mA
Quiescent Current	I_q	V_{SS}-V_D=0.5V	2		3	mA
Shutdown Current		V_{DD} =4V		210	255	µA
		V_{DD}=20V, EN=0V		375	440	
Light-load Mode Current				290	380	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				30		°C
Enable UVLO Rising			1.1	1.5	1.9	V
Enable UVLO Hysteresis				0.2	0.4	V
Internal Pull-up Current On EN Pin				10	15	µA
CONTROL CIRCUITRY SECTION						
V_{SS} –V_D Forward Voltage	V_{fwd}		55	70	85	mV
Turn-on Delay	T_{Don}	C_{LOAD} = 5nF		150		ns
	T_{Don}	C_{LOAD} = 10nF		250		ns
Input Bias Current On V_D Pin		V_D = 180V			1	µA
Minimum On-time (5)	T_{MIN}	C_{LOAD} = 5nF		1.6		µs
Light-load-enter Delay	$T_{LL-Delay}$	R_{LL}=100kΩ		100		µs
Light-load-enter Pulse Width	T_{LL}	R_{LL}=100kΩ 1.3		1.75	2.2	µs
Light-load-enter Pulse Width Hysteresis	T_{LL-H} R	$_{LL}$=100kΩ		0.2		µs
Light-load Resistor Value	R_{LL}		30		300	kΩ
Light-load Mode Exit Pulse Width Threshold (V_{DS})	V_{LL-DS}		-400	-250	-150	mV
Light-load Mode Enter Pulse Width Threshold (V_{GS}) (5)	V_{LL-GS}			1.0		V
GATE DRIVER SECTION						
V_G (Low)	I	$_{LOAD}$=1mA		0.05	0.1	V
V_G (High)		V_{DD} >17V	13	14	15	V
		V_{DD} <17V	V_{DD}-2.2			
Turn-off Threshold (V_{SS}-V_D)				30		mV
Turn-off Propagation Delay		V_D=V_{SS}		15		ns
Turn-off Total Delay	T_{Doff}	V_D =V_{SS}, C_{LOAD}=5nF, R_{GATE}=0Ω	35			ns
	T_{Doff}	V_D =V_{SS}, C_{LOAD}=10nF, R_{GATE}=0Ω	45			ns
Pull Down Impedance				1	2	Ω
Pull Down Current (5)		3V <V_G<10V		2		A

Notes:

5) Guaranteed by Design and Characterization.

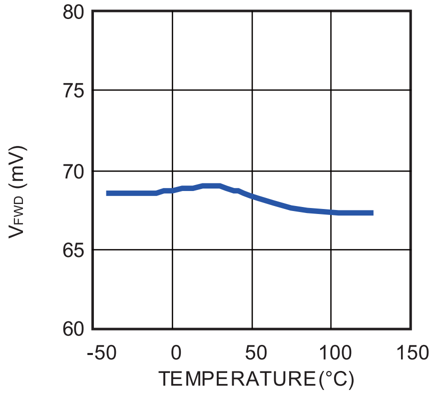
PIN FUNCTIONS

Pin #	Name	Description
1	PGND	Power Ground, return for driver switch
2	EN	Enable pin, active high
3	LL	Light load timing setting. Connect a resistor to set the light load timing.
4	VD	FET drain voltage sense
5	VSS	Ground, also used as reference for VD
6 VDD		Supply Voltage
7 NC		No connection
8	VG	Gate drive output

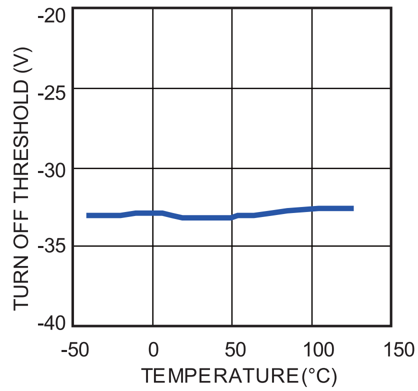
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, unless otherwise noted.

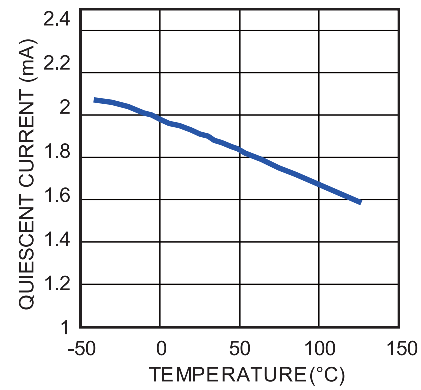
V_{FWD} vs. Temperature



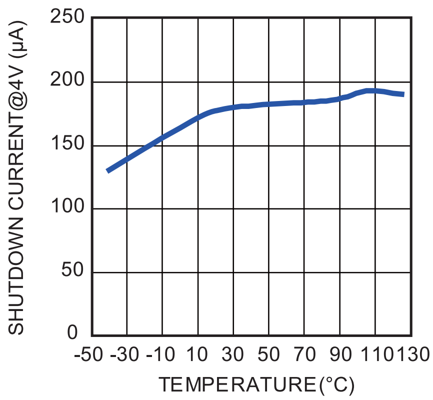
Turn off threshold vs. Temperature



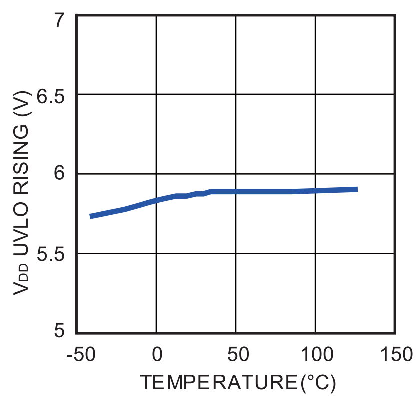
Quiescent Current vs. Temperature



Shutdown Current vs. Temperature

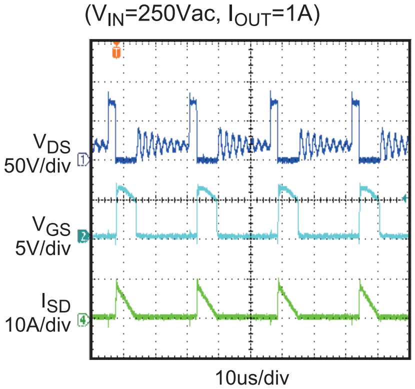


V_{DD} UVLO Rising vs. Temperature



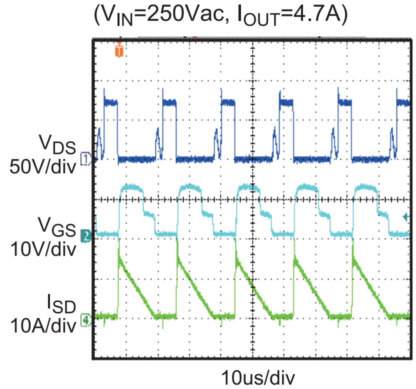
Operation in 90W Flyback Application

(V_{IN}=250Vac, I_{OUT}=1A)



Operation in 90W Flyback Application

(V_{IN}=250Vac, I_{OUT}=4.7A)



Notes:

6) See Figure 13 for the test circuit.

BLOCK DIAGRAM

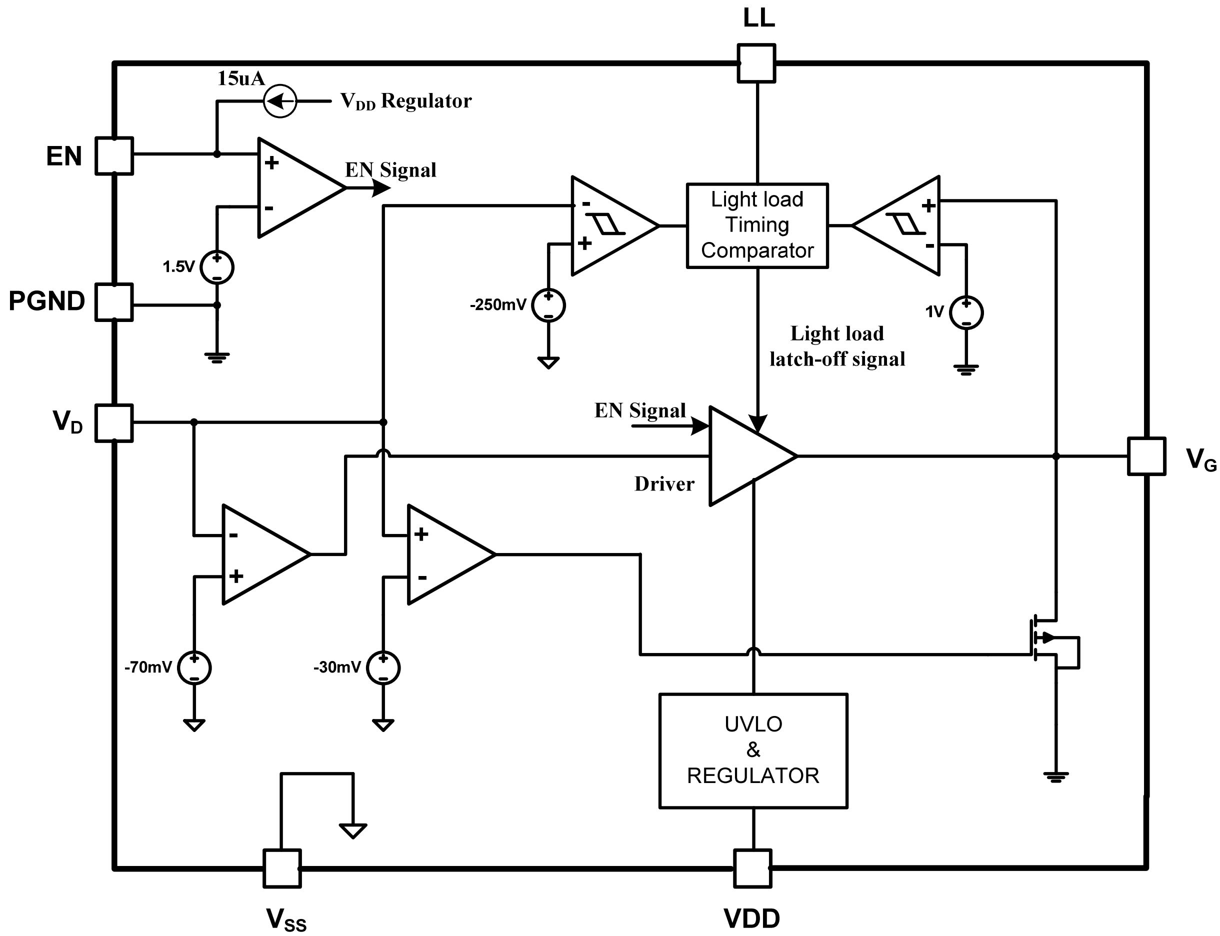


Figure 1—Function Block Diagram

OPERATION

The MP690 2 supports operation in DCM an d Quasi-Resonant Flyback converters. The control circuitry con trols the gate in forward mode an d will turn the gate off when the MOSFET current is fairly low.

Blanking

The control circuitry contains a blanking function. When it pulls the MOSF ET on/off, it makes sur e that the on/ off state at least last s for some time. The turn o n blanking time is ~ 1.6us, which determines the minimum on-time. During the turn on blanking period, the turn off threshold is n ot totally blan ked, but changes t he thresho ld voltage to ~+50mV (i nstead of -30mV). Th is assures tha t the part can always be turned off even during the turn on blanking p eriod. (Albeit slower)

VD Clamp

Because V_D can go a s high as 180V, a Hig h-Voltage JF ET is u sed at the inp ut. To avoid excessive currents when Vg goes b elow -0.7V, a small resist or is re commended between V_D and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When the VDD is below UVLO threshold, the part is in sleep mode and the Vg pin is pulled low by a 10kΩ resistor.

Enable pin

If EN is pulled low, the part is in sleep mode.

Thermal shutdown

If the junction temperat ure of the chip exceeds 170°C, the Vg will be pulled low and the par t stops switching. The part will return to normal function af ter the jun ction temp erature ha s dropped to 120°C.

Thermal Design

If the dissipation of t he chip is higher than 100mW du e to switching frequencies above 100kHz.

Turn-on Phase

When the synchronous MOSFET i s conductin g, current will flow throu gh its body diode which generates a negative Vds across it. Because this body diode voltage drop (<-500mV) is much smaller than the turn on threshold of the control circuitry (-70mV), whic h will then pull the gat e driver volta ge high to turn on the synchronous MOSFET after about 150ns tu rn on delay (Defined in Figure 2).

As soon a s the turn on threshold (-70mV) is triggered, a blanking t ime (Minimum on-time : ~1.6us) will be added during which the turn off threshold will be changed from -30mV to +50mV. This blanking time can help to avoid error trigger on turn off threshold caused by the turn on ringing of the synchronous MOSFET.

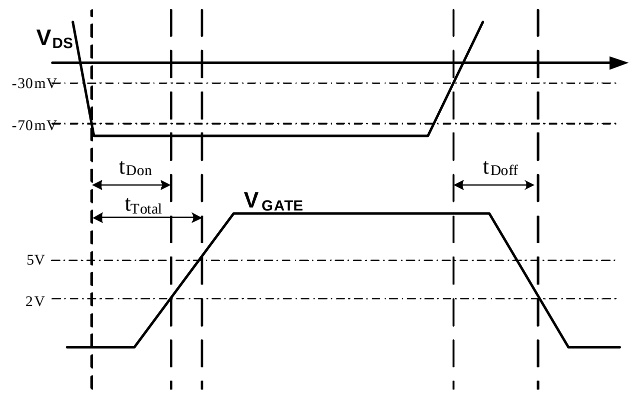


Figure 2—Turn on and Turn off delay

Conducting Phase

When the synchronous MOSFET is turned on, Vds beco mes to rise according to its on resistance, as soon as Vds rises a bove the turn on threshold (-70mV), the control circuitry sto ps pulling up t he gate dr iver which l eads the g ate voltage is p ulled down by the inter nal pull-down resistance (10kΩ) to larger the on resistance of synchronous MOSFET to ease th e rise of V ds. By doing that, Vds is adjusted to be around -70mV even when the current through the MOS is fairly small, this function can ma ke the driver voltage fairly low when the synchronous MOSFET is turned off to fast t he turn off sp eed (this function is still active during turn on blanking time which means the gate driver could still b e turned off even with very s mall duty of the synchronous MOSFET).

Turn-off Phase

When Vds rises to trigger the turn off threshold (-30mV), the gate voltage is pulled to low after about 20ns turn off delay (defined in Figure 2) by the control circuitry. Similar with turn-on phase, a 200ns blanking time is added after the synchronous MOSFET is turned off to avoid error trigger.

Figure 3 shows synchronous rectification operation at heavy load condition. Due to the high current, the gate driver will be saturated at first, during which the gate driver voltage is kept at ~2V lower than V_{DD} (when V_{DD}>16V, gate driver will be internal clamped at 14V). After Vds goes to above -70mV, gate driver voltage decreases to adjust the Vds to typical -70mV.

Figure 4 shows synchronous rectification operation at light load condition. Due to the low current, the gate driver voltage never saturates but begins to decrease as soon as the synchronous MOSFET is turned on and adjust the Vds.

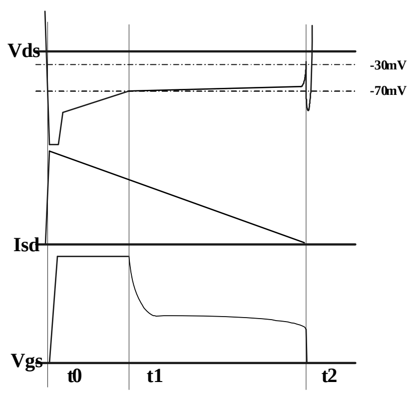


Figure 3—Synchronous Rectification Operation at heavy load

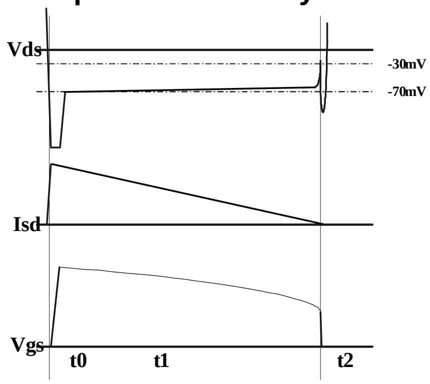


Figure 4—Synchronous Rectification Operation at light load

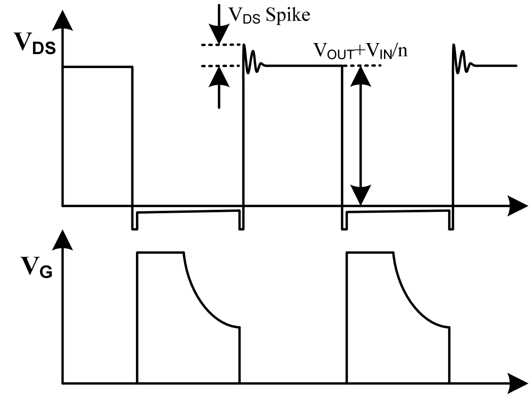


Figure 5—Drain-Source and Gate Driver voltage on SR MOFET

Figure 5 shows the whole synchronous rectification waveform on drain-source voltage V_{DS} and gate driver signal V_{GS}. For safe operation of the IC, it is required:

$$V_{OUT} + V_{IN} / n + V_{DS\_Spike} < 180V * k$$

Where 180V is the maximum voltage rating on V_D pin of MP6902, V_{IN}/V_{OUT} is the input/output DC voltage, n is the turn ratio from primary to secondary of the power transformer, V_{DS_Spike} is the spike voltage on drain-source which is lead by leakage inductance, while k is the de-rating factor which is usually selected as 0.7~0.8.

Light-load Latch-off Function

The gate driver of MP6902 is latched to save the driver loss at light-load condition to improve efficiency. When the synchronous MOSFET's conducting period keeps lower than light load timing (T_{LL}) for longer than the light-load-enter delay ($T_{LL-Delay}$), MP6902 enters light-load mode and latches off the gate driver. Here the synchronous MOSFET's conducting period is from turn on of the gate driver to the moment when V_{GS} drops to below 1V (V_{LL_GS}). During light-load mode, MP6902 monitors the synchronous MOSFET's body diode conducting period by sensing the time duration of the V_{DS} below -250mV(V_{LL_DS}). If it is longer than T_{LL}+T_{LL-H} (T_{LL-H}, light-load-enter pulse width hysteresis), the light-load mode is finished and gate driver of MP6902 is unlatched to restart the synchronous rectification.

For MP6902, the light load enter timing (T_{LL}) is programmable by connecting a resistor (R_{LL}) on LL pin, by monitoring the LL pin current (the LL pin voltage keeps at ~2V internally), T_{LL} is set as following:

$$T_{LL} \approx R_{LL}(k\Omega) \cdot \frac{2.2\mu s}{100k\Omega}$$

SR MOSFET Selection and Driver Ability

The Power Mosfet selection proved to be a trade off between Ron and Qg. In order to achieve high efficiency, the Mosfet with smaller Ron is always preferred, while the Qg is usually larger with smaller Ron, which makes the turn-on/off speed lower and lead to larger power loss. For MP6902, because Vds is regulated at ~-70mV during the driving period, the Mosfet with too small Ron is not recommend, because the gate driver may be pulled down to a fairly low level with too small Ron when the Mosfet current is still fairly high, which make the advantage of the low Ron inconspicuous.

Figure 6 shows the typical waveform of QR flyback. Assume 50% duty cycle and the output current is I_{OUT}.

To achieve fairly high usage of the Mosfet's Ron, it is expected that the Mosfet be fully turned on at least 50% of the SR conduction period:

$$Vds = -Ic \times Ron = -2 \cdot I_{OUT} \times Ron \le -Vfwd$$

Where V_{ds} is Drain-Source voltage of the Mosfet and V_{fwd} is the forward voltage threshold of MP6902, which is ~70mV.

So the Mosfet's Ron is recommended to be no lower than ~35/I_{OUT} (mΩ). (For example, for 5A application, the Ron of the Mosfet is recommended to be no lower than 7mΩ)

Figure 7 shows the corresponding total delay during turn-on period (t_{Total}, see Figure 2) with driving different Qg Mosfet by MP6902. From Figure 7, with driving a 120nC Qg Mosfet, the driver ability of MP6902 is able to pull up the gate driver voltage of the Mosfet to ~5V in 300ns as soon as the body diode of the Mosfet is conducting, which greatly save the turn-on power loss in the Mosfet's body diode.

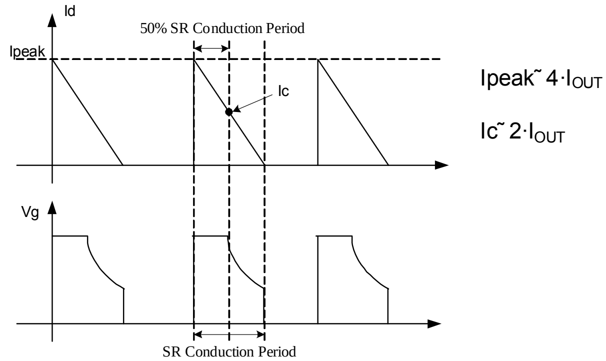


Figure 6—Synchronous Rectification typical waveforms in QR Flyback

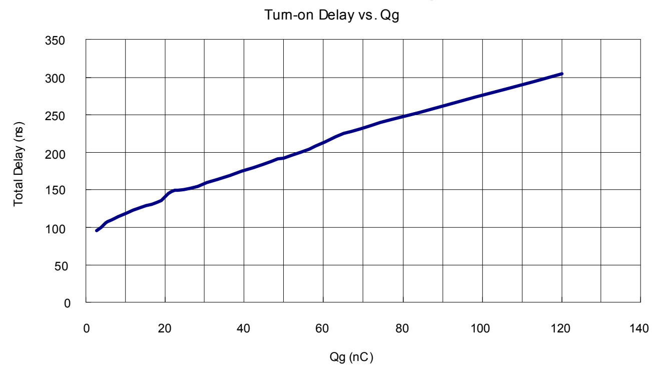


Figure 7—Total Turn-on Delay vs. Qg

Typical System Implementations

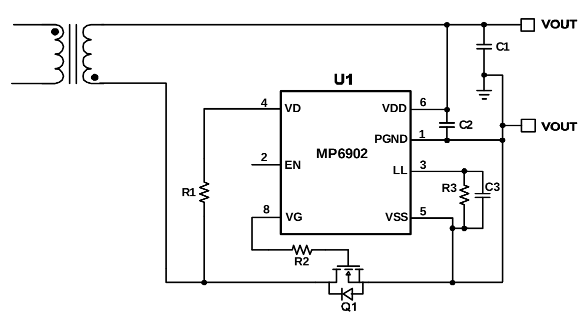


Figure 8— IC Supply derived directly from Output Voltage

Figure 8 shows the typical system implementation for the IC supply derived from output voltage, which is available in low-side rectification and the output voltage is recommended to be in the V_{DD} range of MP6902 (from 8V to 24V).

If output voltage is out of the V_{DD} range of MP6902 or high-side rectification is used, it is recommended to use an auxiliary winding from the power transformer for the IC supply, which is shown in Figure 9 and Figure.10.

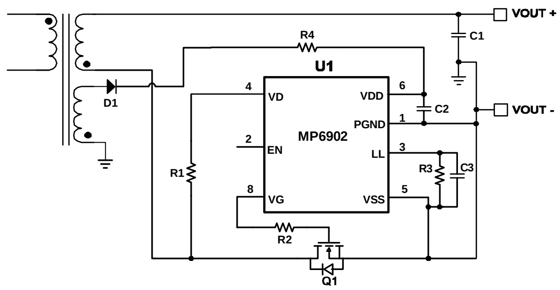


Figure 9— IC Supply derived from Auxiliary Winding in Low-Side Rectification

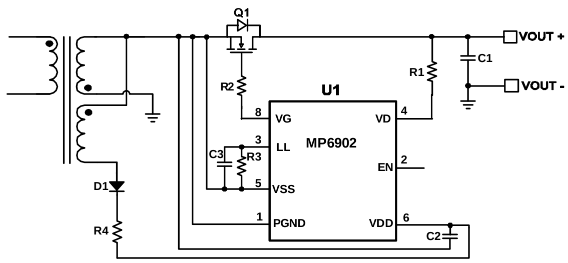


Figure 10— IC Supply derived from Auxiliary Winding in High-Side Rectification

There is another non-auxiliary winding solution for the IC supply, which uses an external LDO circuit from the secondary transformer winding. See Figure.11 and Figure.12, compared with using auxiliary winding for IC supply, this solution has a bit higher power loss which is dissipate on the LDO circuit especially when the secondary winding voltage is high.

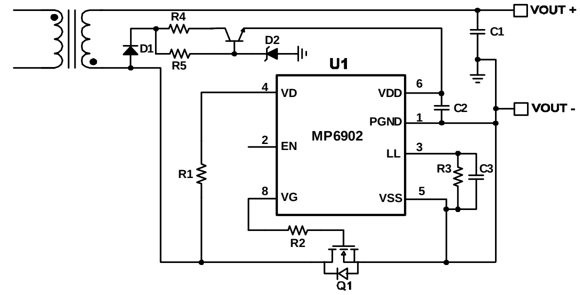


Figure 11— IC Supply derived from Secondary Winding through External LDO in Low-Side Rectification

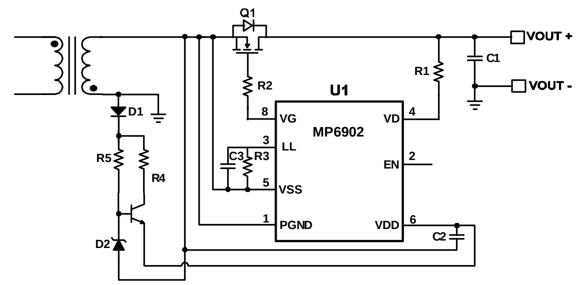


Figure 12— IC Supply derived from Secondary Winding through External LDO in High-Side Rectification

TYPICAL APPLICATION CIRCUIT

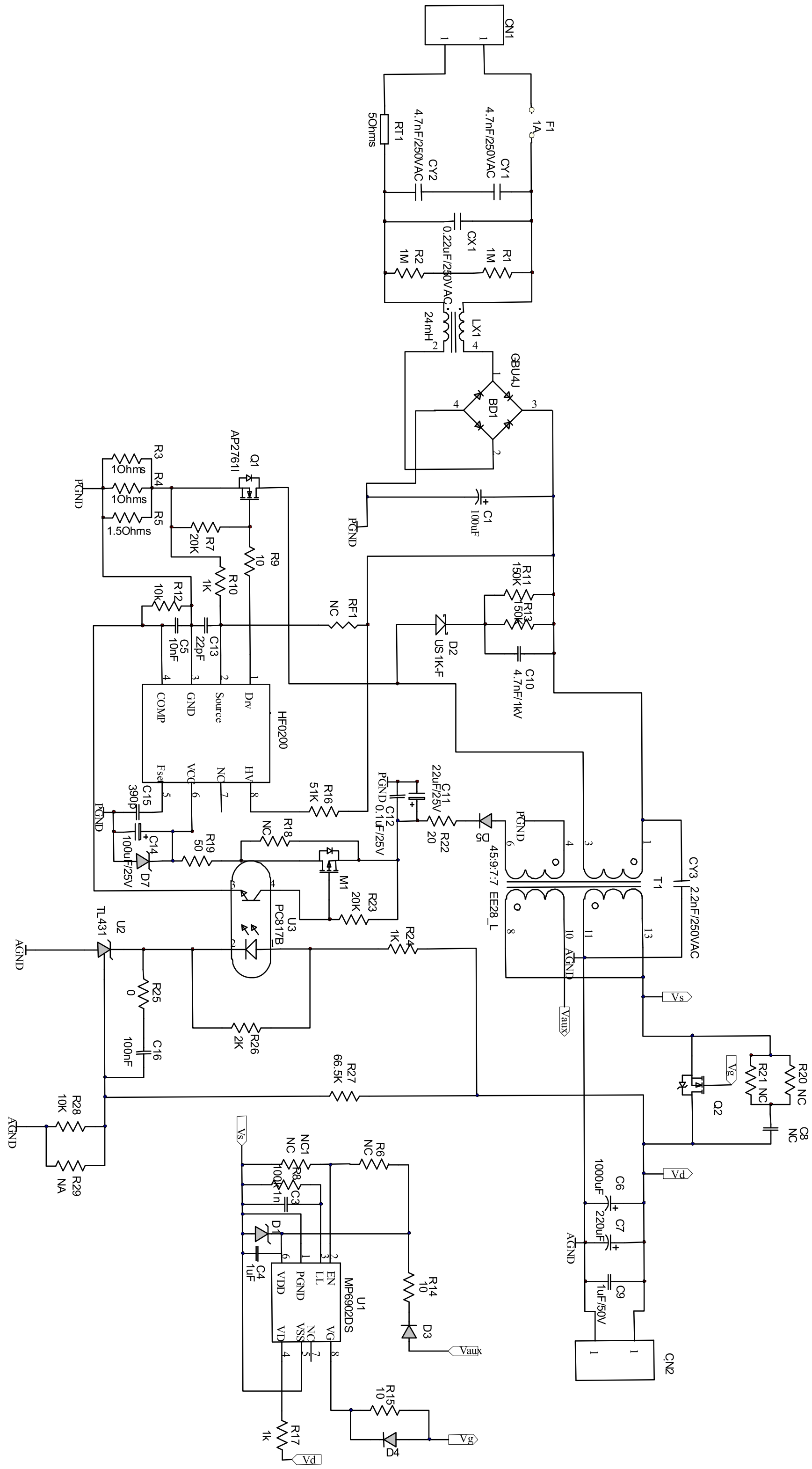
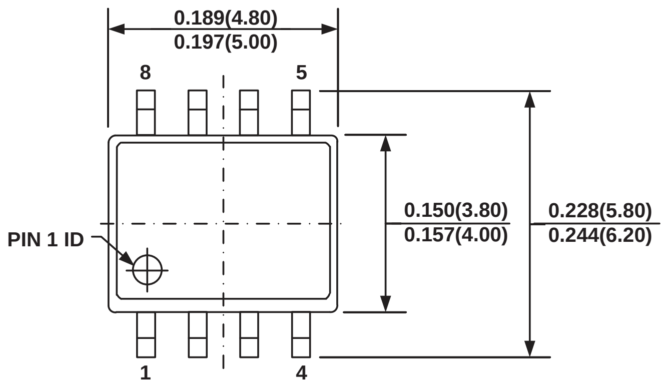


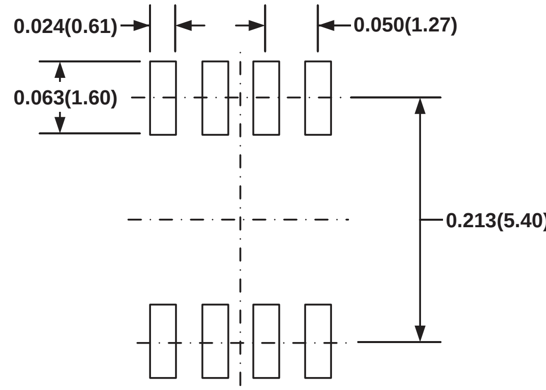
Figure 13—MP6902 for Secondary Synchronous Controller in 90W Flyback Application

PACKAGE INFORMATION

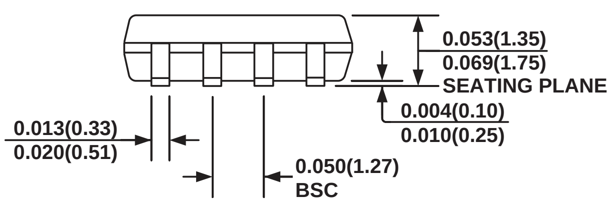
SOIC8



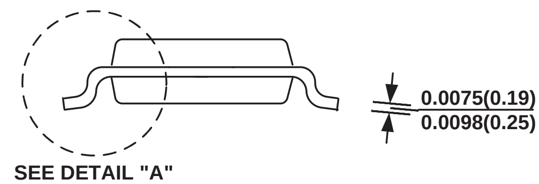
TOP VIEW



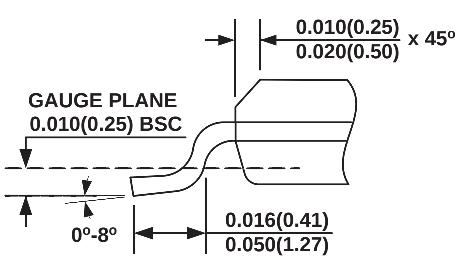
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.