NCP1030

Product Preview

Bias Regulator with On Chip Power Switch

The NCP1030 is a high voltage monolithic switching regulator with on chip Power Switch and active Start–up Circuits. The NCP1030 integrates all the components necessary for implementing high efficiency Voltage–Mode controlled DC–DC converters. It can be easily configured for either primary or secondary side regulation applications, such as a low power boost converter or a secondary side controlled bias regulator. It is designed to operate from a 48 V supply, typically found in telecommunication systems.

The NCP1030 fixed frequency oscillator is designed to operate up to 1 MHz and is capable of external frequency synchronization, providing additional design flexibility. A minimum number of external components are required to set the oscillator frequency, loop compensation and the line under/over lockout thresholds. The NCP1030 is available in the space saving S0–8 and Micro 8 packages, making it a space efficient and cost saving solution.

Features

- On Chip High 200 V Power Switch Circuit and Startup Circuit
- External Frequency Synchronization up to 1 MHz
- Internal Startup Regulator with Auxiliary Winding Override
- Trimmed ±2% Internal Reference
- Line Under/Over Voltage Lockout
- Cycle by Cycle Current Limit
- Over Temperature Protection
- Internal Error Amplifier
- Primary or Secondary Regulation

Typical Applications

- Secondary Bias Supply for Isolated DC – DC Converters
- Stand Alone Low Power DC – DC Converter
- Low Power Boost Converter

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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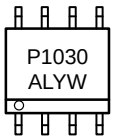
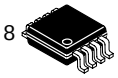
MARKING DIAGRAMS

SCALE 1:1

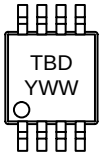
S0–8
D SUFFIX
CASE 751





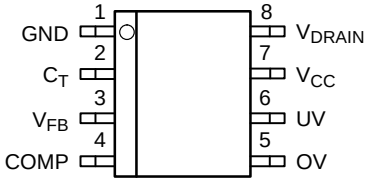
SCALE 2:1

Micro 8
DM SUFFIX
CASE 846A



A = Assembly Location
L = Wafer Lot
Y = Year
WW, W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP1030DR2	S0–8	2500/Tape & Reel
NCP1030DMR2	Micro–8	2500/Tape & Reel

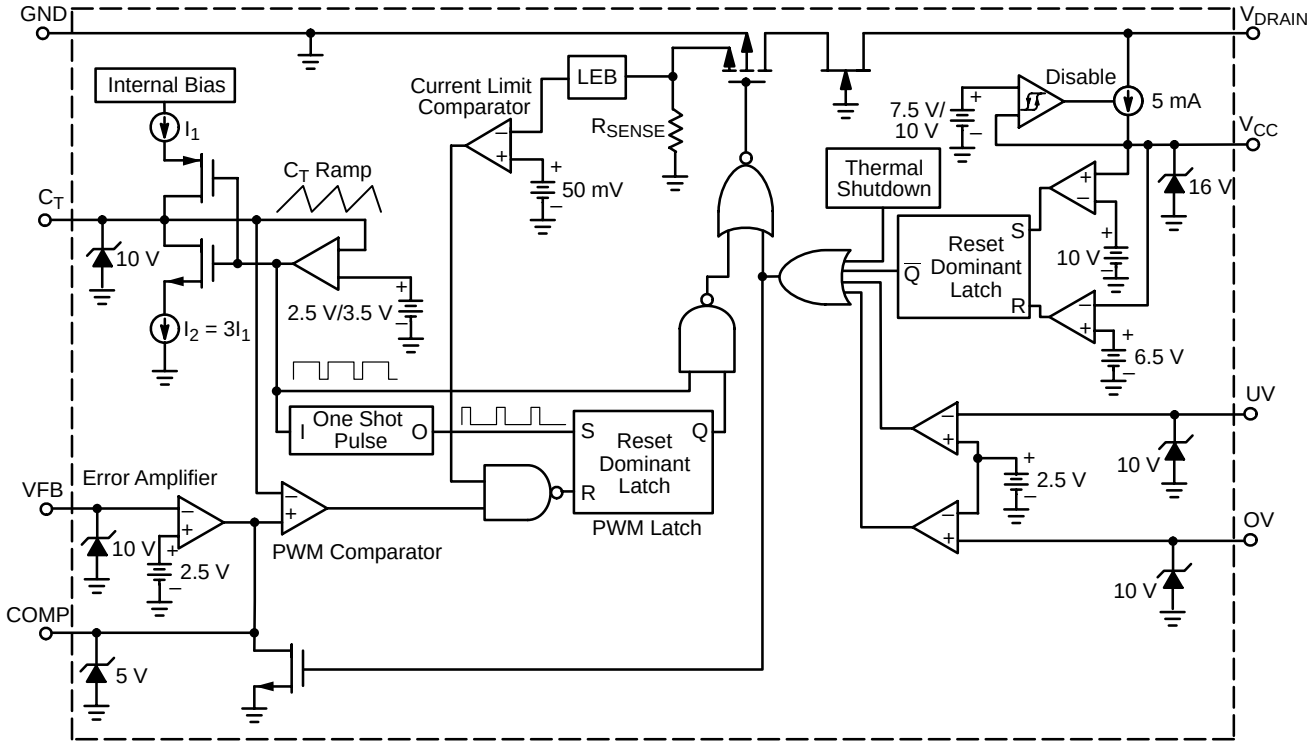


Figure 1. NCP1030 Functional Block Diagram

Functional Pin Description

Pin	Name	Function	Description
1	GND	Ground	Ground reference pin for the circuit.
2	C_T	Oscillator Frequency Selection	An external capacitor connected to this pin sets the oscillator frequency up to 1 MHz. The oscillator can be synchronized to a higher frequency by charging or discharging C_T to trip the internal 2.5 V/3.5 V comparator.
3	V_{FB}	Feedback Input	The regulated voltage is scaled down to 2.5 V by means of a resistor divider. Regulation is then achieved comparing the scaled regulated voltage to an internal 2.5 V reference.
4	COMP	Error Amplifier Compensation	Requires external compensation network between COMP and V_{FB} pins.
5	OV	Line Overvoltage Shutdown	Line voltage (V_{in}) is scaled down using an external resistor divider such that the OV voltage reaches 2.5 V when line voltage reaches its maximum voltage.
6	UV	Line Undervoltage Shutdown	Line voltage is scaled down using an external resistor divider such that the UV voltage reaches 2.5 V when line voltage reaches its minimum voltage.
7	V_{CC}	Supply Voltage	This pin is connected to an external capacitor for energy storage. During Turn–On, the startup circuit sources current to initially charge the capacitor connected to this pin. When the supply voltage reaches $V_{CC(on)}$, the startup circuit turns off and the power switch is enabled. An external winding can be used to supply power after initial startup. V_{CC} should not exceed 16 V.
8	V_{DRAIN}	Power Switch and Startup Circuits	This pin connects directly to one of the transformer windings. The internal High Voltage Power Switch Circuit is connected between this pin and ground. Also, this pin internally connects the Power Switch and Startup Circuits.

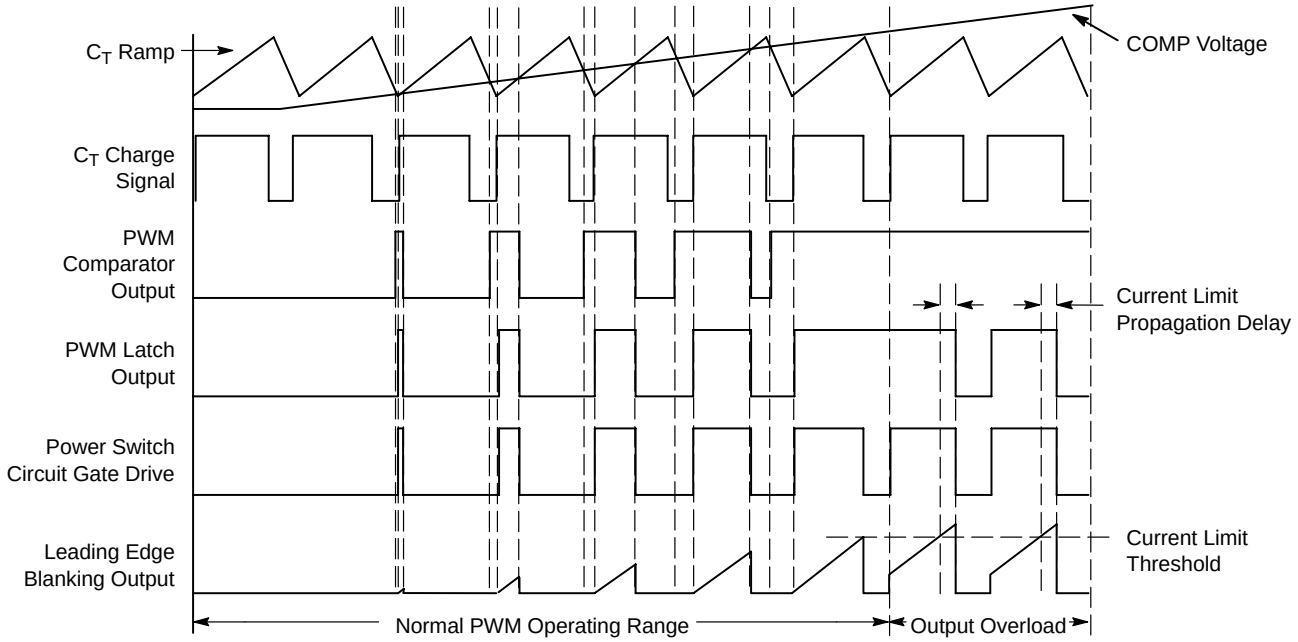


Figure 2. Pulse Width Modulation Timing Diagram

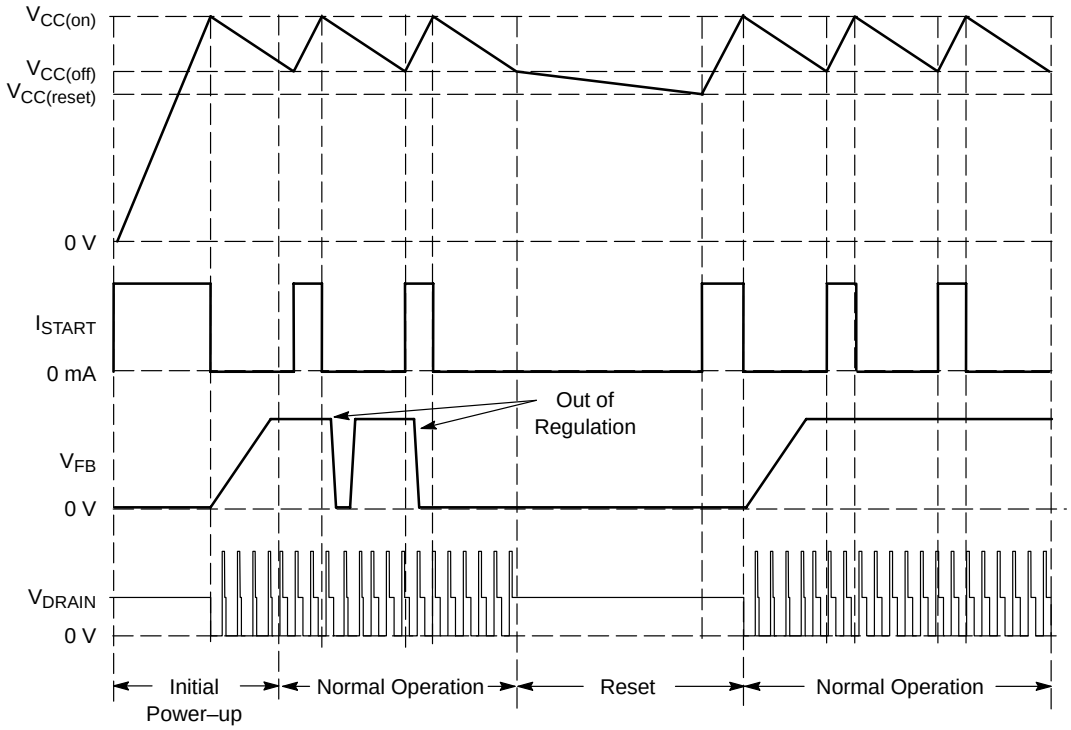


Figure 3. Dynamic Self Supply with Fault Condition Timing Diagram

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Switch and Startup Circuit Voltage	V_{DRAIN}	–0.3 to 200	V
COMP Voltage Range	V_{COMP}	–0.3 to 5	V
All Other Inputs/Outputs Voltage Range	V_{IO}	–0.3 to 10	V
V_{CC} Voltage Range	V_{CC}	–0.3 to 16	V
Operating Junction Temperature	T_J	–40 to 125	°C
Storage Temperature	T_{stg}	–55 to 150	°C
Power Dissipation (T_J = 25°C) D Suffix, Plastic Package Case 751 DM Suffix, Plastic Package Case 846A		 TBD TBD	W
Thermal Resistance D Suffix, Plastic Package Case 751 Junction to Case Junction to Air, 2.0 Oz. Printed Circuit Copper Clad 0.36 Sq. Inch 1.0 Sq. Inch DM Suffix, Plastic Package Case 846A Junction to Case Junction to Air, 2.0 Oz. Printed Circuit Copper Clad 0.36 Sq. Inch 1.0 Sq. Inch	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ 	 TBD TBD TBD TBD TBD TBD	°C/W

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
   A. This device contains ESD protection circuitry and exceeds the following tests:
      Pins 1–7: Human Body Model 2000V per MIL–STD–883, Method 3015.
      Machine Model Method 100 V.
      Pin 8 is connected to the High Voltage Start–up and Power Switch circuits and rated only to the maximum voltage rating of the part, or 200 V.
   B. This device contains Latch–up protection and exceeds ±XX mA per JEDEC Standard JESD78.

DC ELECTRICAL CHARACTERISTICS (V_{DRAIN} = 48 V, V_{CC} = 12 V, C_T = 560 pF, V_{UV} = 3 V, V_{OV} = 2 V, V_{FB} = 2.3 V, T_J = –40°C to 125°C, typical values shown are for T_J = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
START–UP CONTROL					
Start–up Circuit Output Current (V_{FB} = V_{COMP}) V_{CC} = 0 V V_{CC} = $V_{CC(on)}$ – 0.2 V	I_{START}	 5.0 5.0	 TBD TBD	 TBD TBD	mA
V_{CC} Supply Monitor (V_{FB} = 2.7 V) Start–Up Threshold Voltage (V_{CC} Increasing) Minimum Operating V_{CC} After Turn–on (V_{CC} Increasing) Hysteresis Voltage	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(hys)}$	 9.5 7.0 –	 10.0 7.5 2.5	 10.5 8.0 –	V
Undervoltage Lockout Threshold Voltage, V_{CC} Decreasing (V_{FB} = V_{COMP})	$V_{CC(reset)}$	TBD	6.5	TBD	V
ERROR AMPLIFIER					
Reference Voltage (V_{COMP} = V_{FB}, Follower Mode) T_J = 25°C T_J = –40°C to 125°C	V_{REF}	 TBD TBD	 2.5 2.5	 TBD TBD	V
Line Regulation (V_{CC} = 7.5 V to 10 V, T_J = 25°C)	REG_{LINE}	–	1.0	TBD	mV
Input Bias Current (V_{FB} = 0 V to 2.7 V)	I_{VFB}	–	0.1	1.0	μA
Comp Source Current (V_{COMP} = 2.5 V, V_{FB} = 2.3 V)	I_{SRC}	50	100	150	μA
Comp Sink Current (V_{COMP} = 2.5 V, V_{FB} = 2.7 V)	I_{SNK}	500	–	TBD	μA
Comp Maximum Voltage (I_{SRC} = 100 μA)	$V_{C(max)}$	5.0	–	–	V
Comp Minimum Voltage (I_{SNK} = 100 μA, V_{FB} = 2.7 V)	$V_{C(min)}$	–	–	1.0	V
Open Loop Voltage Gain	A_{VOL}	–	80	–	dB
Gain Bandwidth Product	GBW	–	1.0	–	MHz

DC ELECTRICAL CHARACTERISTICS (V_{DRAIN} = 48 V, V_{CC} = 12 V, C_T = 560 pF, V_{UV} = 3 V, V_{OV} = 2 V, V_{FB} = 2.3 V, T_J = –40°C to 125°C, typical values shown are for T_J = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LINE OV/UV LIMITER					
Undervoltage Lockout (V_{FB} = V_{COMP})					
Voltage Threshold (V_{in} Increasing)	V_{UV}	2.4	2.5	2.6	V
Voltage Hysteresis	$V_{UV(hys)}$	0.100	0.150	0.200	V
Input Bias Current	I_{UV}	–	0.1	1.0	μA
Overvoltage Lockout (V_{FB} = V_{COMP})					
Voltage Threshold (V_{in} Increasing)	V_{OV}	2.4	2.5	2.6	V
Voltage Hysteresis	$V_{OV(hys)}$	0.100	0.150	0.200	V
Input Bias Current	I_{OV}	–	0.1	1.0	μA
OSCILLATOR					
Frequency (C_T = 560 pF)	f_{OSC1}				kHz
T_J = 25°C		285	300	315	
T_J = –40°C to 125°C		TBD	TBD	TBD	
Frequency (C_T = 100 pF)	f_{OSC2}				kHz
T_J = 25°C		TBD	1000	TBD	
T_J = –40°C to 125°C		TBD	TBD	TBD	
Externally Synchronized Frequency (Note 2)	f_{SYNC}	f_{OSC}	–	TBD	kHz
PWM COMPARATOR					
PWM Duty Cycle (Maximum)	DC_{MAX}	TBD	75	TBD	%
PWM Ramp					V
Peak	Vrpk	–	3.5	–	
Valley	Vrvly	–	2.5	–	
POWER SWITCH CIRCUIT					
Power Switch Circuit On–State Resistance (I_D = 100 mA)	$R_{DS(on)}$				Ω
T_J = 25°C		–	6	TBD	
T_J = 125°C		–	TBD	10	
Power Switch Circuit and Startup Circuit Breakdown Voltage (I_D = 100 μA, T_J = 25°C)	$V_{(BR)DS}$	200	–	–	V
Power Switch Circuit and Startup Circuit Off–State Leakage Current (V_{DRAIN} = 200 V, V_{UV} = 2.0 V)	$I_{DS(off)}$				μA
T_J = 25°C		–	TBD	50	
T_J = 125°C		–	TBD	TBD	
Switching Characteristics (V_{DS} = TBD, R_L = TBD)					ns
Rise Time	t_r	–	50	–	
Fall Time	t_f	–	50	–	
CURRENT LIMIT AND OVER TEMPERATURE PROTECTION					
Current Limit Threshold (T_J = 25°C, di/dt = X)	I_{LIM}	TBD	0.5	TBD	A
Propagation Delay, Current Limit Threshold to Power Switch Circuit Output R_L = TBD (Leading Edge Blanking plus Current Limit Delay)	t_{PLH}	–	100	TBD	ns
Thermal Protection (Note 3)					°C
Shutdown Threshold (T_J Increasing)	T_{SHDN}	125	150	–	
Hysteresis	T_{HYS}	–	25	–	
TOTAL DEVICE					
Power Supply Current After UV Turn–On					mA
Power Switch Enabled	I_{CC1}	1.0	TBD	2.0	
Power Switch Disabled					
Non–Fault condition (V_{FB} = 2.7 V)	I_{CC2}	–	1.5	2.0	
Fault Condition (V_{FB} = 2.7 V, V_{UV} = 2.0 V)	I_{CC3}	–	0.7	1.0	

2. Oscillator frequency can be externally synchronized to the maximum frequency of the device.
3. Guaranteed by design only.

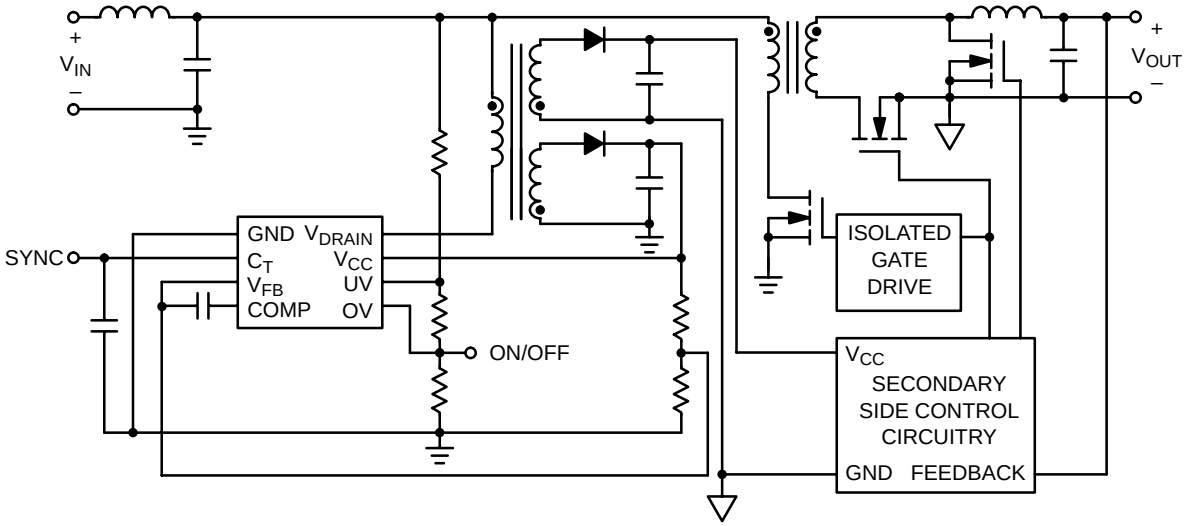


Figure 4. Secondary Side Bias Supply Configuration

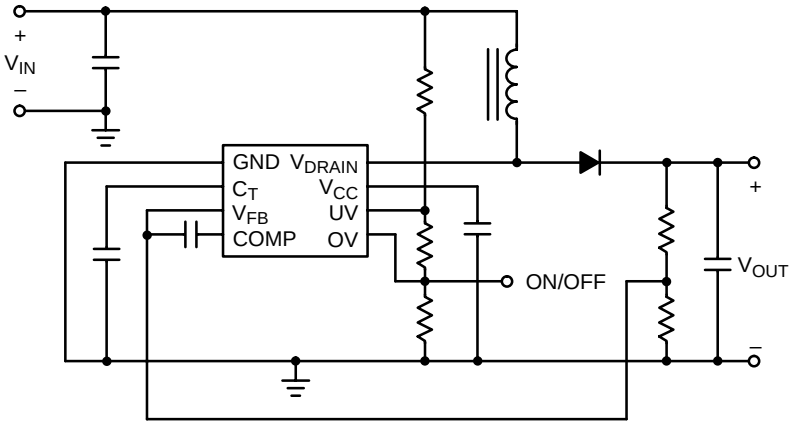


Figure 5. Boost Circuit Configuration

OPERATING DESCRIPTION

Introduction

The NCP1030 is a miniature, monolithic Voltage–Mode switching regulator designed to operate from a 48 V supply, commonly found in telecommunication systems. It is a fixed frequency regulator optimized for operation up to 1 MHz. The NCP1030 incorporates in a single IC all the active power, control logic and protection circuitry required to implement, with a minimum of external components, several switching regulator applications, such as a secondary side bias, low boost converter or secondary side regulator. This device is available in the space saving S0–8 and Micro 8 packages, making it a space efficient and cost saving solution.

The NCP1030 includes a powerful set of features including over temperature protection, cycle by cycle current limiting, line under/over voltage lockout with hysteresis, and regulator output under voltage lockout with hysteresis, providing full protection during fault conditions. A description of each of the functional blocks is given below, and the representative block diagram is shown in Figure 2.

V_{CC} Limiter and Undervoltage Lockout

The NCP1030 contains an internal 200 V start–up regulator that eliminates the need for external start–up components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding.

The start–up regulator consists of a constant current source that supplies current from the input line (V_{in}) to the capacitor on the V_{CC} pin. The start–up current is typically 5 mA. Once the V_{CC} voltage reaches 10 V during initial power up, the start–up circuit is disabled and the Power Switch Circuit is enabled if no faults are present. During this self–bias mode, power to the NCP1030 is supplied by the V_{CC} capacitor. The start–up regulator turns ON again once V_{CC} reaches 7.5 V. This “7.5–10” mode of operation is known as Dynamic Self Supply (DSS).

If V_{CC} falls below 7.5 V after initial power–up, the device enters a re–start mode. While in the re–start mode, the Power Switch Circuit is disabled and V_{CC} is allowed to discharge to 6.5 V. At that time, the start–up regulator turns ON again to charge the V_{CC} capacitor.

The V_{CC} pin can be biased above 7.5 V using an auxiliary winding once switching is allowed. This will keep the start–up regulator from turning ON, thus reducing power consumption.

The external V_{CC} capacitor must be sized such that the self–bias will maintain a V_{CC} voltage greater than 7.5 V during initial start–up.

The start–up circuit is rated at a maximum of 200 V. If the device operates in the DSS mode, power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller.

Error Amplifier

The internal error amplifier compares the scaled output signal to an internal 2.5 V reference connected to its non–inverting input. The feedback pin (V_{FB}) connects directly to the error amplifier inverting input. The output of the error amplifier is available for frequency compensation and connection to the PWM comparator through the COMP pin.

The error amplifier input bias current is less than 1 μA over the operating range. The output source and sink currents are typically 100 μA and 500 μA, respectively.

Line Under/Over Voltage

The NCP1030 incorporates line undervoltage (UV) and overvoltage (OV) shutdown circuits. The UV and OV thresholds are 2.5 V. A fault is present if the UV is below 2.5 V or if the OV voltage is above 2.5 V.

The UV/OV circuits can be biased using an external resistor divider from the input line as shown in Figure 6.

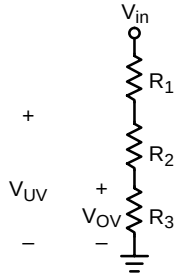


Figure 6. UV/OV resistor divider from the input line

The resistor divider must be sized to enable the controller once V_{in} is within the required operating range. When a UV or UV fault is present, switching is not allowed and the COMP voltage is kept low.

Oscillator

The NCP1030 oscillator is designed to operate up to 1 MHz and its frequency is set by the external timing capacitor (C_T) connected on the C_T pin. The oscillator has two modes of operation, free running and synchronized (sync).

While in free running mode, an internal current source sequentially charges and discharges C_T generating a voltage ramp between 2.5 V and 3.5 V. Under normal operating conditions the charge (I_1) and discharge (I_2) currents are typically 200 μA and 600 μA, respectively. However, if an UV fault is present, I_1 and I_2 are both reduced by a factor of 2.5 to reduce power consumption. The charge:discharge current ratio of 1:3 discharges C_T in 25 % of the charge period. As the Power Switch is disabled while C_T is discharging, a maximum duty cycle of 75% is assured.

If the operating frequency (f) is known, C_T is calculated using the equation below.

$$C_T = \frac{(200\ \mu A) \cdot (0.75)}{(1\ V) \cdot (f)}$$

Other factors such as operating frequency, comparator delay and temperature variations affect the calculated C_T value. Figure X shows the measured frequency variation vs timing capacitor.

The NCP1030 is capable of synchronization to a higher frequency. The oscillator frequency should be set no more that 25% below the target sync frequency. In sync mode, the voltage on the C_T pin needs to be driven above 3.5 V to trigger the internal comparator and complete the C_T charging period. This can be done pulsing the C_T pin as shown below.

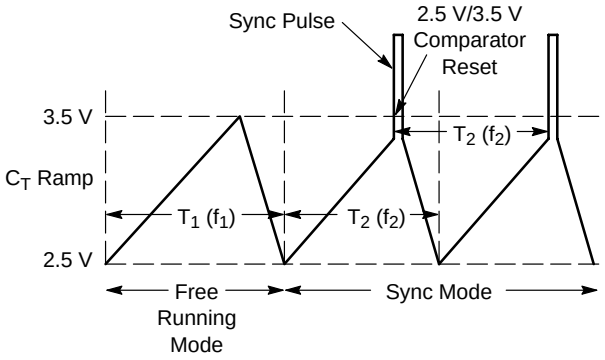


Figure 7. External Frequency Synchronization

Once the sync pulse is removed, the C_T voltage needs to closely match the voltage prior to applying the pulse. If not, the charge:discharge ratio will deviate from the 1:3 ratio, and the preset maximum duty cycle limit (75%) will change accordingly.

PWM Comparator and Latch

The Pulse Width Modulator (PWM) Comparator converts the DC error signal into a duty cycle by comparing the DC error signal to the C_T Ramp. The output of the PWM Comparator goes high, thus disabling the Power Switch, when the DC error signal exceeds the C_T Ramp as shown in Figure 2.

The C_T Charge Signal out of the 2.5 V/3.5 V Comparator is filtered through a One Shot Pulse Generator to set the PWM Latch and enable switching at the beginning of each period. Switching is allowed while the error signal is above the C_T Ramp and a current limit fault is not present. If the C_T Ramp does not exceed the DC error signal or a current limit fault is detected, the Power Switch Circuit is disabled once the C_T Charge Signal goes low. Therefore, the maximum duty cycle is limited by the duration of C_T Charge Signal.

Current Limit Comparator and Power Switch Circuit

The NCP1030 monolithically integrates a 200 V Power Switch Circuit with control logic circuitry. The Power Switch Circuit is designed to directly drive the converter transformer. The characteristics of the Power Switch Circuit are well known. Therefore, the gate drive is tailored to control switching transitions and help limit electromagnetic interference (EMI). The Power Switch Circuit is capable of switching 200 V with a nominal peak drain current of 0.5 Amps.

The Power Switch Circuit incorporates SENSEFET™ technology to monitor the drain current. A sense voltage is generated by driving a sense element, R_{SENSE}, with a current proportional to the drain current. The sense voltage is compared to an internal reference voltage on the non–inverting input of the Current Limit Comparator. If the sense voltage exceeds the reference level, the comparator resets the PWM Latch and switching is terminated until the next cycle.

Each time the Power Switch Circuit turns ON, a narrow voltage spike appears across R_{SENSE} . The spike is due to the Power Switch Circuit gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. This spike can cause a premature reset of the PWM Latch. A Leading Edge Blanking (LEB) Circuit masks the current signal until the Power Switch Circuit turn–on transition is complete.

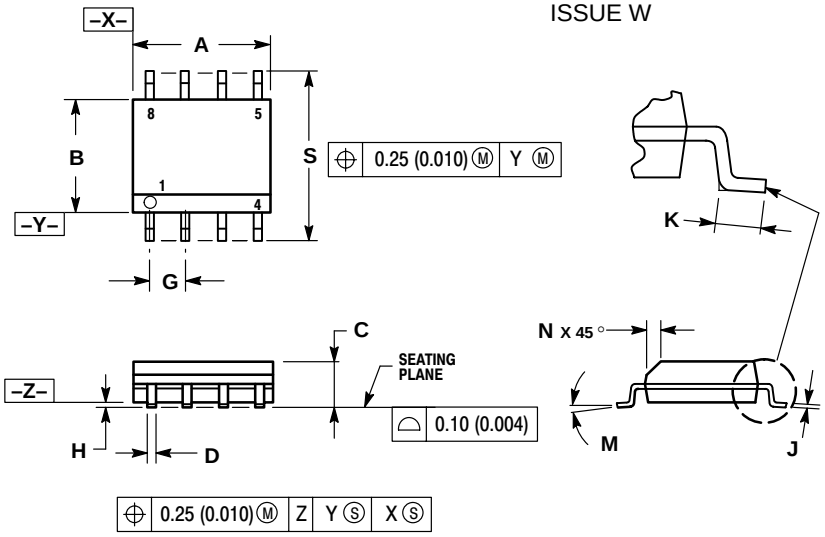
The current limit propagation delay time is typically 100 nanoseconds. This time is measured from when an over current fault appears at the Power Switch Circuit drain, to the start of the turn–off transition. Propagation delay must be factor in the transformer design to avoid transformer saturation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 150°C, the Power Switch Circuit is disabled. Once the junction temperature falls below 125°C, the NCP1030 is allowed to resume normal operation. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

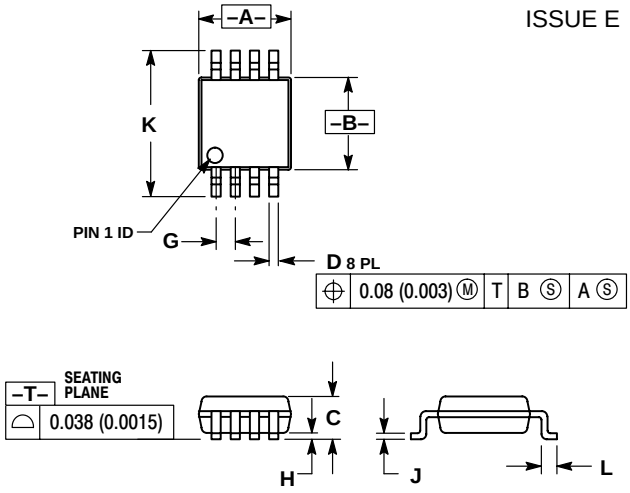
PACKAGE DIMENSIONS

S0–8
D SUFFIX
CASE 751–07
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

Micro 8
DM SUFFIX
CASE 846A–02
ISSUE E



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2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

Notes

Notes

The product described herein (NCP1030) may be covered by one or more U.S. patents. There may be other patents pending.
SENSEFET is a trademark of Semiconductor Components Industries, LLC.

PUBLICATION ORDERING INFORMATION

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