Synchronous PWM Controller with Over-Current Protection

Features

- Current Limit using Lower MOSFET Sensing
- Using the 6V internal regulator for charge pump circuit allows single supply operation up to 18V
- Programmable Switching Frequency up to 400KHz
- Soft-Start Function
- 0.8V Precision Reference Voltage Available
- Uncommitted Error Amplifier Available for DDR Voltage Tracking Applications
- Stable with Ceramic Capacitor
- RoHS-compliant, halogen-free packages

Applications

- DDR Memory V_{DDQ}/V_{TT} Applications
- Graphic Card
- Hard Disk Drive
- Netcom on-board DC to DC regulator application
- Output voltage as low as 0.8V
- Low Cost On-Board DC to DC

Description

The APU3039 controller IC is designed to provide a synchronous Buck regulator and is targeted for applications where cost and size are critical. The APU3039 operates with a single input supply up to 18V, and the output voltage can be programmed as low as 0.8V for low voltage applications. Selectable current limit is provided to tailor to external MOSFET's on-resistance for optimum cost and performance. The APU3039 features an uncommitted error amplifier for tracking output voltage and is capable of sourcing or sinking current for applications such as DDR bus termination.

This device features a programmable switching frequency set from 200KHz to 400KHz, under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

Typical Application

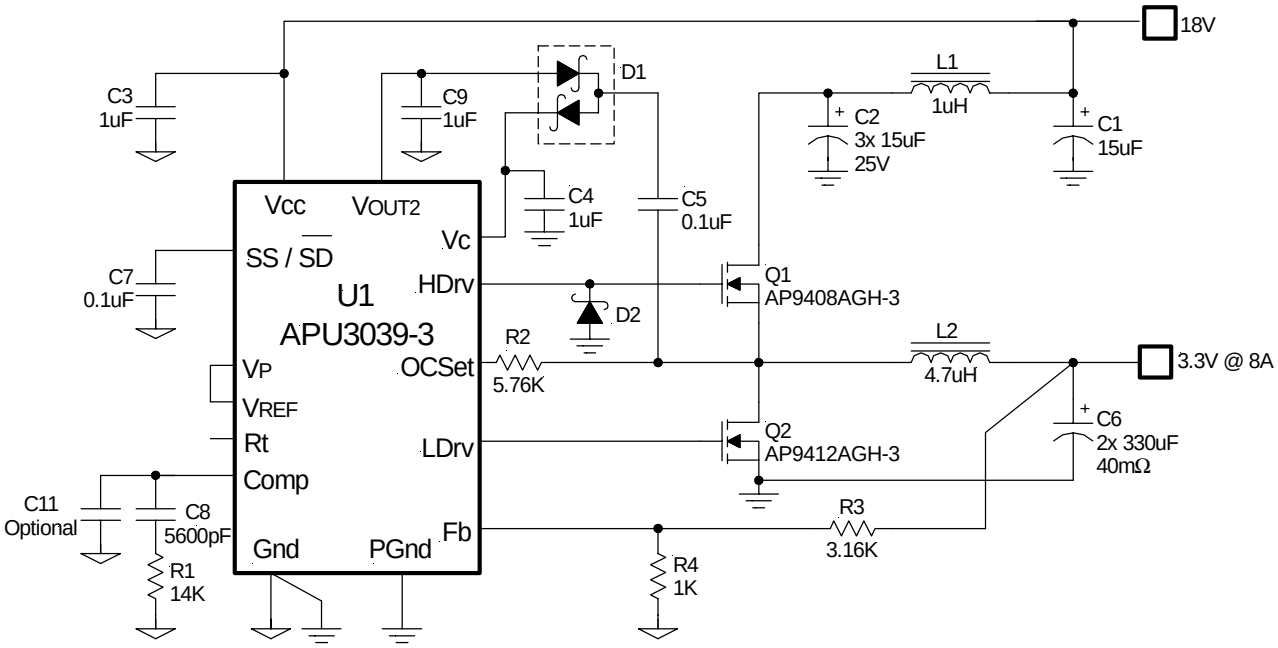


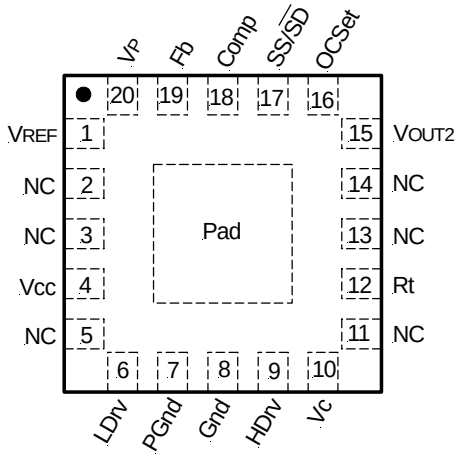
Figure 1 - Typical application of APU3039-3

Ordering Information

APU3039M-HF-3TR	RoHS-compliant, halogen-free 14-Pin plastic SOIC, shipped on tape and reel, 3000pcs/reel.
APU3039VN-HF-3TR	RoHS-compliant, halogen-free 20-Pin 5x5mm VQFN, shipped on tape and reel, 3000pcs/reel.

Pin Configuration

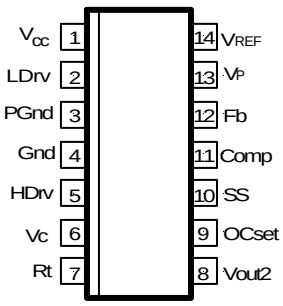
20-Pin VQFN 5x5



$R_{th(ja)}$ = 37°C/W
$R_{th(jc)}$ = 2.3°C/W

*Exposed pad on underside is connected to a typical 1" square copper pad through vias for 4-layer PCB board design.

14-PIN PLASTIC SOIC (M)



$R_{th(ja)}$ = 88°C/W
$R_{th(jc)}$ = 45°C/W

Absolute Maximum Ratings

Vcc Supply Voltage	-0.5V to 25V
Vc Supply Voltage	-0.5V to 25V
Storage Temperature Range	-65°C to 150°C
Operating Junction Temperature Range	0°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

Electrical Specifications

Unless otherwise specified, specifications apply over Vcc=5V, Vc=12V and T_A=0-70°C. Typical values refer to 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temp.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage						
Fb Voltage Initial Accuracy	V_{FB}		0.784	0.800	0.816	V
Fb Voltage Line Regulation	L_{REG}	4.75V<Vcc<20V		0.3		%
Reference Voltage						
Ref Voltage Initial Accuracy	V_{REF}		0.784	0.8	0.816	V
Drive Current	I_{REF}	Note 1		2		µA
UVLO						
UVLO Threshold - Vcc	UVLO V_{CC}	Supply Ramping Up		4.4		V
UVLO Hysteresis - Vcc				0.26		V
UVLO Threshold - Vc	UVLO V_C	Supply Ramping Up		3.47		V
UVLO Hysteresis - Vc				0.20		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down	0.3	0.4	0.5	V
Supply Current						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		7	15	mA
Vc Dynamic Supply Current	Dyn I_C	Freq=200KHz, C_L=1500pF		7	9	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		5	9	mA
Vc Static Supply Current	I_{CQ}	SS=0V		3	4	mA
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V	-1	+0.08	+1	µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V	30	55	70	µA
Transconductance				700		µmho
VP Voltage Range	V_P	Note 1	0.8		1.5	V
Soft-Start Section						
Charge Current	SS I_B	SS=0V	14	22	35	µA
Oscillator Section	Freq	Rt=Open		200		KHz
Frequency		Rt=Gnd		400		
Ramp Amplitude	V_{RAMP}	Note 1		1.25		V_{PP}
Output Drivers						
Lo Drive Rise Time	$Tr_{(LO)}$	C_{LOAD}=1500pF, V_{CC}=12V		40	100	ns
Hi Drive Rise Time	$Tr_{(HI)}$	C_{LOAD}=1500pF, V_{CC}=12V		40	100	ns
Lo Drive Fall Time	$Tf_{(LO)}$	C_{LOAD}=1500pF		40	100	ns
Hi Drive Fall Time	$Tf_{(HI)}$	C_{LOAD}=1500pF		40	100	ns
Dead Band Time	T_{DB}	HDrv going Hi or Low		100		ns
Max Duty Cycle	D_{MAX}	Fb=0.6V, Freq=200KHz		88		%
Min Duty Cycle	D_{MIN}	Fb=1.0V			0	%
Internal Regulator						
Output Voltage	V_{OUT2}	Vcc=12V	5.7	6	6.3	V
Drive Current	I_{OUT2}		40	65		mA
Current Limit						
OC Threshold Set Current	I_{OCSET}		21	28	35	µA
OC Comp Off-Set Voltage	$V_{OC(OFFSET)}$		-2	1.5	5	mV

Note 1: Guaranteed by design but not tested in production.

Pin Descriptions (Pin numbering for 20pin VQFN)

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	V_{REF}	Reference Voltage. This pin can source current about 2μA.
4	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side FET driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
6	LDrv	Output driver for the synchronous power MOSFET.
7	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to system's ground plane.
8	Gnd	This pin serves as analog ground for internal reference and control circuitry. A high frequency capacitor must be connected from Vcc pin to this pin for noise free operation.
9	HDrv	Output driver for the high side power MOSFET. This pin should not go negative (below ground), this may cause problem for the gate drive circuit. It can happen when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load. To prevent negative voltage at gate drive, a low forward voltage drop diode might be connected between this pin and ground.
10	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
12	Rt	The switching frequency can be Programmed between 200KHz and 400KHz by connecting a resistor between Rt and Gnd. By floating the pin, the switching frequency will be 200KHz and by grounding the pin, the switching frequency will be 400KHz.
15	V_{OUT2}	Output of internal regulator. The output is protected for short circuit. A high frequency capacitor is recommended to be connected from this pin to ground.
16	OCSet	This pin is connected to the Drain of the lower MOSFET via an external resister and it provides the positive sensing for the internal current sensing circuitry. The external resistor programs the current limit threshold depending on the $R_{DS(ON)}$ of the power MOSFET. An external capacitor can be placed in parallel with the programming resistor to provide high frequency noise filtering.
17	SS / $\overline{SD}$	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin down below 0.4V.
18	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
19	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
20	V_P	Non-inverting input of error amplifier.
2,3,5, 11,13,14	NC	No connection.

Block Diagram

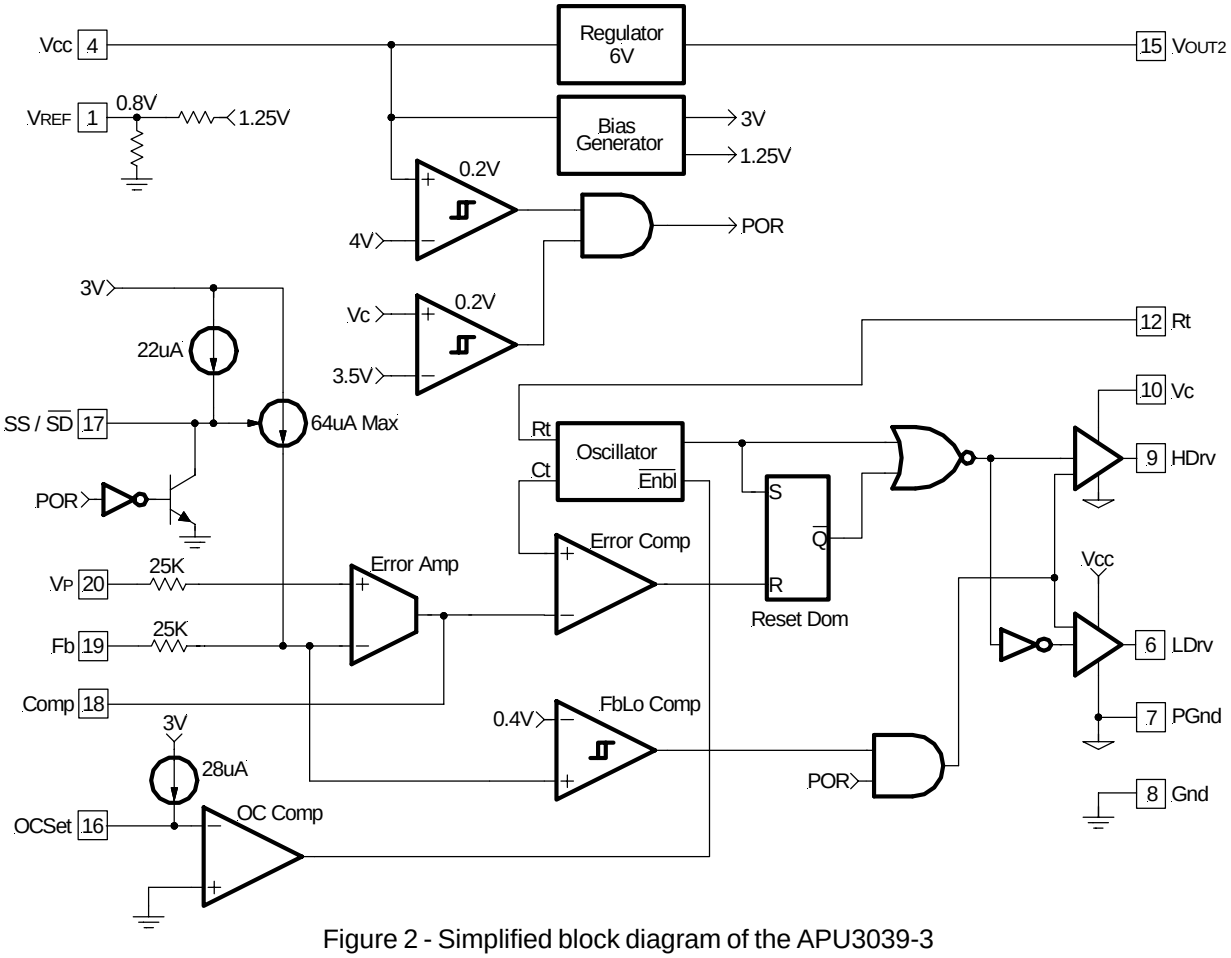


Figure 2 - Simplified block diagram of the APU3039-3

Theory of Operation

Introduction

The APU3039 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an uncommitted error amplifier, an internal oscillator, a PWM comparator, an internal regulator, a comparator for current limit, gate drivers, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the voltage on non-inverting input of error amplifier(V_P). This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor. The oscillation frequency is programmable between 200KHz to 400KHz by using an external resistor. Figure 14 shows switching frequency vs. external resistor (Rt).

Soft-Start

The APU3039 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.4V and 4.4V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter and disables the short circuit protection. During the power up, the output starts at zero and voltage at Fb is below 0.4V. The feedback UVLO is disabled during this time by injecting a current (64μA) into the Fb. This generates a voltage about 1.6V (64μAx25kΩ) across the negative input of E/A and positive input of the feedback UVLO comparator (see Figure 3).

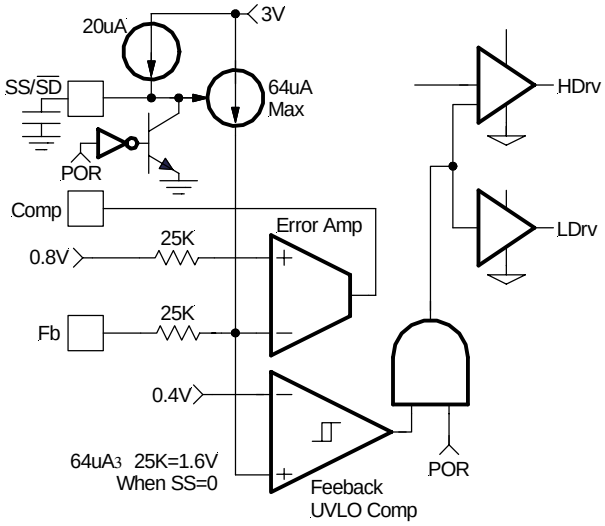


Figure 3 - Soft-start circuit for APU3039.

The magnitude of this current is inversely proportional to the voltage at soft-start pin.

The 20μA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at the positive pin of feedback UVLO comparator and the voltage negative input of E/A.

When the soft-start capacitor is around 1V, the current flowing into the Fb pin is approximately 32μA. The voltage at the positive input of the E/A is approximately:

$$32\mu A \times 25k\Omega = 0.8V$$

The E/A will start to operate and the output voltage starts to increase. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb pin will keep decreasing. Because the voltage at pin of E/A is regulated to reference voltage 0.8V, the voltage at the Fb is:

$$V_{FB} = 0.8 - (25k\Omega \times (\text{Injected Current}))$$

Theory of Operation (cont.)

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 2V and the output voltage goes into steady state.

As shown in Figure 4, the positive pin of feedback UVLO comparator is always higher than 0.4V, therefore, feedback UVLO is not functional during soft-start.

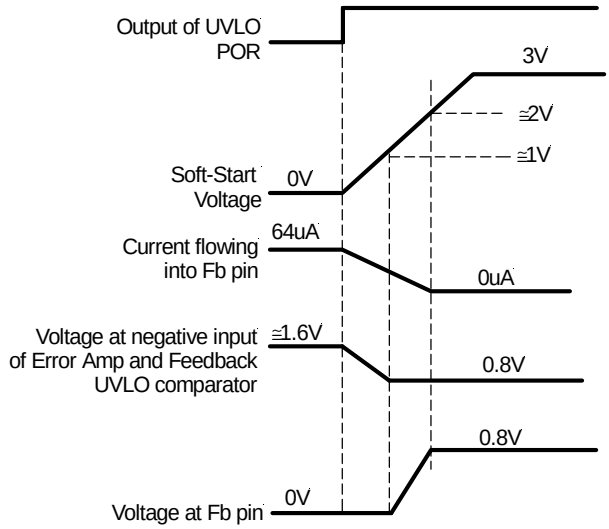


Figure 4 - Theoretical operational waveforms during soft-start.

the output start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$20\mu A \times T_{START}/C_{SS} = 2V\text{-}1V$$

For a given start up time, the soft-start capacitor can be estimated as:

$$C_{SS} \cong 20\mu A \times T_{START}/1V$$

Internal Regulator

The regulator powers directly from Vcc and generates a regulated voltage (6V @ 40mA). The output is protected for short circuit. This voltage can be used for charge pump circuitry as shown in Figure 1.

Supply Voltage Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc or Vcc fall below 3.4V and 4.4V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.4V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

Over-Current Protection

Over-current protection is achieved with a cycle by cycle scheme and it is performed by sensing current through the $R_{DS(ON)}$ of low side MOSFET. As shown in Figure 5, an external resistor (R_{SET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) and sets the current limit set point. The internal current source develops a voltage across R_{SET}. When the low side switch is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times i_L \qquad ---(1)$$

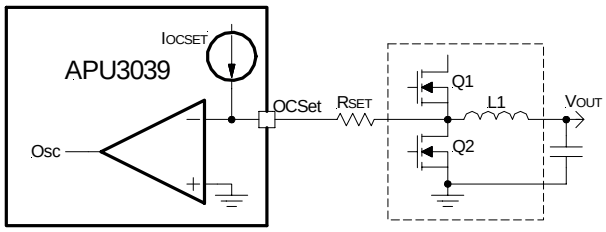


Figure 5 - Diagram of the over current sensing.

When voltage V_{OCSET} is below zero, the current sensing comparator flips and disables the oscillator. The high side MOSFET is turned off and the low side MOSFET is turned on until the inductor current reduces to below current set value. The critical inductor current can be calculated by setting:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times I_L = 0$$

$$I_{SET} = I_{L(CRITICAL)} = \frac{R_{SET} \times I_{OCSET}}{R_{DS(ON)}} \qquad ---(2)$$

If the over-current condition is temporary and goes away quickly, the APU3039 will resume its normal operation.

If output is shorted or over-current condition persists, the output voltage will keep going down until it is below 0.4V. Then the output under-voltage lock out comparator goes high and turns off both MOSFETs. The operation waveforms are shown in Figure 6.

Theory of Operation (cont.)

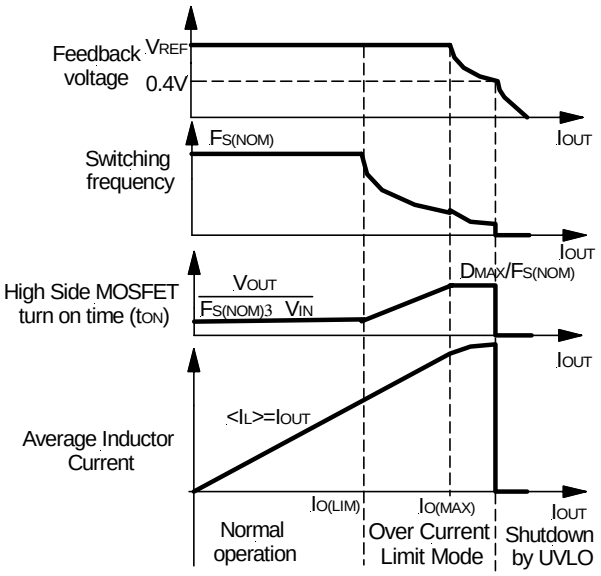


Figure 6 - Diagram of over-current operation.

Operation in current limit is shown in Figure 7, the high side MOSFET is turned off and inductor current starts to decrease. Because the output inductor current is higher than the current limit setpoint (I_{SET}), the over-current comparator keeps high until the inductor current decreases to be below I_{SET}. Then another cycle starts.

During over-current mode, the valley inductor current is:

$$i_{L(VALLEY)} = I_{SET}$$

The peak inductor current is given as:

$$I_{L(PEAK)} = I_{SET} + (V_{IN} - V_{OUT}) \times t_{ON}/L \qquad ---(3)$$

To avoid undesirable trigger of over-current protection, this relationship must be satisfied:

$$I_{SET} / I_{O(NOM)} - \frac{\Delta I_{PK-PK(NOM)}}{2}$$

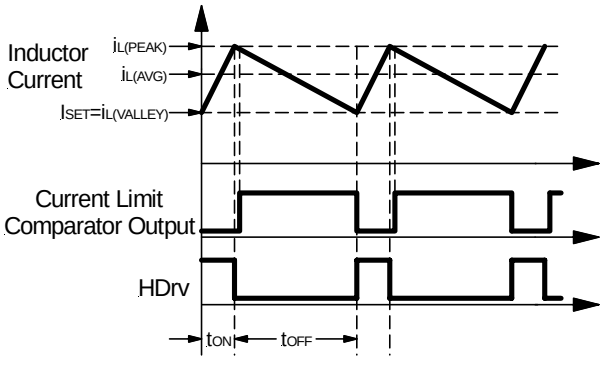


Figure 7 - Operation waveforms during current limit.

From Figure 7, the average inductor current during the current limit mode is:

$$I_{O(LIM)} = I_{SET} + \frac{\Delta I_{PK-PK(LIM)}}{2} \qquad ---(4)$$

The inductor's ripple current can be expressed as:

$$\Delta I_{PK-PK(LIM)} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times L \times f_S}$$

Combination of above equation and (4) results in:

$$I_{SET} = I_{O(LIM)} - \left(\frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{2 \times f_S \times L \times V_{IN}}\right) \qquad ---(5)$$

Combination of equations (5) and (2) results in the relationship between R_{SET} and output current limit.

$$R_{SET} = \frac{R_{DS(ON)}}{I_{OCSET}} \times \left[I_{O(LIM)} - \left(\frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{2 \times f_S \times L \times V_{IN}}\right)\right] \qquad ---(6)$$

Where:
$I_{O(LIM)}$ = The Output Current Limit. Typical is 50% higher than nominal output current
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
f_S = Switching Frequency
L = Output Inductor
$R_{DS(ON)}$ = $R_{DS(ON)}$ of Low Side MOSFET
I_{OCSET} = OC Threshold Set Current

From the above analysis, the current limit is not only dependent on the current setting resistor R_{SET} and $R_{DS(ON)}$ of low side MOSFET but it is also dependent on the input voltage, output voltage, inductance and switching frequency as well.

The cycle-by-cycle over-current limit will hold for a certain amount of time, until the output voltage drops below 0.4V, the under-voltage lock out activates and latches off the output driver. The operation waveform is shown in Figure 7. Normal operation will resume after APU3039 is powered up again.

Application Information

Design Example:
The following example is a typical application for APU3039, the schematic is Figure 17 on page 16.

V_{IN} = 18V
V_{OUT} = 3.3V
I_{OUT} = 8A
ΔV_{OUT} = 100mV (output voltage ripple ≅ 3% of V_{OUT})
f_S = 200KHz

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is referenced to the voltage on non-inverting pin of error amplifier. For this application, this pin (V_P) is connected to reference voltage (V_{REF}). The output voltage is defined by using the following equation:

$$V_{OUT} = V_P \times \left(1 + \frac{R_6}{R_5}\right) \quad ---(7)$$

$V_P = V_{REF} = 0.8V$

When an external resistor divider is connected to the output as shown in Figure 8.

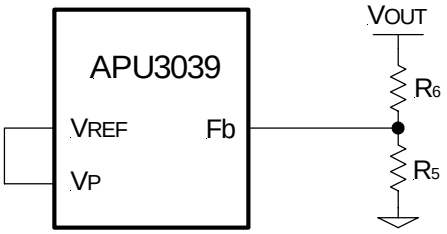


Figure 8 - Typical application of the APU3039 for programming the output voltage.

Equation (7) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_P} - 1\right)$$

Choose R_5 = 1K
This will result to R_6 = 3.16K

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} \cong 20 \times t_{START} \quad (\mu F) \quad ---(8)$$

Where t_{START} is the desired start-up time (ms)

For a start-up time of 5ms, the soft-start capacitor will be 0.1µF. Choose a ceramic capacitor at 0.1µF.

Boost Supply Vc
To drive the high side switch, it is necessary to supply a gate voltage at least 4V grater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 9. This method is simple and inexpensive. The operation of the circuit is as follows: when the lower MOSFET is turned on, the capacitor (C1) is pulled down to ground and charges, up to V_{OUT2} value, through the diode (D1). The bus voltage will be added to this voltage when upper MOSFET turns on in next cycle, and providing supply voltage (Vc) through diode (D2). Vc is approximately:

$$V_C \cong V_{OUT2} + V_{BUS} - (V_{D1} + V_{D2})$$

Capacitors in the range of 0.1µF and 1µF are generally adequate for most applications. The diode must be a fast recovery device to minimize the amount of charge fed back from the charge pump capacitor into V_{OUT2}. The diodes need to be able to block the full power rail voltage, which is seen when the high side MOSFET is switched on. For low voltage application, schottky diodes can be used to minimize forward drop across the diodes at start up.

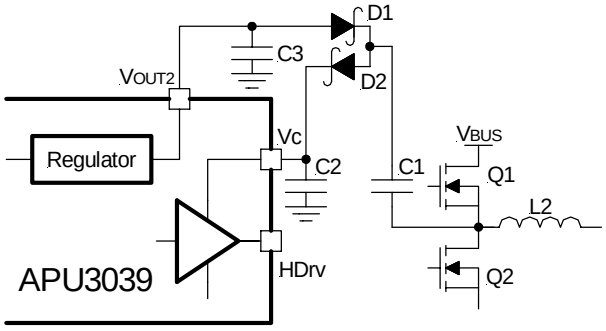


Figure 9 - Charge pump circuit.

Input Capacitor Selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

Application Information (cont.)

$$I_{RMS} = I_{OUT}\sqrt{D(1-D)} \quad ---(9)$$

Where:
D is the Duty Cycle, $D=V_{OUT}/V_{IN}$.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN}=20V, I_{OUT}=8A and D=0.165, the I_{RMS}=3A

For higher efficiency, a low ESR capacitor is recommended. Choose three Poscap from Sanyo 25TQC15M (25V, 15µF, 90mΩ) with a maximum allowable ripple current of 3A.

Inductor Selection
The inductor is selected based on operating frequency, transient performance and allowable output voltage ripple.

Low inductor value results to faster response to step load (high Δi/Δt) and smaller size but will cause larger output ripple due to increase of inductor ripple current. As a rule of thumb, select an inductor that produces a ripple current of 10-40% of full load DC.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \Delta t = D \times \frac{1}{f_S} \; ; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \quad ---(11)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

If $\Delta i = 37\%(I_O)$, then the output inductor will be:

L = 4.65µH

The Coilcraft DO5022HC series provides a range of inductors in different values, low profile suitable for large currents, 4.7µH, 13A is a good choice for this application. This will result to a ripple approximately 37% of output current.

Output Capacitor Selection
The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \; [\; \frac{\Delta V_O}{\Delta I_O} \quad ---(10)$$

Where:
ΔV_O = Output Voltage Ripple
Δi = Inductor Ripple Current
ΔV_O = 100mV and $\Delta I \cong 40\%$ of 8A = 3.2A
This results in ESR = 31mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC330M, 330µF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results in an ESR of ≅ 20mohm which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

Power MOSFET Selection
The APU3039 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter, the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND}(\text{Upper Switch}) \cong I_{LOAD}^2 \times R_{DS(ON)} \times D \times \theta$$

$$P_{COND}(\text{Lower Switch}) \cong I_{LOAD}^2 \times R_{DS(ON)} \times (1 - D) \times \theta$$

θ = $R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Application Information (cont.)

Choose AP9408AGH-3 for the control MOSFET and AP9412AGH-3 for the synchronous MOSFET. These devices provide low on-resistance in a small TO-252 package.

The MOSFETs have the following data:

AP9408AGH-3	AP9412AGH-3
V_{DSS} = 30V	V_{DSS} = 30V
I_D = 53A	I_D = 68A
$R_{DS(ON)}$ = 10mΩ	$R_{DS(ON)}$ = 6mΩ

The total conduction losses will be:

$P_{CON(TOTAL)} = P_{CON(UPPER)} + P_{CON(LOWER)}$

$P_{CON(TOTAL)} = 0.64W$

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \quad \text{---(12)}$$

Where:

$V_{DS(OFF)}$ = Drain to Source Voltage at off time

t_r = Rise Time

t_f = Fall Time

T = Switching Period

I_{LOAD} = Load Current

The switching time waveform is shown in Figure 10.

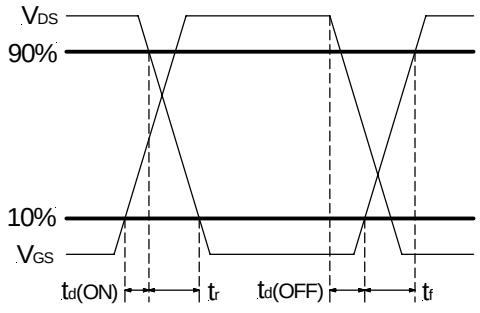


Figure 10 - Switching time waveforms.

From AP9408AGH-3 data sheet we obtain:

AP9408AGH-3

t_r = 5ns

t_f = 6ns

These values are taken under a certain condition test. For more details please refer to the AP9408AGH-3 and AP9412AGH-3 data sheets.

By using equation (12), we can calculate the total switching losses.

$P_{SW(TOTAL)}$ = 150mW

Programming the Over-Current Limit

The over-current threshold can be set by connecting a resistor (R_{SET}) from drain of low side MOSFET to the OCSet pin. The resistor can be calculated by using equation (2).

The $R_{DS(ON)}$ has a positive temperature coefficient and it should be considered for the worse case operation.

$R_{DS(ON)}$ = 8mΩ x 1.5 = 12mΩ

$I_{SET} \cong I_{O(LIM)}$ = 8A x 1.5 = 12A

(50% over nominal output current)

This results in:

R_{SET} = 5.76kΩ

Feedback Compensation

The APU3039 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 11). The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad \text{---(13)}$$

Figure 11 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

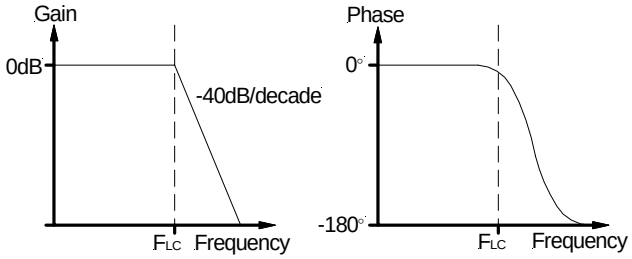


Figure 11 - Gain and phase of LC filter.

Application Information (cont.)

The APU3039's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback, the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 12.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general, the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(14)$$

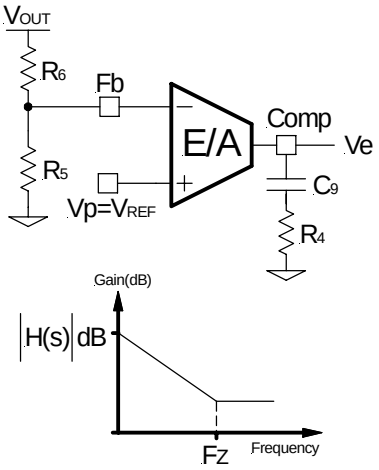


Figure 12 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(15)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s=j x 2\pi x F_O)| = g_m \times \frac{R_5}{R_6 x R_5} \times R_4 \qquad ---(16)$$

$$F_Z = \frac{1}{2\pi x R_4 x C_9} \qquad ---(17)$$

|H(s)| is the gain at zero cross frequency.

First select the desired zero-crossover frequency (Fo):

$F_O > F_{ESR}$ and F_O [(1/5 ~ 1/10) x f_S

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo x F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \qquad ---(18)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:

V_{IN} = 18V	F_{LC} = 2.8kHz
V_{OSC} = 1.25V	R_5 = 1kΩ
Fo = 20kHz	R_6 = 3.16kΩ
F_{ESR} = 12kHz	g_m = 700µmho

This results in R_4=12.08kΩ
Choose R_4=14kΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \qquad ---(19)$$

For:

Lo = 4.7µH	F_Z = 2.1kHz
Co = 660µF	R_4 = 14kΩ

Using equations (17) and (19) to calculate C_9, we get:

$C_9 \cong$ 5300pF; Choose C_9=5600pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi x R_4 x \frac{C_9 x C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi x R_4 x f_S - \frac{1}{C_9}} \cong \frac{1}{\pi x R_4 x f_S}$$

for $F_P << \frac{f_S}{2}$

Application Information (cont.)

For a general solution for unconditionally stability for ceramic capacitor with very low ESR and any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for a voltage-mode controller is shown in Figure 13.

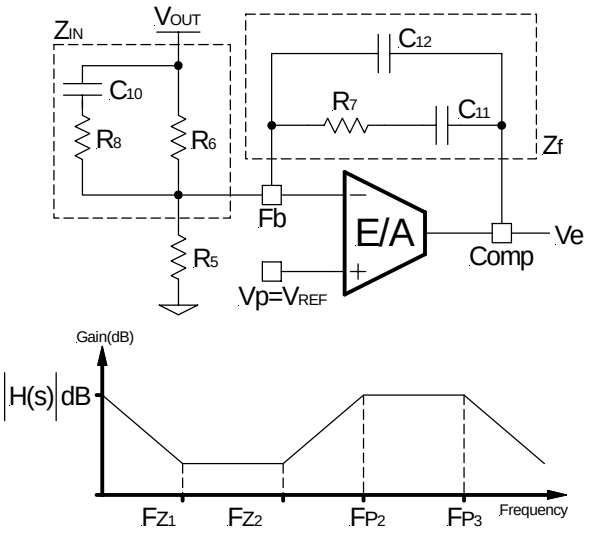


Figure 13 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(20)}$$

By replacing Z_{IN} and Z_f according to Figure 9, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11})\times[1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right]} \times (1+sR_8C_{10})$$

As known, transconductance amplifier has high impedance (current source) output, therefore, care should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12} + C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(21)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (20) regarding transconductance error amplifier.

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

Based on the frequency of the zero generated by ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation type and location of crossover frequency.

Compensator Type	Location of Zero Crossover Frequency (F_O)	Typical Output Capacitor
Type II (PI)	$F_{PO} < F_{ZO} < F_O < f_S/2$	Electrolytic, Tantalum
Type III (PID) Method A	$F_{PO} < F_O < F_{ZO} < f_S/2$	Tantalum, Ceramic
Type III (PID) Method B	$F_{PO} < F_O < f_S/2 < F_{ZO}$	Ceramic

Table - The compensation type and location of zero crossover frequency.

Application Information (cont.)

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components. Make all the connections in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET. To reduce the ESR, replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources and be placed close to the IC. In multilayer PCB, use one layer as power ground plane and have a separate control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

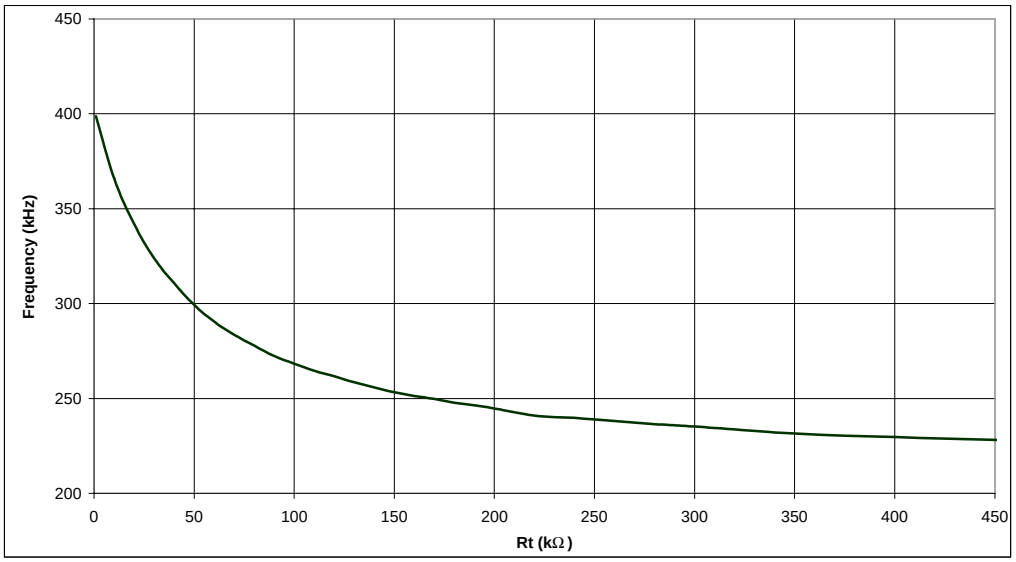


Figure 14 - Switching Frequency versus Resistor.

Typical Applications

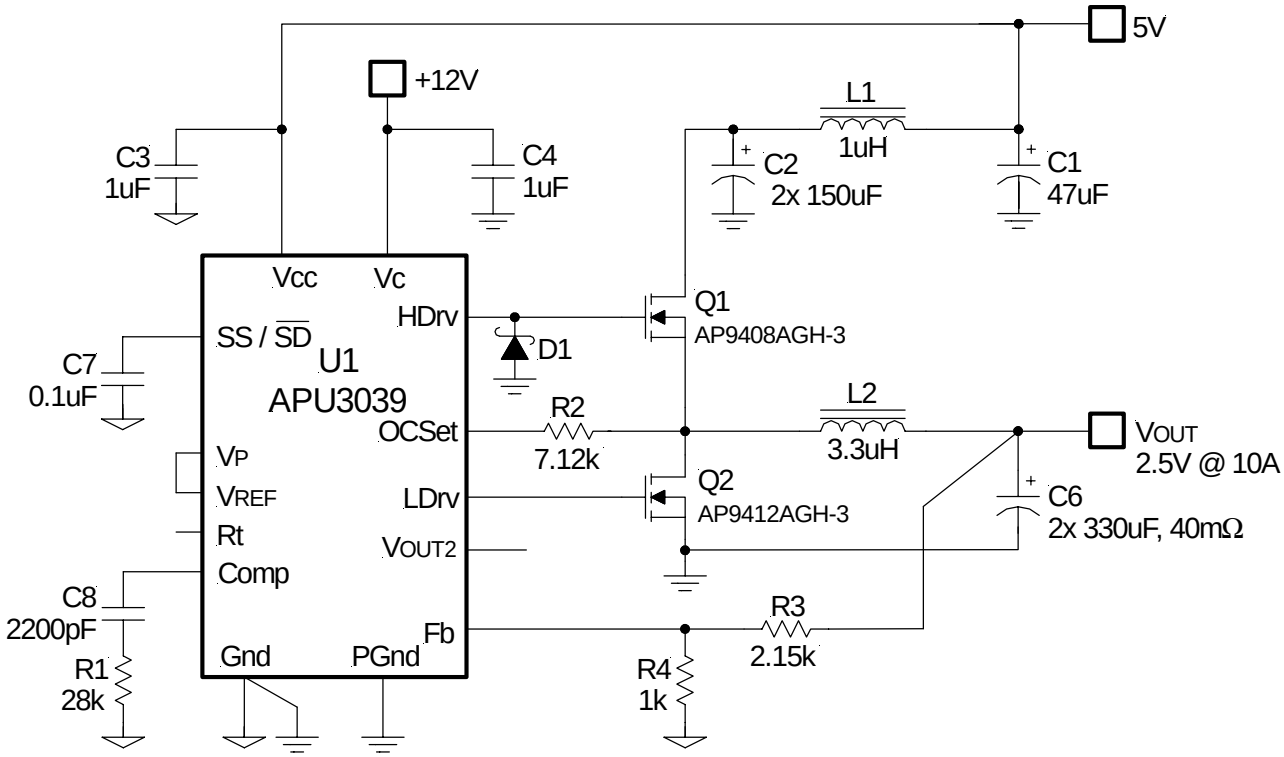


Figure 15 - Typical application of the APU3039-3 with two input supplies.

Typical Applications (cont.)

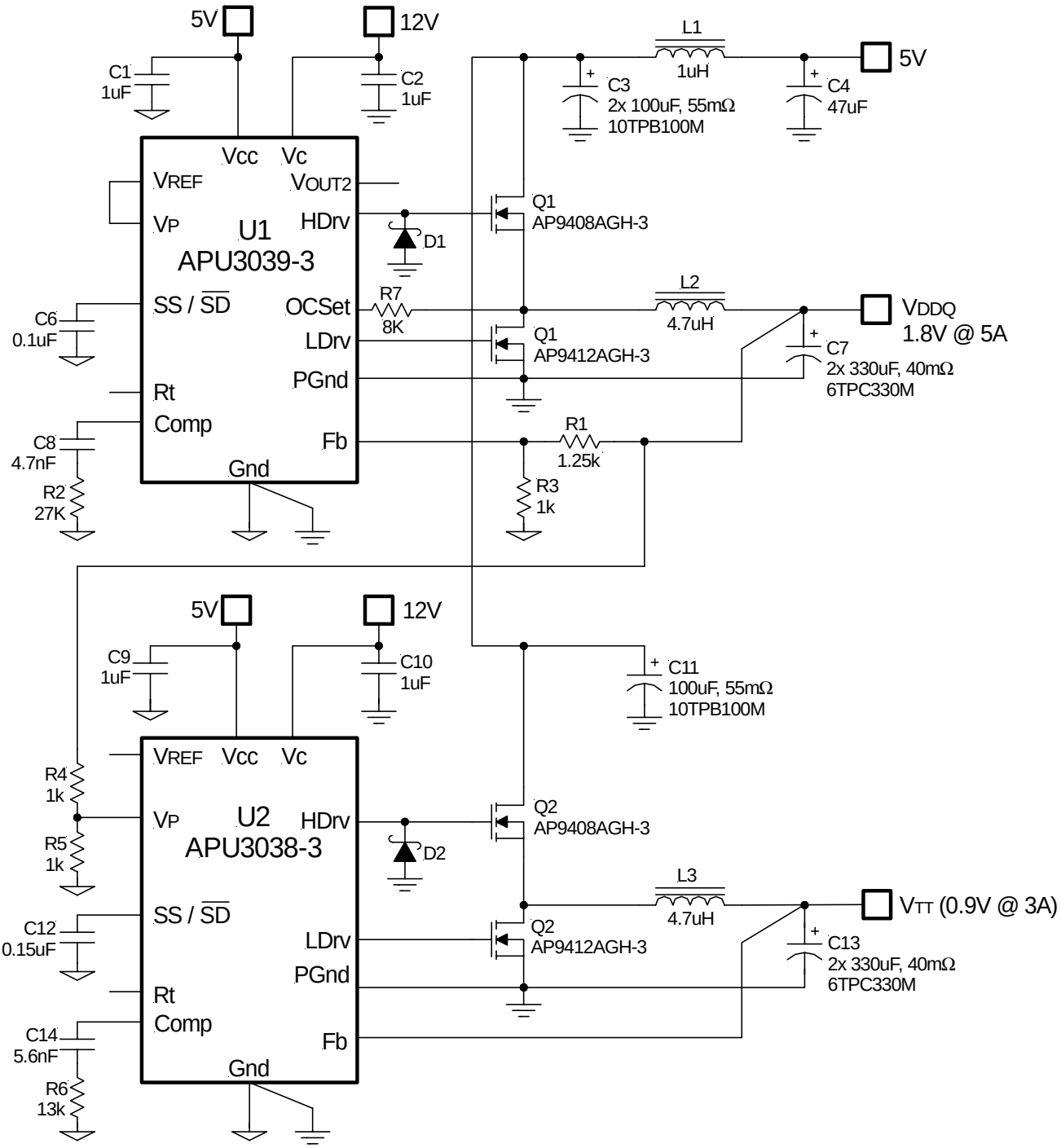


Figure 16 - Typical application of APU3039-3 for DDR memory using APU3039-3 to generate V_{CORE} and APU3038-3 to generate the termination voltage.

Demo Board Application

18V to 3.3V at 8A

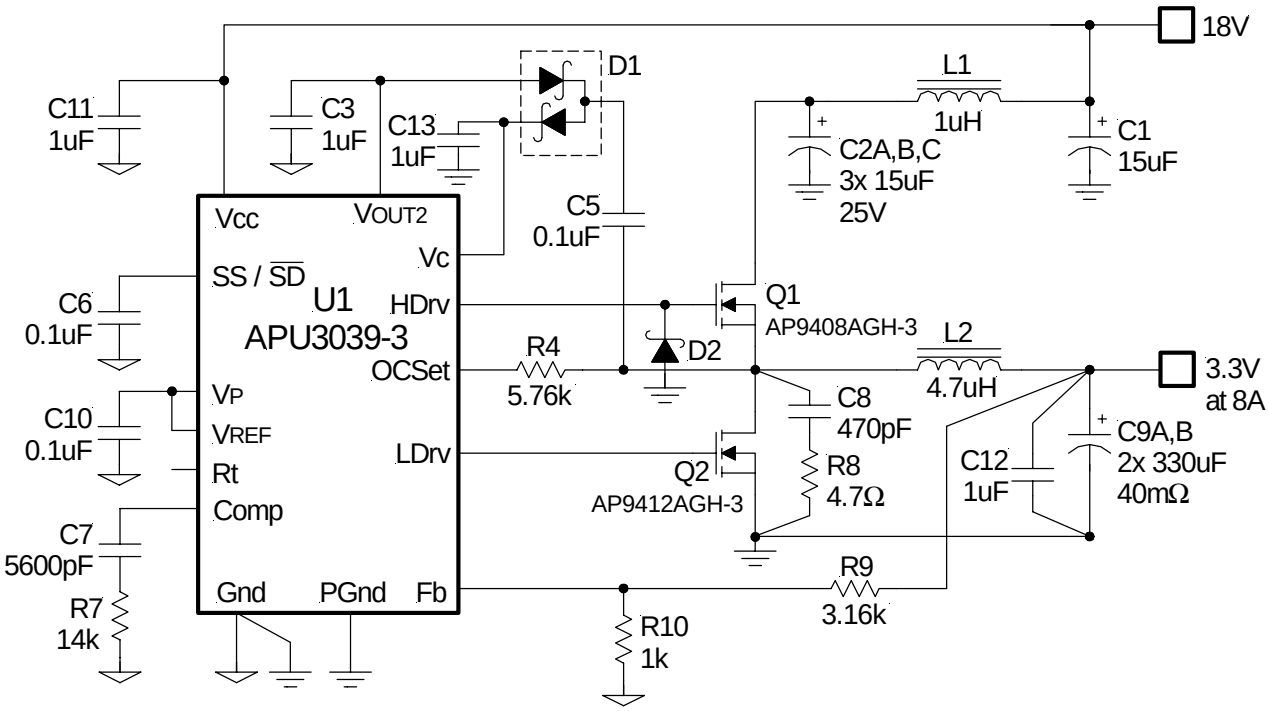


Figure 17 - Demo-board application of the APU3039-3

PARTS LIST

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1	MOSFET	30V, 10mΩ, 53A	1	AP9408AGH-3	APEC	a-powerusa.com
Q2	MOSFET	30V, 6mΩ, 68A	1	AP9412AGH-3	APEC	a-powerusa.com
U1	Controller	Synchronous PWM	1	APU3039-3	APEC	
D1	Schottky Diode	Fast Switching	1	BAT54S	IR	
D2	Schottky Diode	Fast Switching	1	BAT54	IR	
L1	Inductor	1µH, 3A	1	DS1608C-102	Coilcraft	coilcraft.com
L2	Inductor	4.7µH, 13A	1	DO5022P-472HC	Coilcraft	
C1,C2A,B,C	Cap, Poscap	15µF, 25V	4	25TQC15M	Sanyo	sanyo.com
C5,6,10	Capacitor	0.1µF, Y5V, 25V	3	ECJ-2VF1E104Z	Panasonic	maco.panasonic.co.jp
C7	Capacitor	5600pF, X7R, 50V	1	ECU-V1H562KBG	Panasonic	
C8	Capacitor	470pF, X7R, 50V	1	ECJ-2VC1H471J	Panasonic	
C9A,B	Capacitor	330uF, 40mΩ	2	6TPB-330M	Sanyo	sanyo.com
C3,11,12	Capacitor	1µF, Y5V, 16V	3	ECJ-2VF1C105Z	Panasonic	maco.panasonic.co.jp
C13	Capacitor	1µF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
R4	Resistor	5.76kΩ	1			
R7	Resistor	14kΩ	1			
R8	Resistor	4.7Ω	1			
R9	Resistor	3.16kΩ	1			
R10	Resistor	1kΩ	1			

Typical Operating Characteristics

Test Conditions:
V_{IN}=20V, V_{OUT}=3.3V, I_{OUT}=0-8A, Fs=200kHz

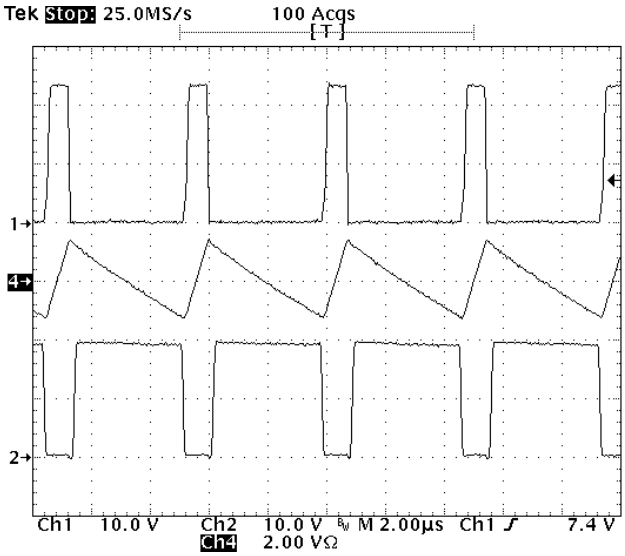


Figure 18 - Normal condition at No Load.
Ch1: HDrv, Ch2: LDrv, Ch4: Inductor Current

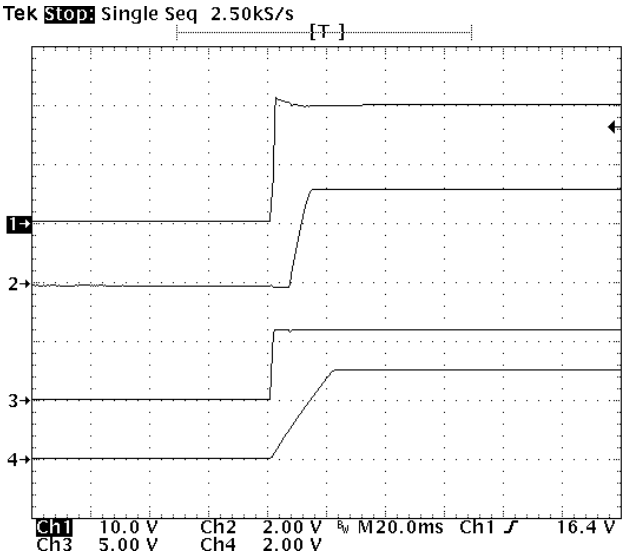


Figure 20 - Soft-Start.
Ch1: V_{IN}, Ch2: V_{OUT}, Ch3: V_{OUT2}, Ch4: Vss

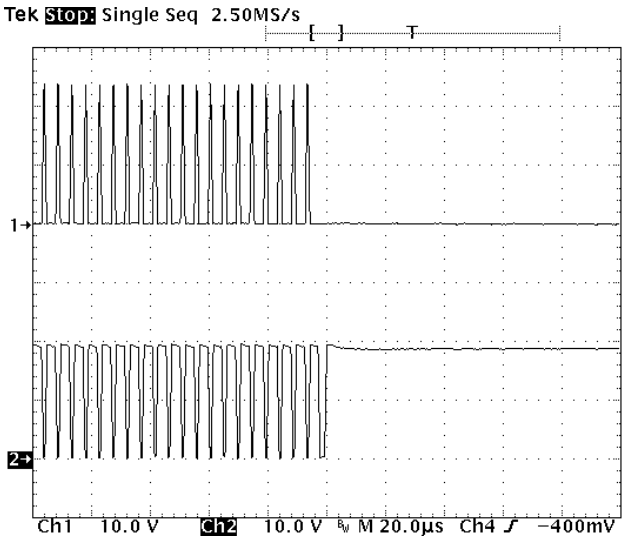


Figure 19 - Soft-Start pin grounded.
Ch1: HDrv, Ch2: LDrv

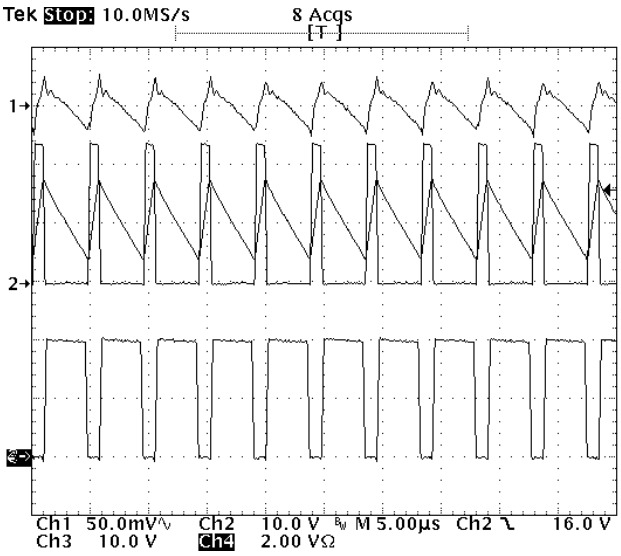


Figure 21 - Output Ripple.
Ch1: Output Ripple, Ch2: HDrv, Ch3: LDrv,
Ch4: Inductor Current

Typical Operating Characteristics (cont.)

Test Conditions:
V_{IN}=20V, V_{OUT}=3.3V, I_{OUT}=0-8A, Fs=200kHz

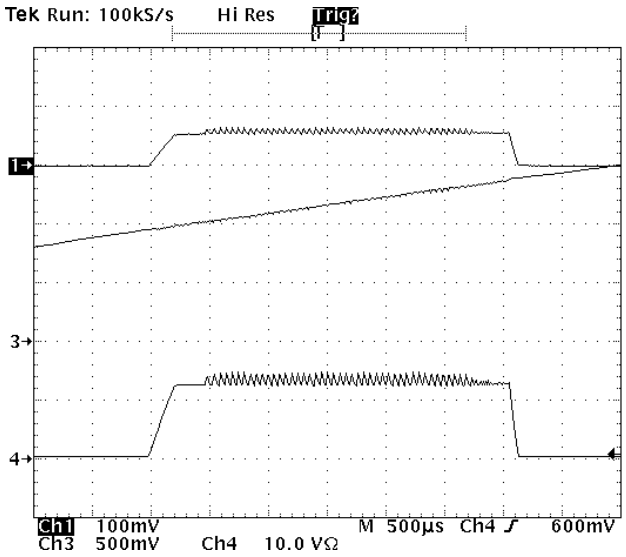


Figure 22 - Output shorted at start up.
Ch1: V_{OUT}, Ch3: Vss, Ch4: Inductor Current

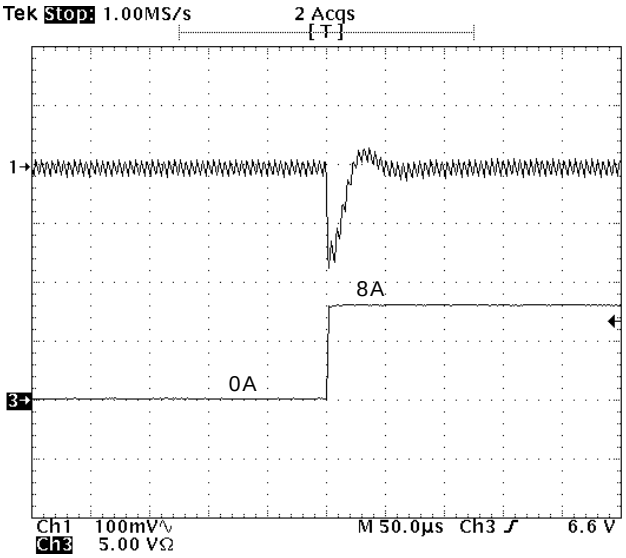


Figure 23 - Load Transient Response
Ch1: V_{OUT}, Ch3: Output Current

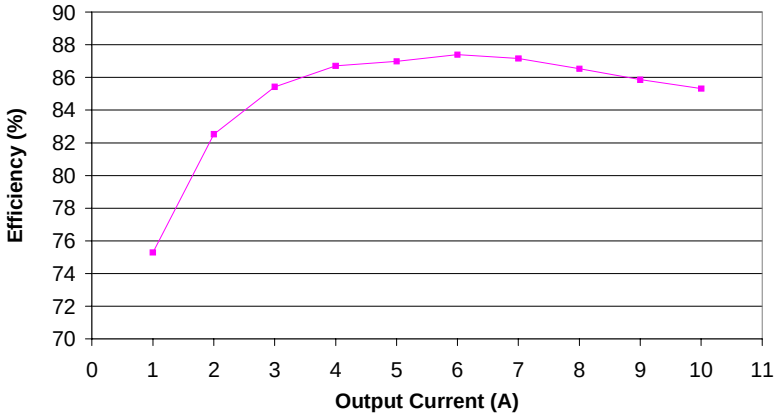


Figure 24 - Efficiency Measurement.
V_{IN}=20V, V_{OUT}=3.3V

Typical Performance Characteristics

For all charts: VC=VCC=12V, 20V, 24V

Note: Data are taken with few samples to indicate the variation of these parameters over the wide temperature range.

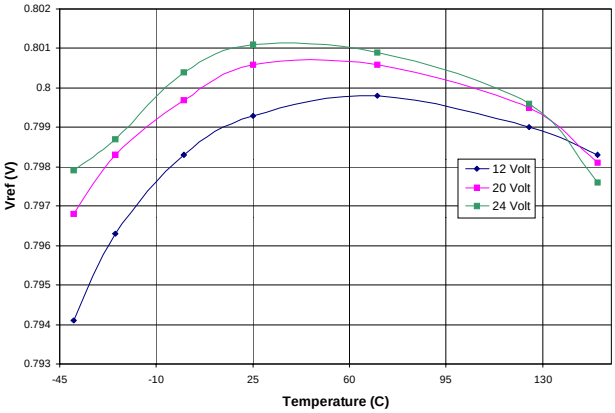


Figure 25 - V_{REF} vs.Temperature

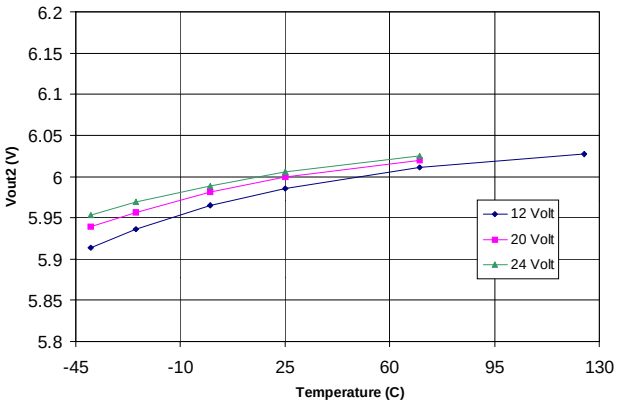


Figure 28 - V_{OUT2} vs.Temperature

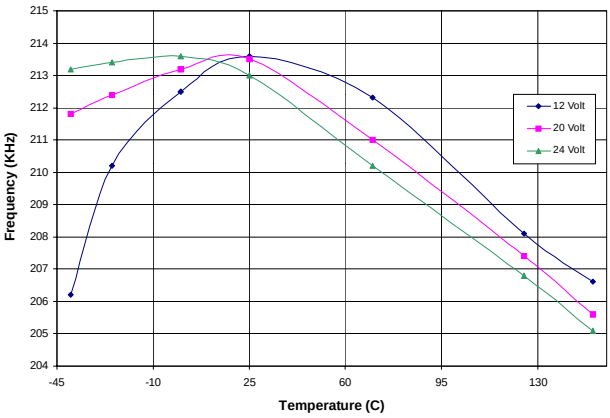


Figure 26 - Frequency vs.Temperature
F_S=200kHz

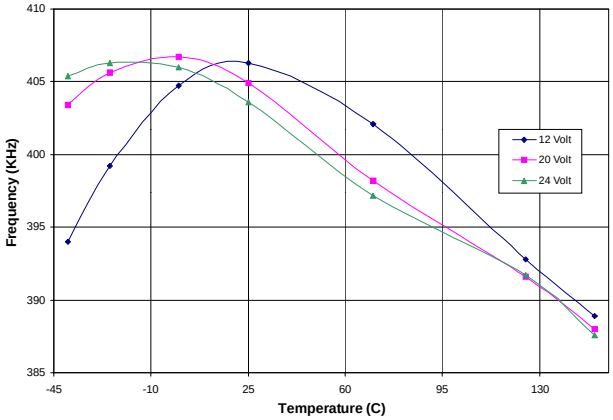


Figure 29 - Frequency vs.Temperature
F_S=400kHz

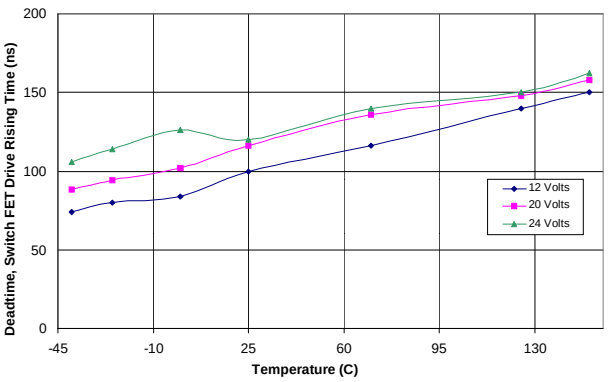


Figure 27 - Deadtime, Control FET Drive Rising Time vs.Temperature
F_S=400kHz, C_{LOAD}=3300pF

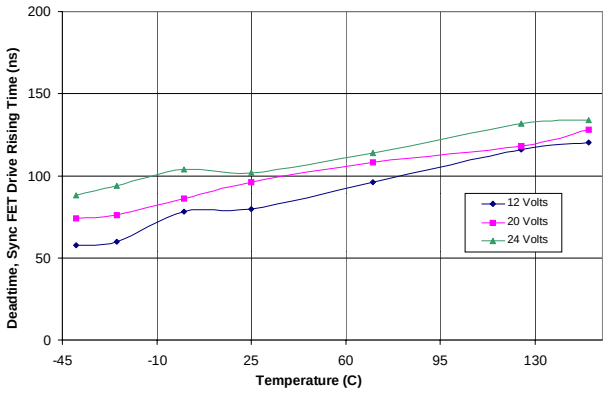


Figure 30 - Deadtime, Sync FET Drive Rising Time vs.Temperature
F_S=400kHz, C_{LOAD}=3300pF

Typical Performance Characteristics (cont.)

For all charts: VC=VCC=12V, 20V, 24V

Note: Data are taken with few samples to indicate the variation of these parameters over the wide temperature range.

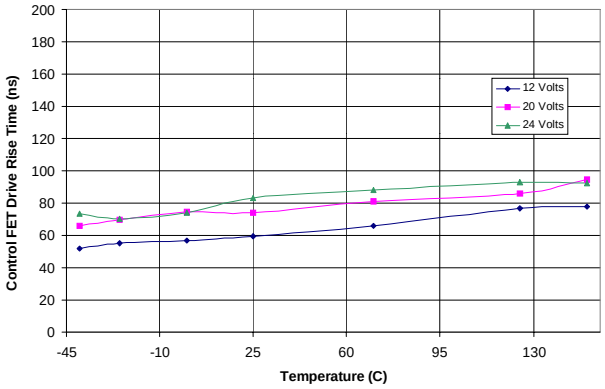


Figure 31 - Control FET Drive Rise Time vs.Temp.
F_S=400kHz, C_{LOAD}=3300pF

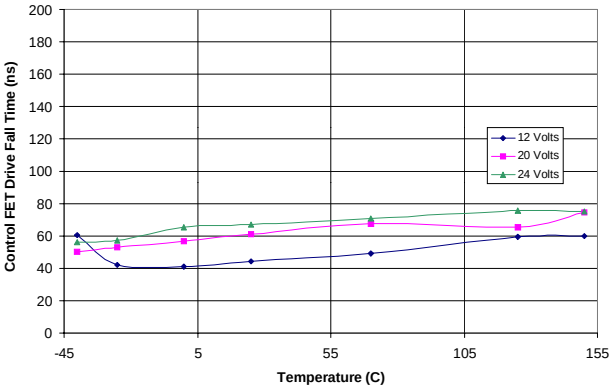


Figure 33 - Control FET Drive Fall Time vs.Temp.
F_S=400kHz, C_{LOAD}=3300pF

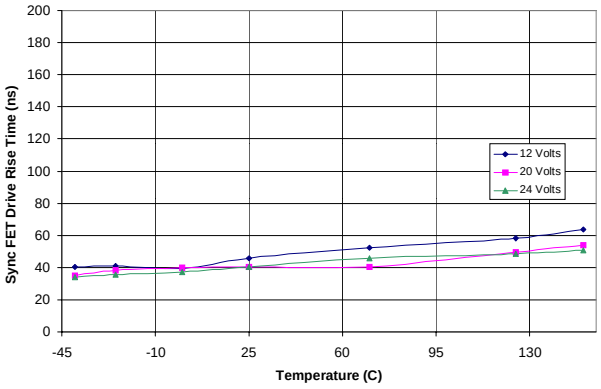


Figure 32 - Sync FET Drive Rise Time vs.Temp.
F_S=400kHz, C_{LOAD}=3300pF

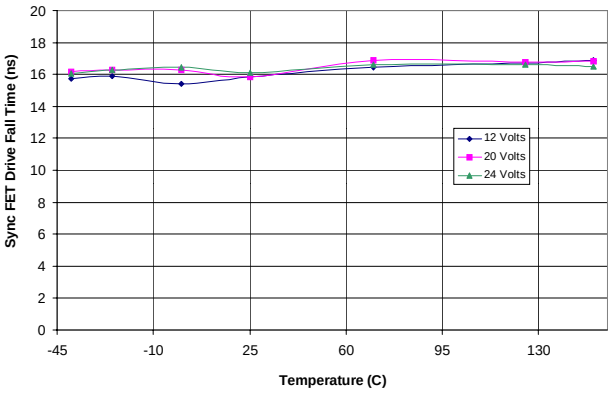
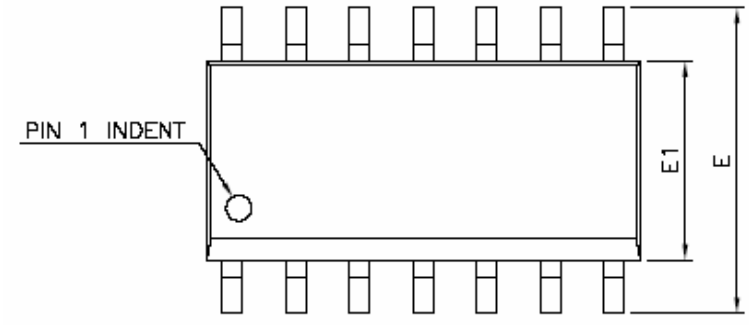
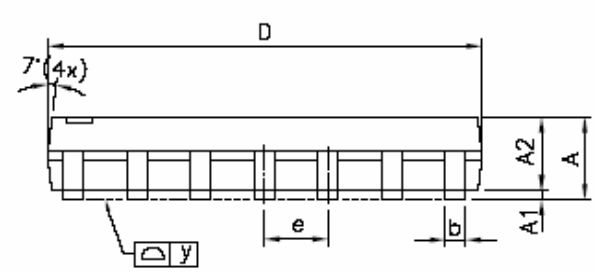
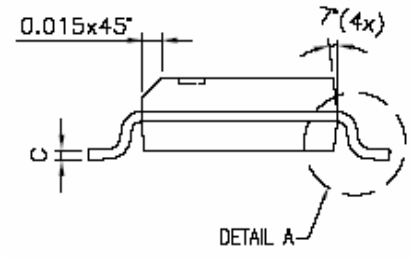


Figure 34 - Sync FET Drive Fall Time vs.Temp.
F_S=400kHz, C_{LOAD}=3300pF

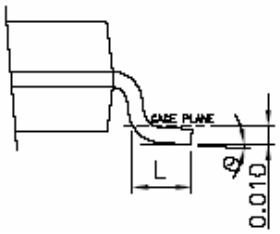
Package Dimensions: SOP-14





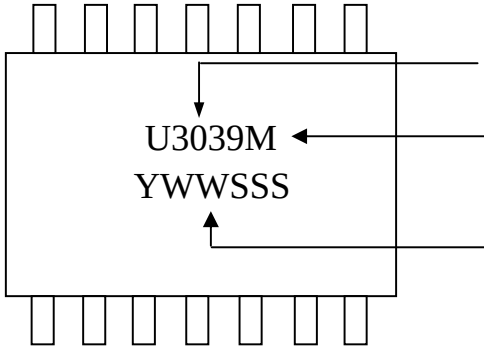


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.47	1.60	1.73
A1	0.10	—	0.25
A2	—	1.45	—
b	0.33	0.41	0.51
C	0.19	0.20	0.25
D	8.53	8.64	8.74
E	5.79	5.99	6.20
E1	3.81	3.91	3.99
e	—	1.27	—
L	0.40	0.71	1.27
y	—	—	0.076
θ	0°	—	8°



1. All dimension are in millimeters.
2. Dimensions do not include mold protrusions.

Part Marking



Product: U3039 = APU3039

Package code: M = RoHS-compliant halogen-free SO-14

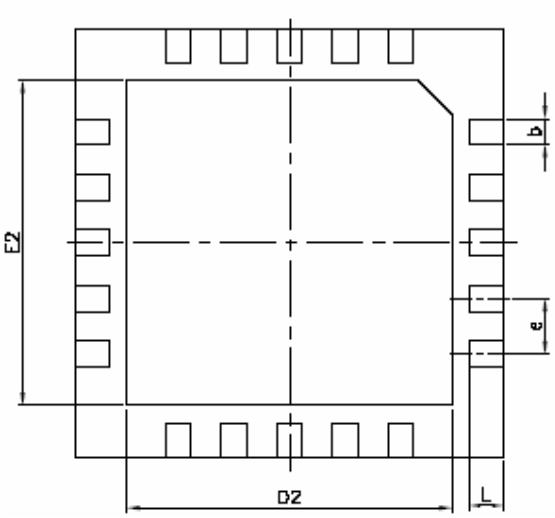
Date/lot code (YWWSSS)

Y: last digit of the year

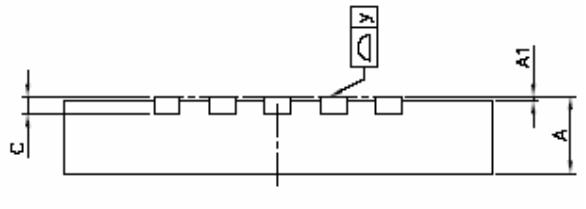
W: Work week

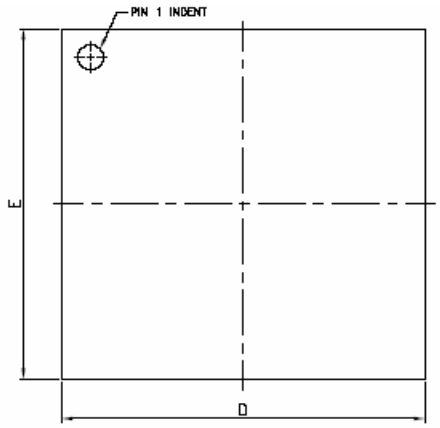
SSS: lot code sequence

Package Dimensions: VQFN20



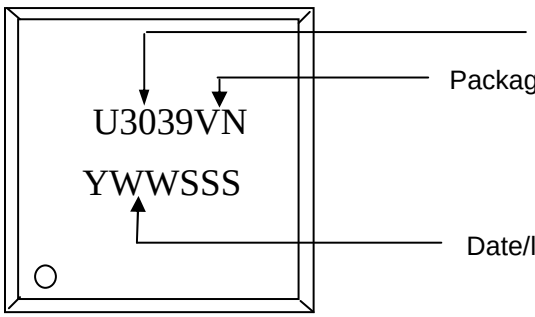
SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
C	0.19	0.20	0.25
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
E	4.90	5.00	5.10
E2	3.70	3.80	3.90
e	__	0.65	__
L	0.35	0.40	0.45
y	0.00	__	0.076





1. All dimension are in millimeters.
2. Dimensions do not include mold protrusions.

Part Marking



Product: U3039 = APU3039

Package code: VN = RoHS-compliant halogen-free VQFN

Date/lot code (YWWSSS)

Y: last digit of the year

W: Work week

SSS: lot code sequence