MJD148

NPN Silicon Power Transistor

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

Features

- High Gain – 50 Min @ I_C = 2.0 A
- Low Saturation Voltage – 0.5 V @ I_C = 2.0 A
- High Current Gain – Bandwidth Product – f_T = 3.0 MHz Min @ I_C = 250 mAdc
- Epoxy Meets UL 94 V–0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; >8000 V
  Machine Model, C; >400 V
- This is a Pb–Free Package

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	45	Vdc
Collector–Base Voltage	V_{CB}	45	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous – Peak	I_C	4.0 7.0	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation (Note 1) @ T_A = 25°C Derate above 25°C	P_D	 1.75 0.014	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction–to–Ambient (Note 1)	$R_{\theta JA}$	71.4	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

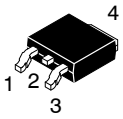
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ON Semiconductor®

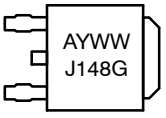
http://onsemi.com

POWER TRANSISTOR
4.0 AMPERES
45 VOLTS, 20 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



A = Assembly Location
Y = Year
WW = Work Week
J148 = Device Code
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJD148T4	DPAK	2500/Tape & Reel
MJD148T4G	DPAK (Pb–Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2)	I_C = 100 mAdc, I_B = 0	$V_{CEO(sus)}$	45	−	Vdc
Collector Cutoff Current	V_{CB} = 45 Vdc, I_E = 0	I_{CBO}	−	20	μAdc
Emitter Cutoff Current	V_{BE} = 5 Vdc, I_C = 0	I_{EBO}	−	1	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2)	I_C = 10 mAdc, V_{CE} = 5 Vdc I_C = 0.5 Adc, V_{CE} = 1 Vdc I_C = 2 Adc, V_{CE} = 1 Vdc I_C = 3 Adc, V_{CE} = 1 Vdc	h_{FE}	40 85 50 30	− 375 − −	−
Collector−Emitter Saturation Voltage (Note 2)	I_C = 2 Adc, I_B = 0.2 Adc	$V_{CE(sat)}$	−	0.5	Vdc
Base−Emitter On Voltage (Note 2)	I_C = 2 Adc, V_{CE} = 1 Vdc	$V_{BE(on)}$	−	1.1	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain−Bandwidth Product	I_C = 250 mAdc, V_{CE} = 1 Vdc, f = 1 MHz	f_T	3	−	MHz

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

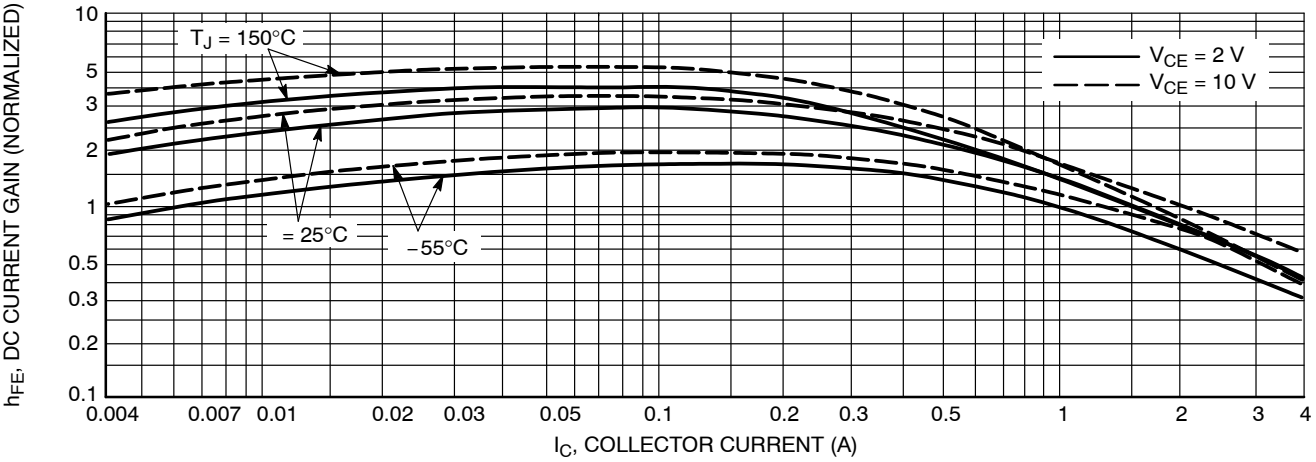


Figure 1. DC Current Gain

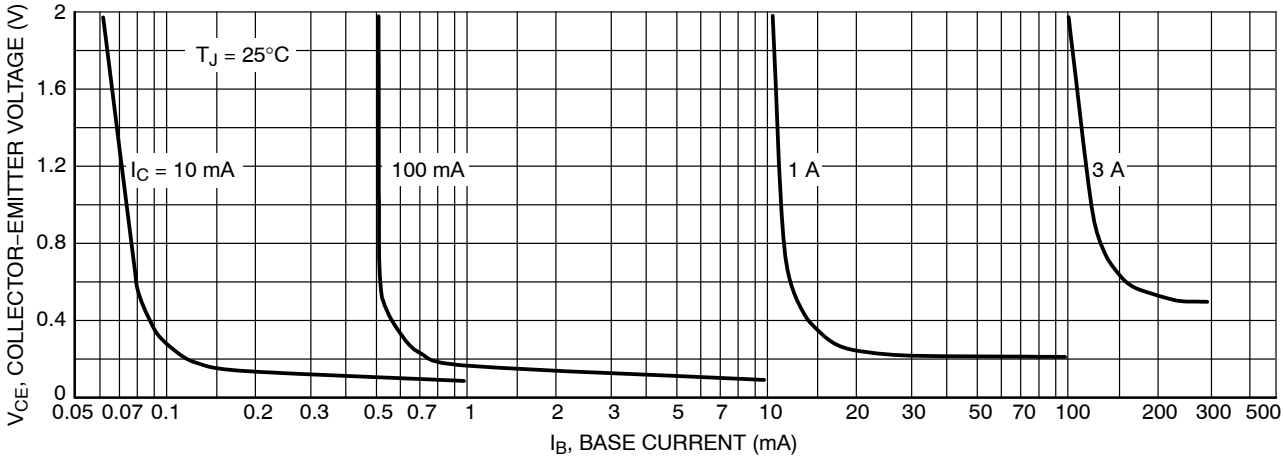


Figure 2. Collector Saturation Region

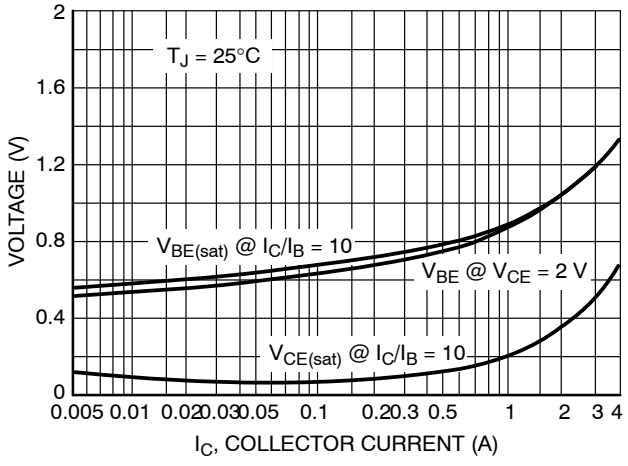


Figure 3. “On” Voltages

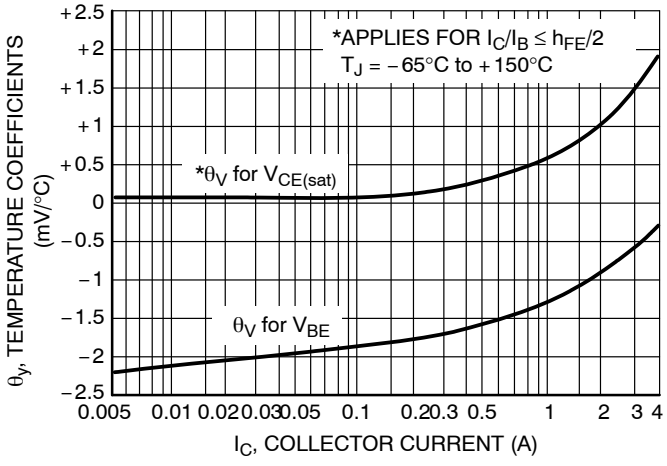


Figure 4. Temperature Coefficients

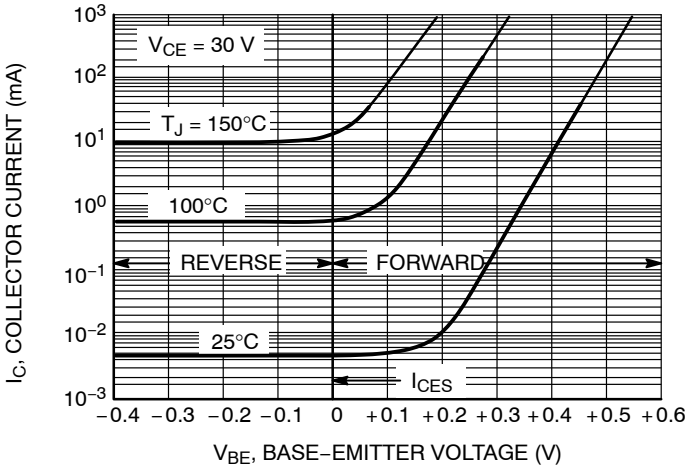


Figure 5. Collector Cut−Off Region

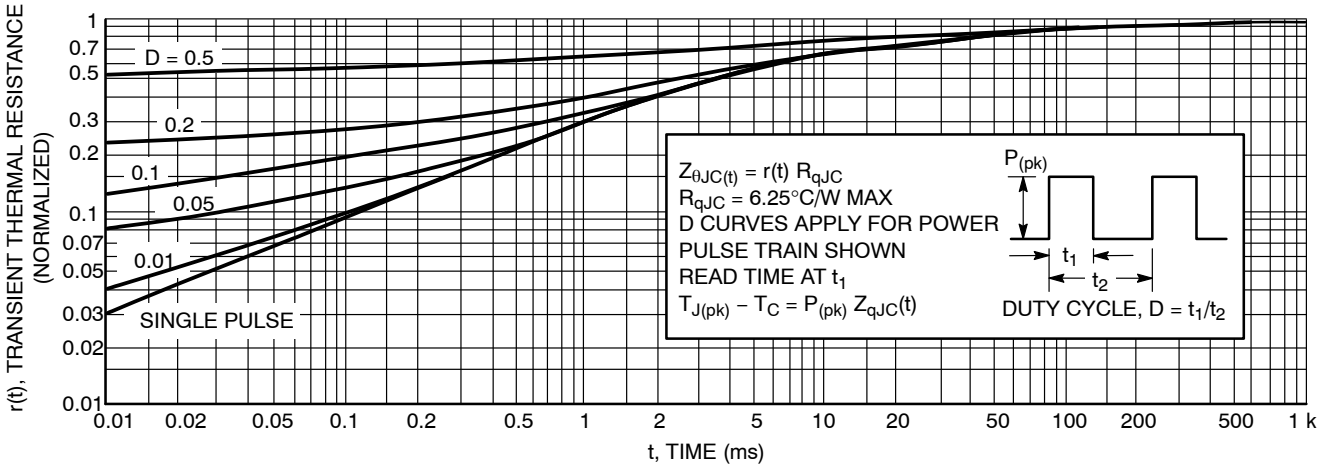


Figure 6. Thermal Response

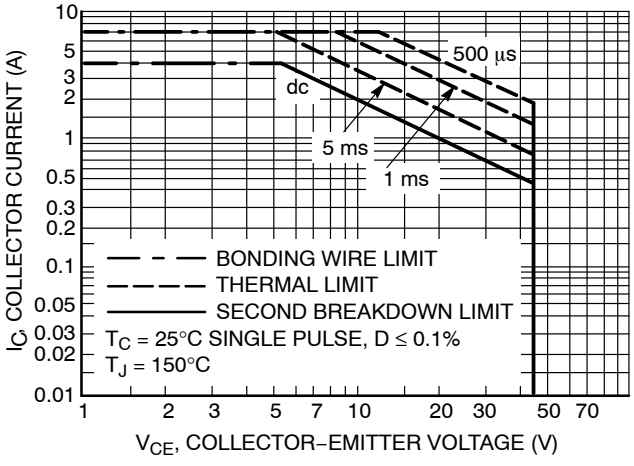


Figure 7. Maximum Rated Forward Bias

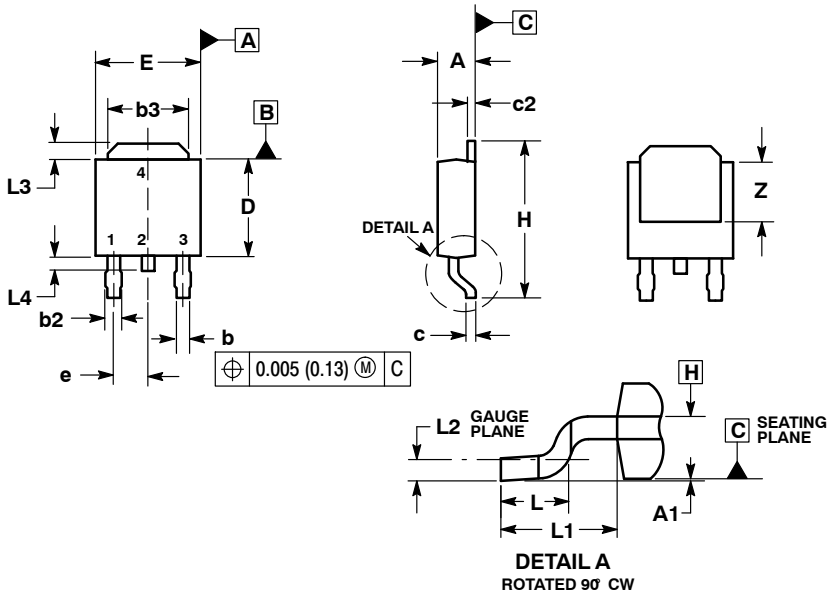
FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C−01
ISSUE D

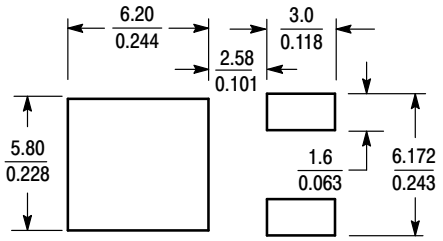


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	−−−	0.040	−−−	1.01
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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