MTH20P08
MTH20P10
MTM20P08
MTM20P10

Designer's Data Sheet

Power Field Effect Transistor

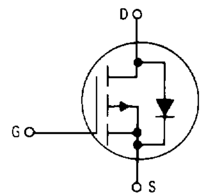
P-Channel Enhancement-Mode Silicon Gate TMOS

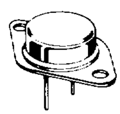
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

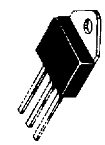
TMOS

TMOS POWER FETs
20 AMPERES
$r_{DS(on)}$ = 0.15 OHM
80 and 100 VOLTS





MTM20P08
MTM20P10
CASE 1-04
TO-204AA



MTH20P08
MTH20P10
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTM and MTH 20P08	MTM and MTH 20P10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage				
Continuous	V_{GS}	±20		Vdc
Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40		Vpk
Drain Current				Adc
Continuous	I_D	20		
Pulsed	I_{DM}	80		
Total Power Dissipation @ T_C = 25°C	P_D	125		Watts
Derate above 25°C		1		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1	
Junction to Ambient	$R_{\theta JA}$	30	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTH20P08, MTM20P08 MTH20P10, MTM20P10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3.2 3	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 10 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	950	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	45	ns
Rise Time		t_r	—	200	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	52 (Typ)	75	nC
Gate-Source Charge		Q_{gs}	22 (Typ)	—	
Gate-Drain Charge		Q_{gd}	30 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.8 (Typ)	4	Vdc
Forward Turn-On Time		t_{on}	100 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	350 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

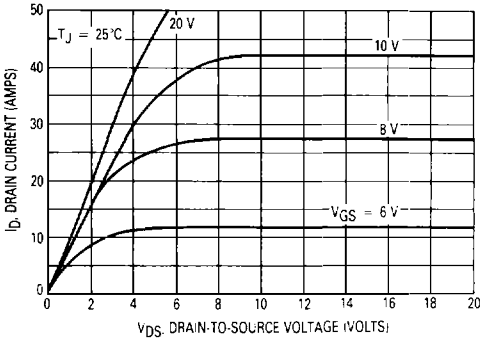

Figure 1. On-Region Characteristics

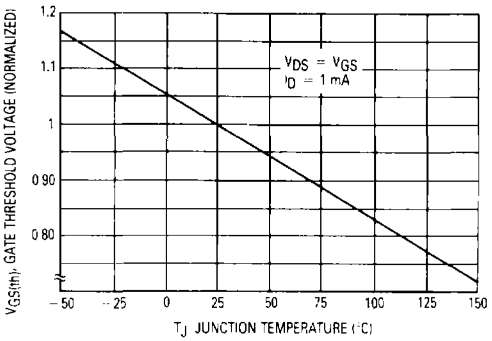

Figure 2. Gate-Threshold Voltage Variation With Temperature

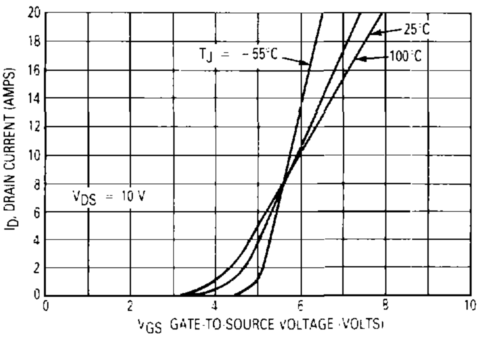

Figure 3. Transfer Characteristics

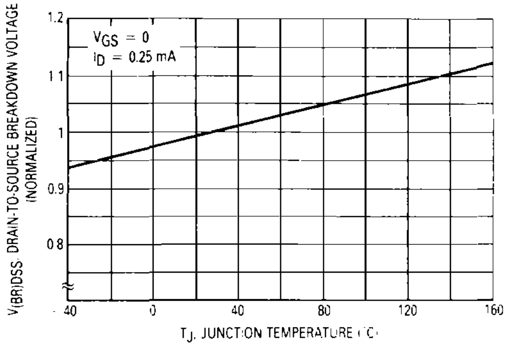

Figure 4. Breakdown Voltage Variation With Temperature

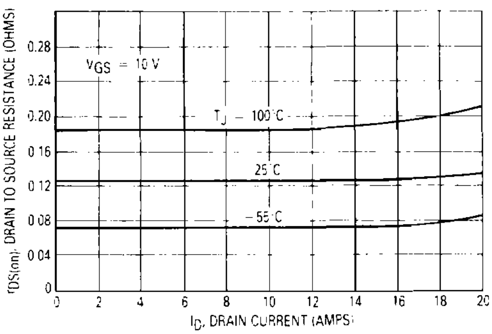

Figure 5. On-Resistance versus Drain Current

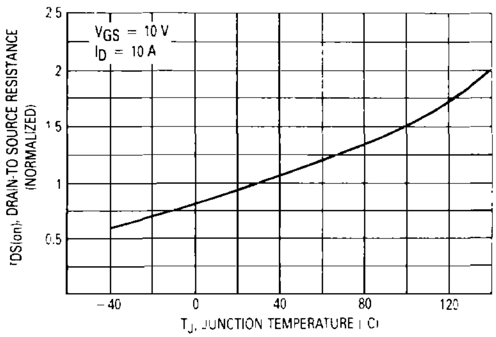

Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

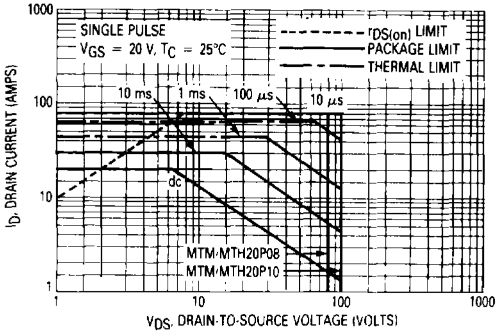


Figure 7. Maximum Rated Forward Biased Safe Operating Area

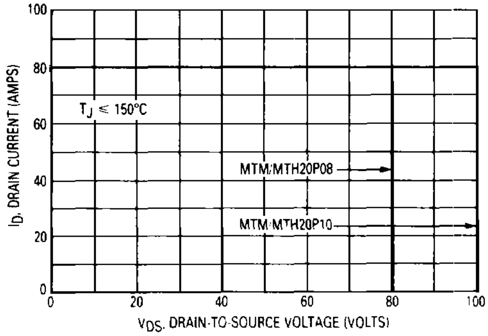


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

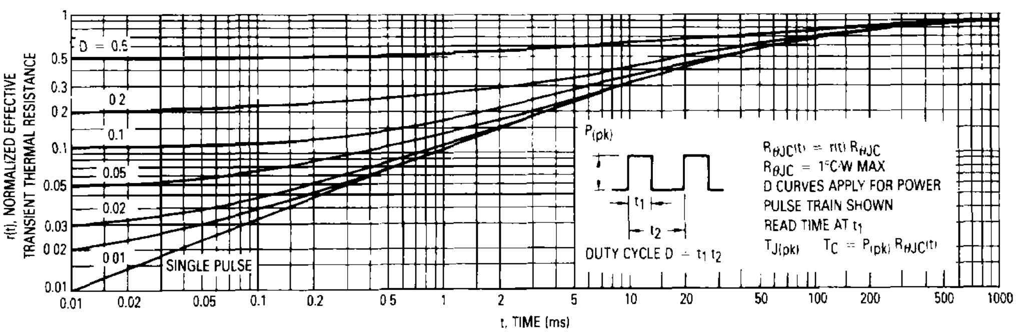


Figure 9. Thermal Response

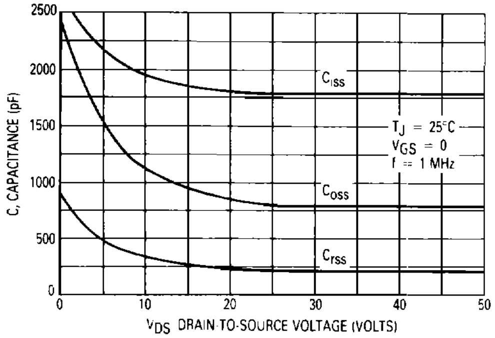


Figure 10. Capacitance Variation

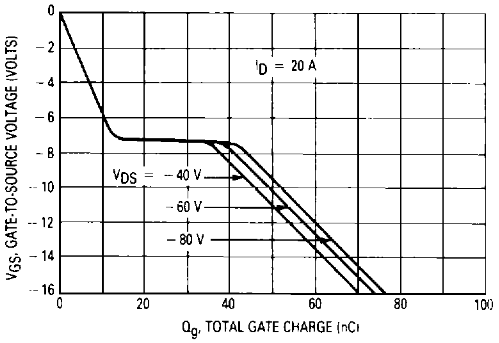


Figure 11. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

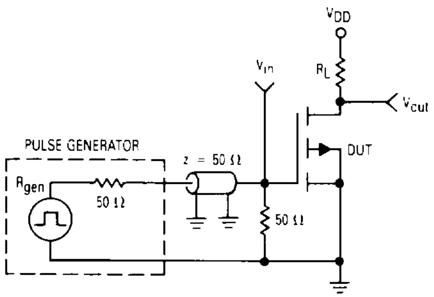


Figure 12. Switching Test Circuit

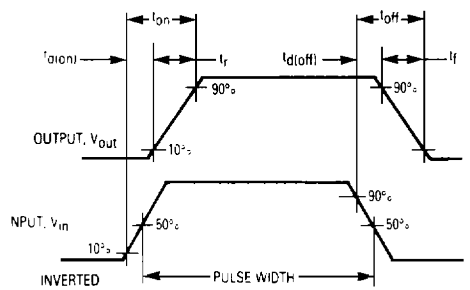
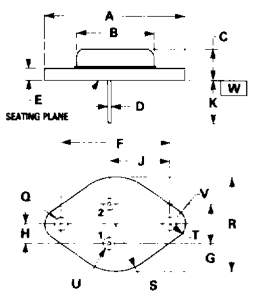


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-04
TO-204AA

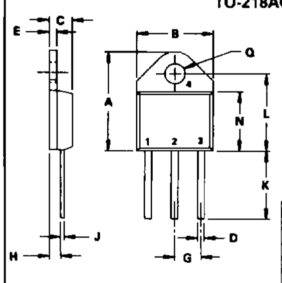


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1 550
B	—	21 08	—	0 830
C	6 35	7 62	0 250	0 300
D	0 97	1 09	0 038	0 043
E	1 40	1 78	0 055	0 070
F	30 15 BSC		1.187 BSC	
G	10 92 BSC		0.430 BSC	
H	5 46 BSC		0.215 BSC	
J	16 89 BSC		0.665 BSC	
K	11 18	12 19	0 440	0 480
Q	3 81	4 19	0 151	0 165
R	—	26.67	—	1 050
U	2 54	3.05	0 100	0 120
V	3 81	4.19	0 151	0 165

STYLE 3
PIN 1 GATE
2 SOURCE
CASE DRAIN

NOTES
1 DIAMETER V AND SURFACE W ARE DATUMS
2 POSITIONAL TOLERANCE FOR HOLE Q
⌖ | ϕ 0.25 (0 010) Ⓜ | W | V Ⓜ
3 POSITIONAL TOLERANCE FOR LEADS
⌖ | ϕ 0.30 (0 012) Ⓜ | W | V Ⓜ | Q Ⓜ

CASE 340-02
TO-218AC



STYLE 2
PIN 1. GATE
2. DRAIN
3. SOURCE
4 DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.