PHS Transceiver GaAs MMIC

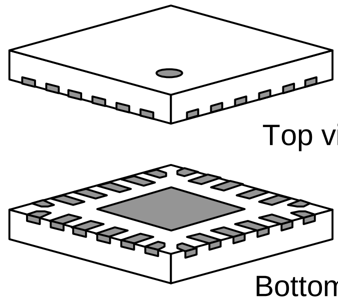
■ GENERAL DESCRIPTION

NJG1717KT2 is a GaAs multi-function MMIC composed of a power amplifier, a SPDT switch and a LNA+MIXER for Japanese PHS or WLL application.

NJG1717KT2 is operated at low voltage, and includes a low current and low distortion PA, a low insertion loss antenna switch and a low noise and high gain LNA+MIXER.

The small QFN24-T2 package is applied.

■ PACKAGE OUTLINE



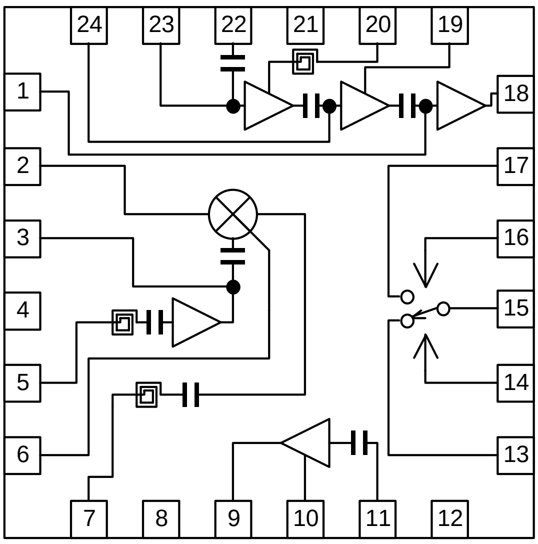
NJG1717KT2

■ FEATURES

●Supply Voltage	PA	3.0V
	SW, LNA, MIXER	2.7V
●Low current consumption	Tx mode	150mA typ.
	Rx mode	8.3mA typ.
●Ultra small & ultra thin package	QFN24-T2 (Package Size: 4.0 x 4.0 x 0.78mm)	
❍TX Mode (PA+ANT SW)		
●High Gain	39dB typ. @Pout=+20.2dBm	
●Adjacent Channel leak Power Ratio	-63dBc typ. @offset 600kHz	
❍RX Mode (ANT SW+LNA+MIXER)		
●High Conversion Gain	20.5dB typ. @ f_{RF}=1900MHz, f_{LO}=1660MHz, P_{LO}=-15dBm	
●Low noise figure	2.6dB typ. @ f_{RF}=1900MHz, f_{LO}=1660MHz, P_{LO}=-15dBm	
●High input IP3	-10dBm typ. @ f_{RF}=1900.0+1900.6MHz, f_{LO}=1660MHz	
●Image suppression ratio	36dB typ. @ f_{RF}=1900/1420MHz	

■PIN CONFIGURATION

(Top View)



Pin Connection

1.	VBB3	13.	P2
2.	IFOUT	14.	VCTL2
3.	VLO	15.	PC
4.	NC(GND)	16.	VCTL1
5.	LOIN	17.	P1
6.	BPC	18.	PAOUT
7.	MIXIN	19.	VCC2
8.	GND1	20.	VCC1
9.	LNAOUT	21.	GND3
10.	LNACAP	22.	PAIN
11.	LNAIN	23.	VBB1
12.	GND2	24.	VBB2

•Exposed PAD: GND

NOTE: Please note that any information on this catalog will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}	Iidle=140mA	6.0	V
V_{CC} Terminal Current	I_{CC}		330	mA
Control Voltage1, 2	$V_{CTL1, 2}$		7.5	V
LNA Voltage	V_{LNA}		5.0	V
MIXER Voltage	V_{MIX}		5.0	V
Local Amplifier Voltage	V_{LO}		5.0	V
Input Power 1 (PA IN terminal)	P_{PAIN}	VCC=3.0V, Iidle=140mA	+3.0	dBm
Input Power 2 (ANT terminal)	P_{ANTIN}	V_{LNA}=V_{MIX}=V_{LO}=2.7V	-5.0	dBm
Input Power 3 (LOCAL IN terminal)	P_{LOIN}	V_{LNA}=V_{MIX}=V_{LO}=2.7V	+10.0	dBm
Power Dissipation	P_D	At on PCB(FR4), Tj=150°C	620	mW
Operating Temperature	T_{opr}		-40~+85	°C
Storage Temperature	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS 1 (DC)

GENERAL CONDITIONS: T_a=+25°C, V_{CC}=3.0V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=2.7V, V_{LNA}=V_{MIX}=V_{LO}=2.7V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7	3.0	5.0	V
Base Voltage	V_{BB}	I_{CC}=150mA	1.2	1.6	2.0	V
Idle Current	Iidle	PA IN: No signal	-	140	200	mA
Base Current	I_{BB}	PA IN: No signal	-	1.0	1.4	mA
Operating Voltage (Low)	$V_{CTL(L)}$		-0.2	0	0.2	V
Operating Voltage (High)	$V_{CTL(H)}$		2.5	2.7	6.5	V
Control Current	I_{CTL}	PA IN, RF, LO: No signal	-	8.0	14.0	uA
LNA Voltage	V_{LNA}		2.5	2.7	4.5	V
LNA Operating Current	I_{LNA}	P_{RF}, P_{LO}=OFF	-	2.8	3.5	mA
MIXER Operating Voltage	V_{MIX}		2.5	2.7	4.5	V
MIXER Current	I_{MIX}	P_{RF}, P_{LO}=OFF	-	4.6	5.7	mA
Local Amplifier Voltage	V_{LO}		2.5	2.7	4.5	V
Local Amplifier Operating Current	I_{LO}	P_{RF}, P_{LO}=OFF	-	0.9	1.3	mA

■ ELECTRICAL CHARACTERISTICS 2 (TX: PA+ANT SW)

GENERAL CONDITIONS: T_a=+25°C, V_{CC}=3.0V, V_{CTL1}=2.7V, V_{CTL2}=0V, Icc=150mA, f_{RF}=1900MHz, P_{OUT}=+20.2dBm, Z_s=Z_l=50Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	freq		1880	1900	1920	MHz
V_{CC} Terminal Current	I_{CC}		-	150	-	mA
Power Gain	Gp		36	39	-	dB
Gain Flatness	Gflat $_{TX}$	f_{RF}=1880~1920MHz	-	0.5	1.0	dB
Pout at 1dB Gain Compression Point	$P_{-1dB\ TX}$		+19	+21	-	dBm
Adjacent Channel leak Power Ratio1	ACPR1	Pin: π/4QPSK, Burst off, offset 600kHz	-	-63	-55	dBc
Adjacent Channel leak Power Ratio2	ACPR2	Pin: π/4QPSK, Burst off, offset 900kHz	-	-70	-60	dBc
2nd Harmonics 3rd Harmonics	Phm		-	-35	-30	dBc
Occupied bandwidth	OBW		-	250	275	kHz
PA IN VSWR	VSWR1	Small signal PA IN terminal	-	1.5	2.0	
ANT VSWR (Transmit active)	VSWR2	Small signal ANT terminal	-	1.5	2.0	

■ TRUTH TABLE

Control Voltage: “High”=$V_{CTL(H)}$, “Low”=$V_{CTL(L)}$

Pass	VCTL1	VCTL2
PC(ANT)-P1(TX)	High	Low
PC(ANT)-P2(RX)	Low	High

■ ELECTRICAL CHARACTERISTICS 3 (RX: ANT SW+LNA+MIXER)

GENERAL CONDITIONS: T_a=+25°C, V_{CTL1}=0V, V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=2.7V, f_{RF}=1900MHz, f_{LO}=1660MHz, P_{RF}=-45dBm, P_{LO}=-15dBm, Z_s=Z_l=50Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	freq		1880	1900	1920	MHz
LNA Operating Current	ILNA		-	2.8	3.5	mA
MIXER Operating Current	IMIX		-	4.6	5.7	mA
LNA Operating Current	ILO		-	0.9	1.3	mA
Conversion Gain	Gc		16.5	20.5	-	dB
Gain Flatness	$Gflat_{RX}$	f_{RF}=1880~1920MHz	-	0.5	1.5	dB
Noise Figure	NF	SSB	-	2.6	3.5	dB
Input 3rd order Intercept Point	IIP3	f_{RF}=1900.0+1900.6MHz	-14	-10	-	dBm
Pin at 1dB Gain Compression Point	$P_{-1dB\ RX}$		-25.5	-21.5	-	dBm
Image suppression ratio	IMR	f_{RF}=1900/1420MHz	31	36	-	dB
1/2 IF suppression ratio	1/2IFR	f_{RF}=1900/1780MHz	49	55	-	dB
2×LO-IF suppression ratio	SPR1	f_{RF}=1900/3080MHz	39	47	-	dB
2×LO+IF suppression ratio	SPR2	f_{RF}=1900/3560MHz	24	62	-	dB
LO to ANT leak	Plk		-	-55	-45	dBm
ANT VSWR (Receive active)	VSWR3		-	1.5	2.0	
LOCAL IN VSWR	VSWR4		-	2.0	2.5	
IF OUT VSWR	VSWR5		-	1.5	2.0	

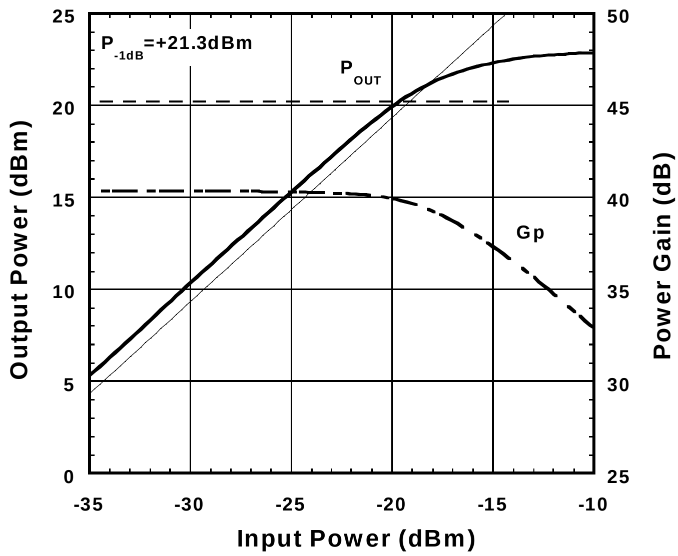
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	VBB3	This terminal is for base bias supply of the 3rd stage of power amplifier. Operation current of the power amplifier is adjusted by changing the bias voltage applied to this terminal. Please connect bypass capacitors C12 and C13 with ground plane close to this terminal. Please connect pin 23 and pin 24, and connect the resistor R1 for temperature characteristic compensation of PA gain.
2	IFOUT	IF signal output terminal. The IF signal is output through external matching circuit connected to this terminal. Please connect inductances L6, L7 and power supply as shown in the application circuit, since this terminal is also the terminal of mixer power supply.
3	VLO	Power supply terminal for local amplifier. Please place L5 and C8 shown in the application circuit, very close to this terminal.
4	NC(GND)	Nonconnection terminal. Please connect with Ground terminal.
5	LOIN	Local signal input terminal connected to the local amplifier. An external matching circuit is required.
6	BPC	Terminal to connect to the external bypass capacitor of mixer. The bypass capacitor C7 shown in the application circuit should be connected to this terminal as close as possible.
7	MIXIN	Input terminal of RF signal to the mixer. An external matching circuit is required.
8	GND1	Ground terminal (0V)
9	LNAOUT	Output terminal of LNA. The RF signal from LNA goes out through external matching circuit connected to this terminal. Please connect inductances L3, L4 and power supply as shown in the application circuit, since this terminal is also the terminal of LNA power supply.
10	LNACAP	Terminal to connect to an external bypass capacitor of LNA. The bypass capacitor C4 shown in the application circuit should be connected to this terminal as close as possible.
11	LNAIN	RF input terminal of LNA. An external matching circuit is required.
12	GND2	Ground terminal (0V)
13	P2	RF port. This terminal is one of ports of SPDT SW. This terminal connects to PC terminal (pin 15) when logical high voltage signal is supplied to VCTL2 (pin 14) and logical low voltage signal is supplied to VCTL1 (pin 16). External capacitor C3 is required to block the DC bias voltage of internal circuit.

No.	SYMBOL	DESCRIPTION
14	VCTL2	Control port. Please connect bypass capacitor C2 with ground plane close to this terminal.
15	PC	Common RF port. The terminal PC is connected to the terminal P1 or the terminal P2 by the voltage supplied to the terminal VCTL1 and VCTL2. In order to block the DC bias voltage of internal circuit, external capacitor C1 is required.
16	VCTL1	Control port. Please connect bypass capacitor C24 with ground plane close to this terminal.
17	P1	RF port. This terminal is one of ports of SPDT SW. This terminal connects to PC terminal (pin 15) when logical low voltage signal is supplied to VCTL2 (pin 14) and logical high voltage signal is supplied to VCTL1 (pin 16). External capacitor C23 is required to block the DC bias voltage of internal circuit.
18	PAOUT	Output terminal of power amplifier. The RF signal from power amplifier goes out through an external matching circuit connected to this terminal. Moreover, this terminal should be connected to DC power supply through inductor L9 shown in the application circuit, since it is the terminal for power supply of the 3rd stage of Power Amplifier.
19	VCC2	This terminal is for DC power supply of the 2nd stage of power amplifier. Please place bypass capacitors C17 and C18 between this terminal and GND as near as possible.
20	VCC1	This terminal is for DC power supply of the 1st stage of power amplifier. Please place bypass capacitors C15 and C16 between this terminal and GND as near as possible.
21	GND3	Ground terminal (0V)
22	PAIN	RF input terminal of power amplifier. An external matching circuit is required.
23	VBB1	This terminal is for base bias supply of the 1st stage of power amplifier. Operation current of the power amplifier is adjusted by changing the bias voltage applied to this terminal. Please connect bypass capacitors C12 and C13 with ground plane close to this terminal. Please connect pin 24 and pin 1, and connect the resistor R1 for temperature characteristic compensation of PA gain.
24	VBB2	This terminal is for base bias supply of the 2nd stage of Power Amplifier. Operation current of the power amplifier is adjusted by changing the bias voltage applied to this terminal. Please connect bypass capacitors C12 and C13 with ground plane close to this terminal. Please connect pin 23 and pin 1, and connect the resistor R1 for temperature characteristic compensation of PA gain.

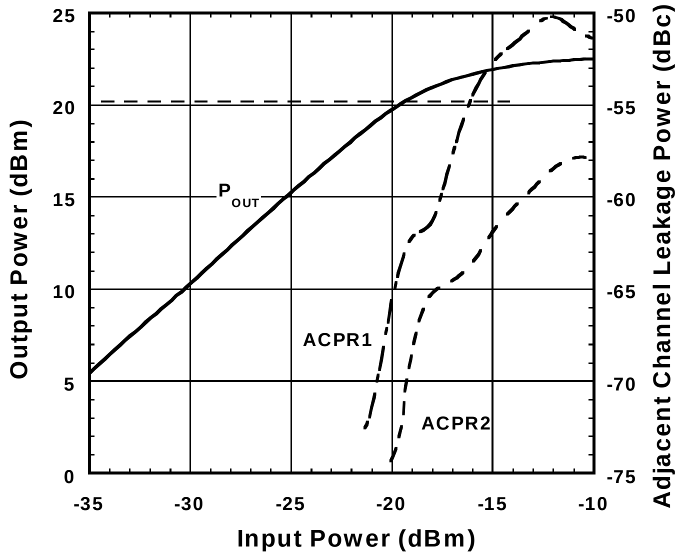
■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)

Output Power, Gp vs. Input Power



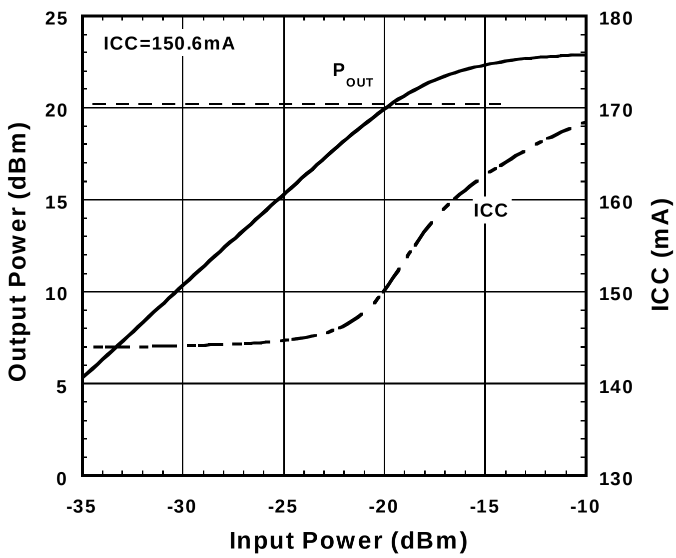
Condition
f_{RF}=1900MHz(CW), Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA)
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

Output Power, ACPR vs. Input Power



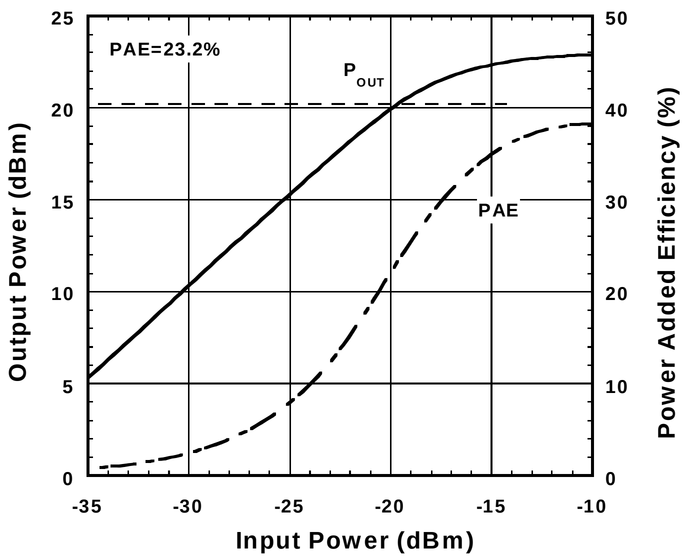
Condition
f_{RF}=1900MHz(π/4DQPSK), Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA)
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

Output Power, ICC vs. Input Power



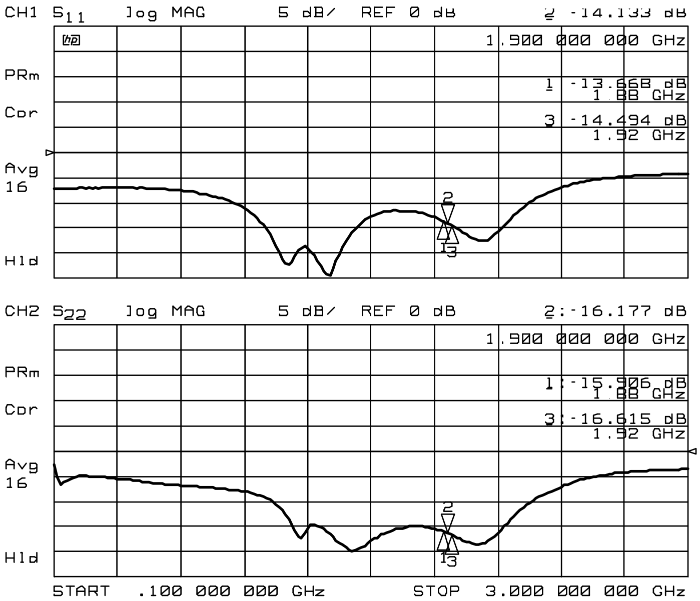
Condition
f_{RF}=1900MHz(CW), Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA)
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

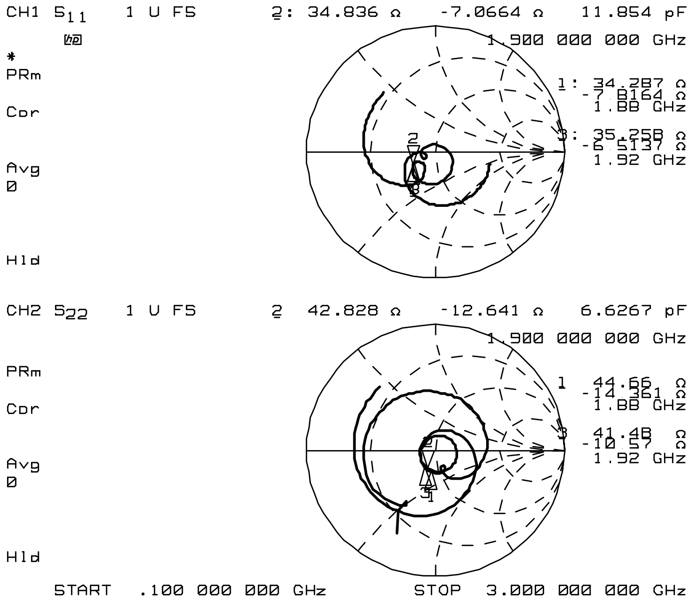
Output Power, PAE vs. InputPower



Condition
f_{RF}=1900MHz(CW), Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA)
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)





Condition
Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA)
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

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V_{BB}=Const. (@I_{CC}=150mA)
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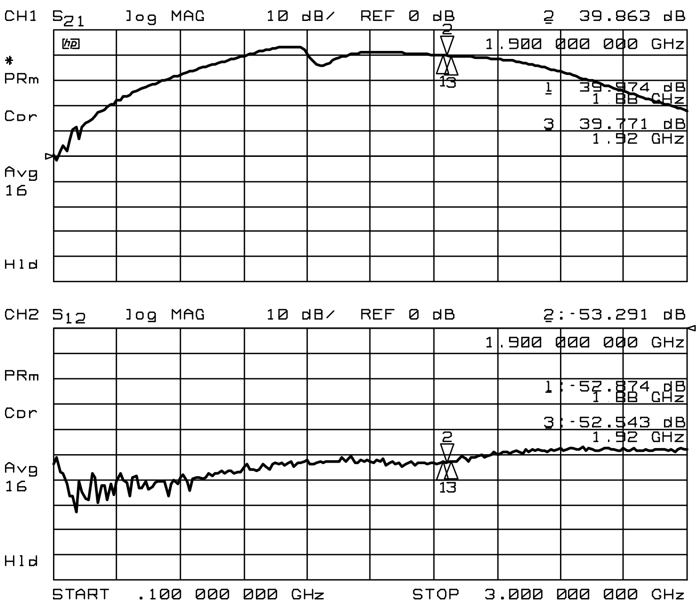
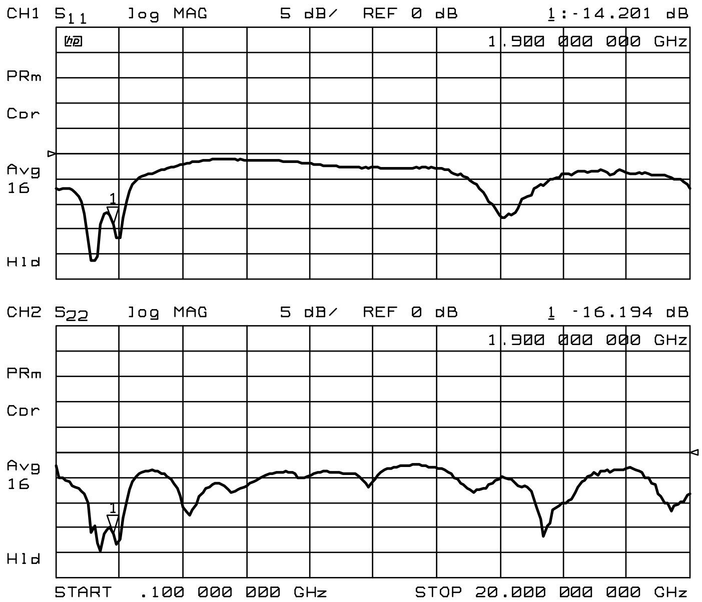
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V



Condition
Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA)
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)



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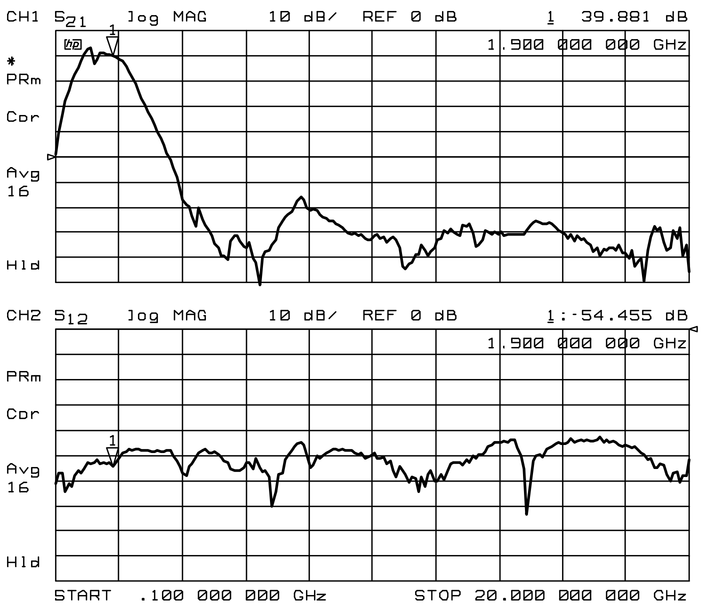

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V_{BB}=Const. (@I_{CC}=150mA)
V_{CC}=3.0V, V_{CTL1} =2.7V
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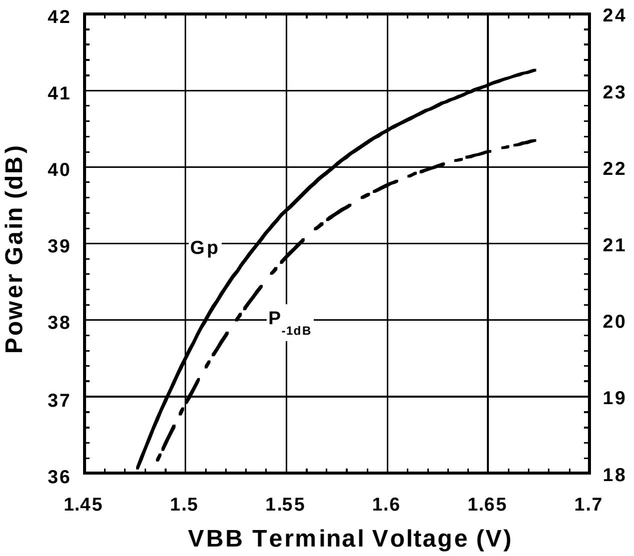
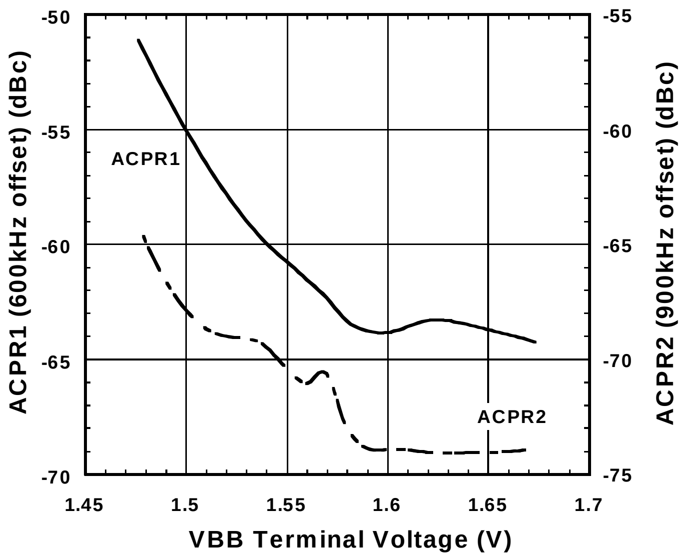
■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)

Gp, P_{-1dB} vs. VBB Terminal Voltage



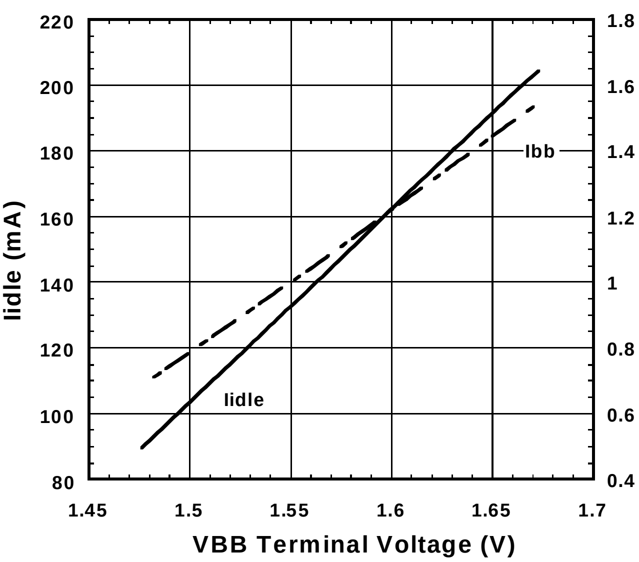
Condition
f_{RF}=1900MHz(CW)
P_{OUT}=+20.2dBm, Ta=+25°C
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

ACPR1, ACPR2 vs. VBB Terminal Voltage



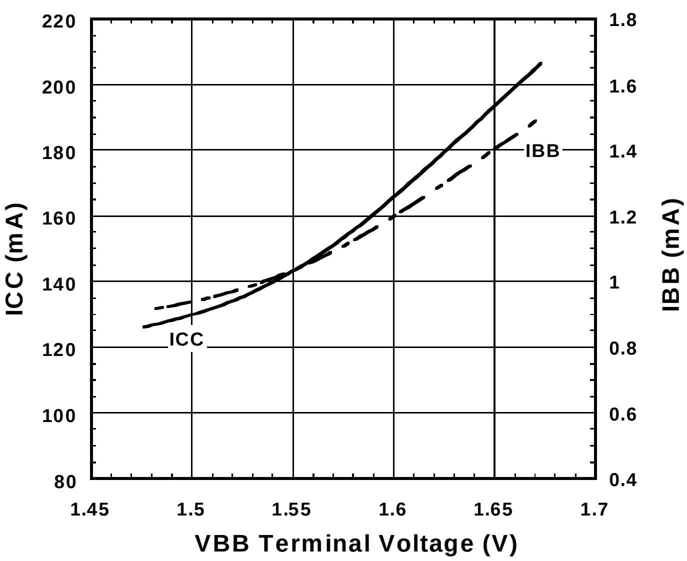
Condition
f_{RF}=1900MHz(π/4DQPSK)
P_{OUT}=+20.2dBm, Ta=+25°C
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

Iidle, Ibb vs. VBB Terminal Voltage



Condition
Ta=+25°C
V_{CC}=3.0V, V_{CTL1} =2.7V
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

ICC, IBB vs. VBB Terminal Voltage



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P_{OUT}=+20.2dBm, Ta=+25°C
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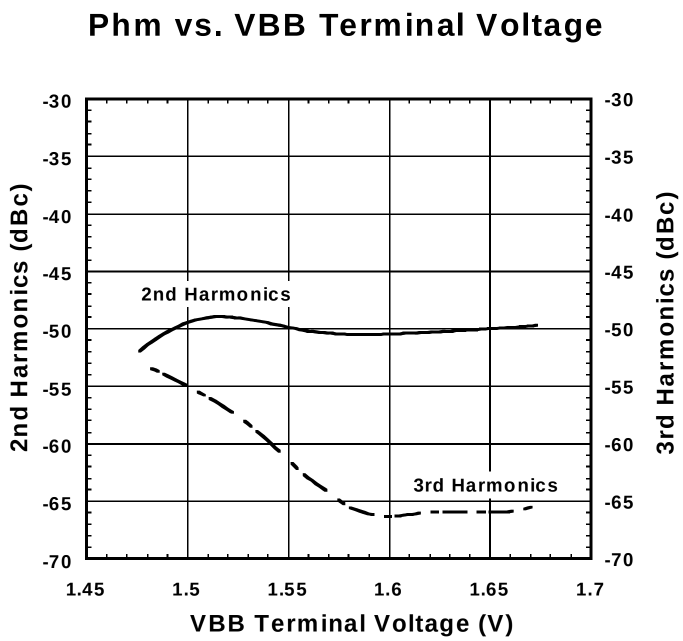
■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)



Condition
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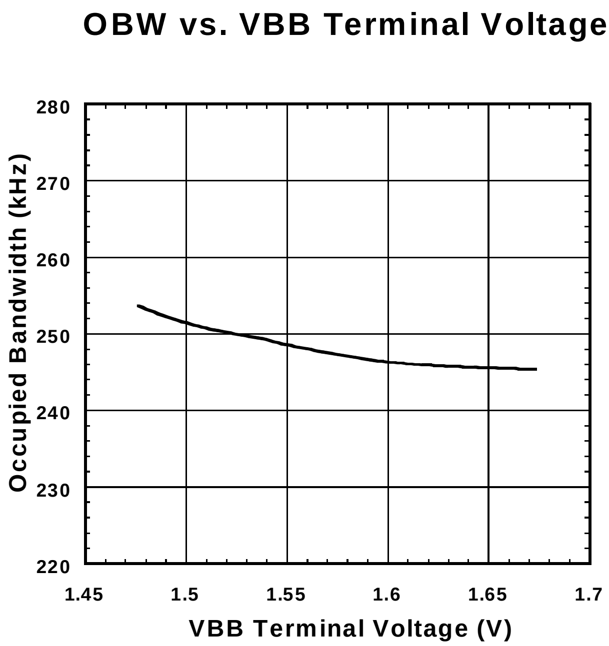
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V



Condition
f_{RF}=1900MHz(π/4DQPSK)
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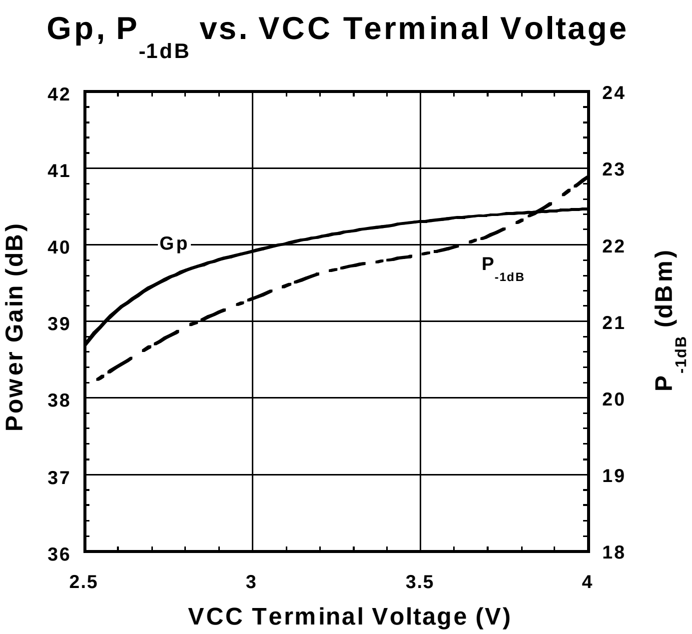
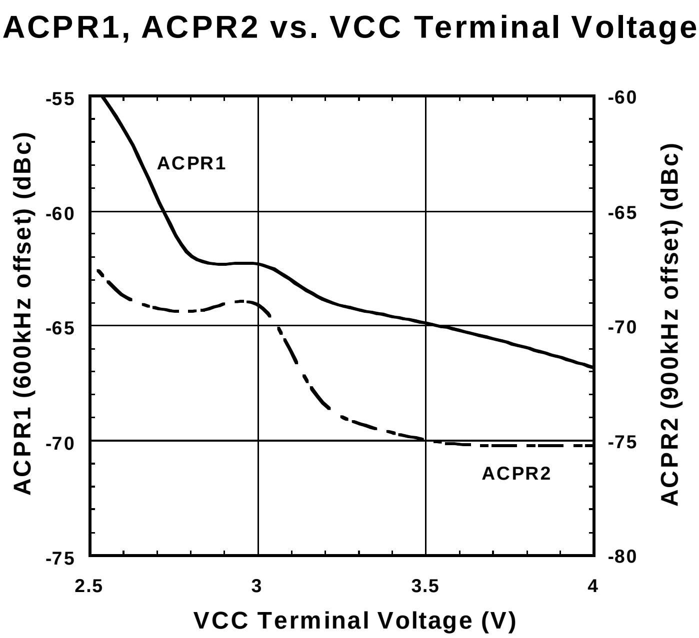
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

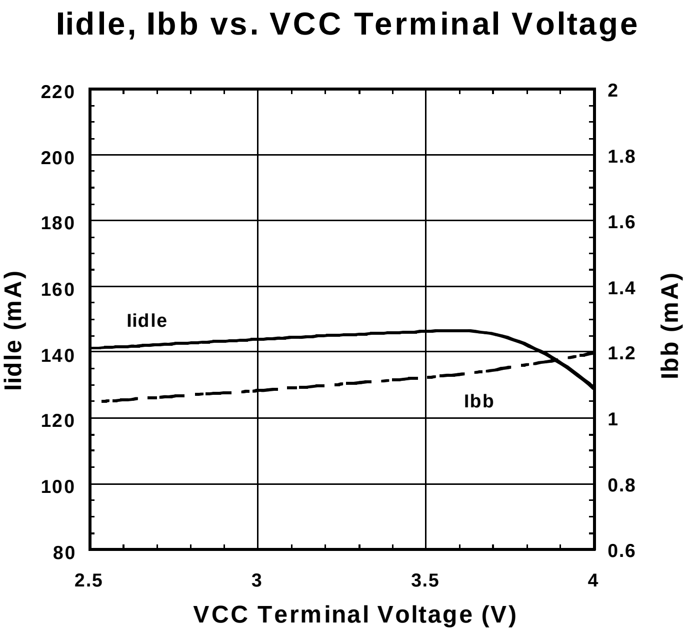


Condition
f_{RF}=1900MHz(CW)
P_{OUT}=+20.2dBm, Ta=+25°C
V_{BB}=Const.(@Iidle=144mA,V_{CC}=3.0V)
V_{CTL1} =2.7V, V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

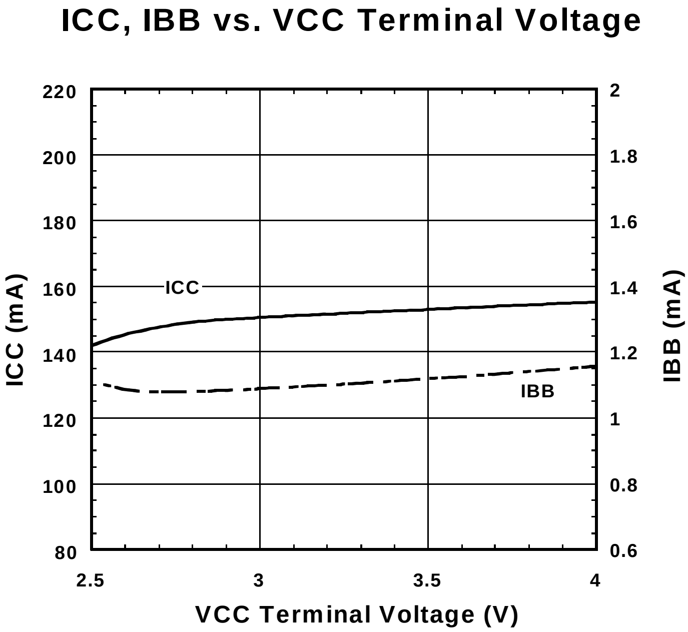


Condition
f_{RF}=1900MHz(π/4DQPSK)
P_{OUT}=+20.2dBm, Ta=+25°C
V_{BB}=Const.(@Iidle=144mA,V_{CC}=3.0V)
V_{CTL1} =2.7V, V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

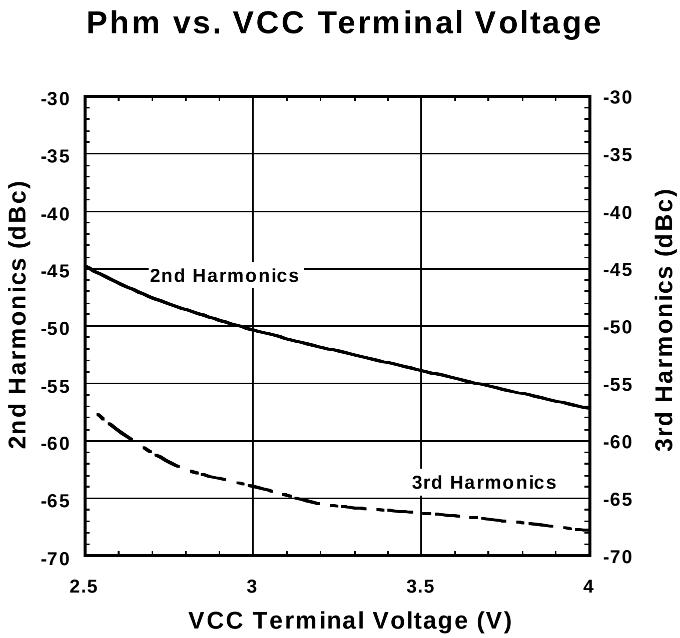
■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)



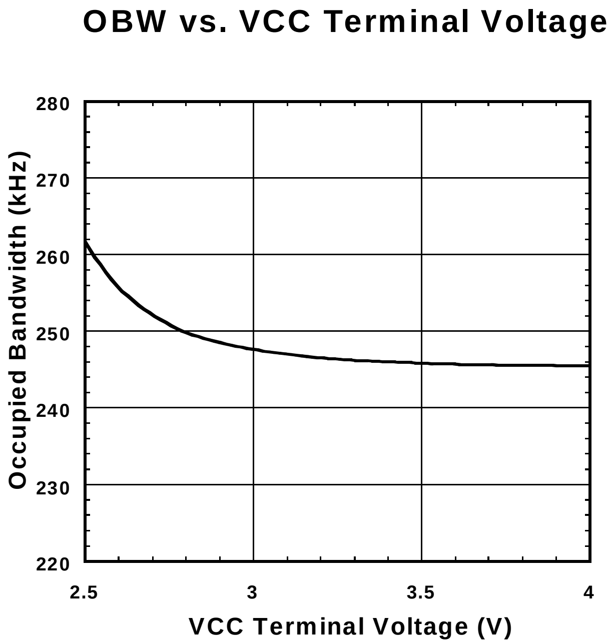
Condition
Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA,V_{CC}=3.0V)
V_{CTL1} =2.7V, V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V



Condition
f_{RF}=1900MHz(CW)
P_{OUT}=+20.2dBm, Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA,V_{CC}=3.0V)
V_{CTL1} =2.7V, V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V



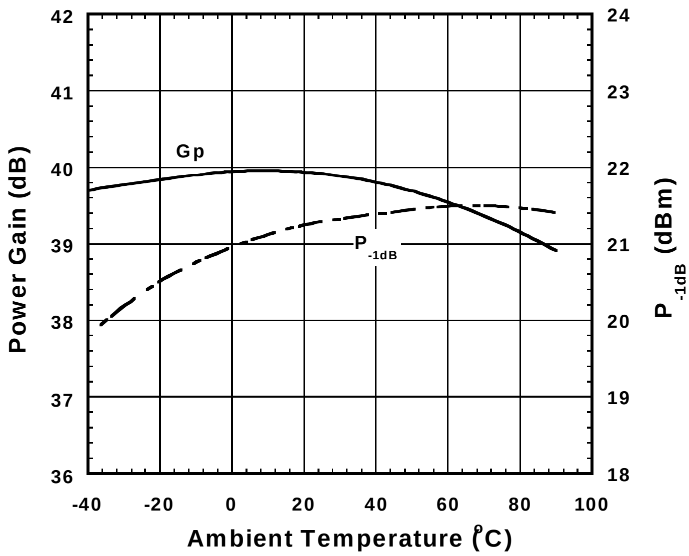
Condition
f_{RF}=1900MHz(CW)
P_{OUT}=+20.2dBm, Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA,V_{CC}=3.0V)
V_{CTL1} =2.7V, V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V



Condition
f_{RF}=1900MHz(π/4DQPSK)
P_{OUT}=+20.2dBm, Ta=+25°C
V_{BB}=Const. (@I_{CC}=150mA,V_{CC}=3.0V)
V_{CTL1} =2.7V, V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

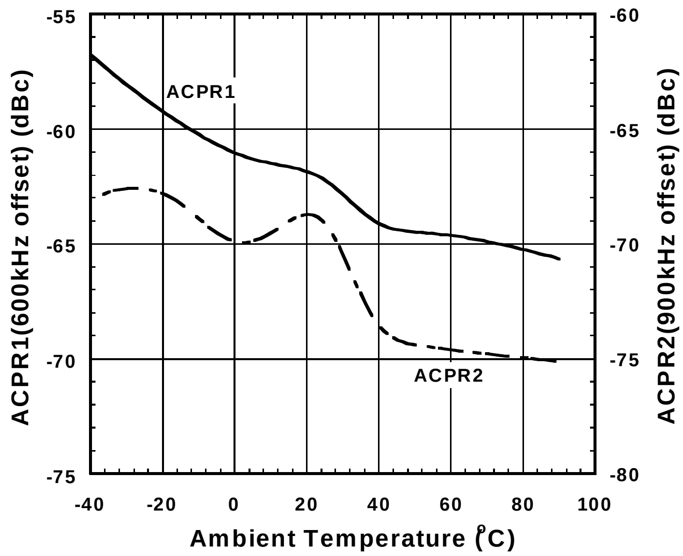
■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)

Gp, P_{-1dB} vs. Temperature



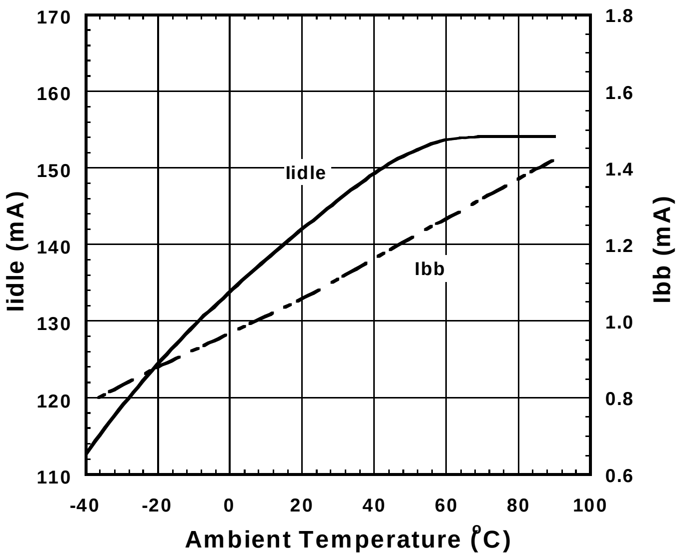
Condition
f_{RF}=1900MHz(CW)
P_{OUT}=+20.2dBm
V_{BB}=Const. (@I_{CC}=150mA,Ta=+25°C)
V_{CC}=3.0V, V_{CTL1} =2.7V,
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

ACPR1, ACPR2 vs. Temperature



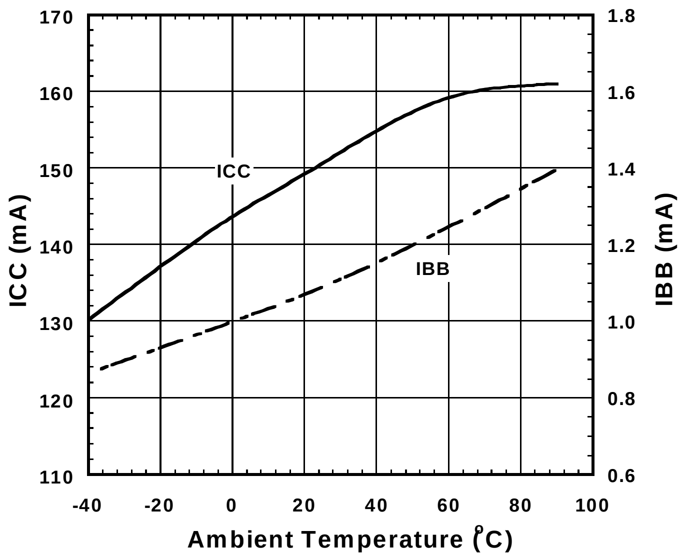
Condition
f_{RF}=1900MHz(π/4DQPSK)
P_{OUT}=+20.2dBm
V_{BB}=Const. (@I_{CC}=150mA,Ta=+25°C)
V_{CC}=3.0V, V_{CTL1} =2.7V,
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

Iidle, Ibb vs. Temperature



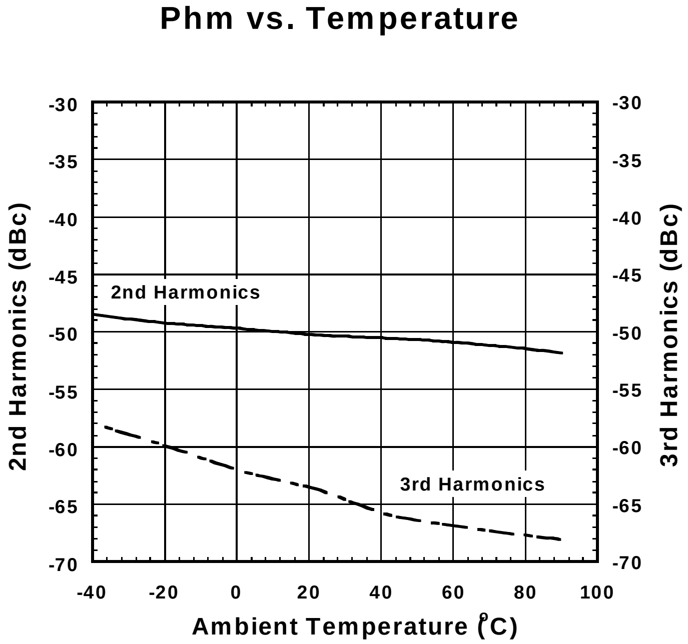
Condition
V_{BB}=Const. (@I_{CC}=150mA,Ta=+25°C)
V_{CC}=3.0V, V_{CTL1} =2.7V,
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

ICC, IBB vs. Temperature

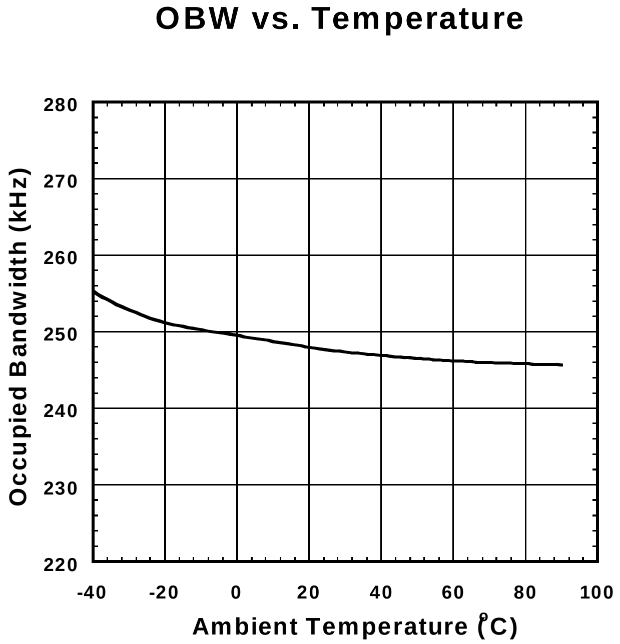


Condition
f_{RF}=1900MHz(CW)
P_{OUT}=+20.2dBm
V_{BB}=Const. (@I_{CC}=150mA,Ta=+25°C)
V_{CC}=3.0V, V_{CTL1} =2.7V,
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

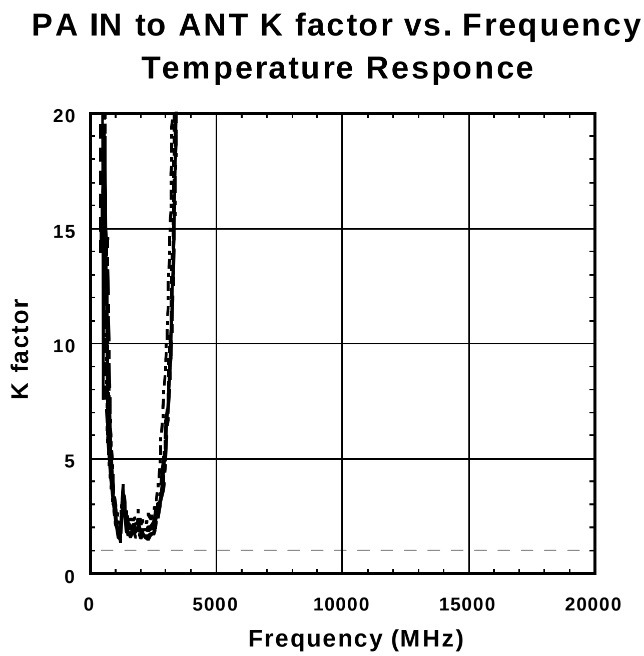
■ TYPICAL CHARACTERISTICS (TX: PA + ANT SW SECTION)



Condition
f_{RF}=1900MHz(CW)
P_{OUT}=+20.2dBm
V_{BB}=Const. (@I_{CC}=150mA,Ta=+25°C)
V_{CC}=3.0V, V_{CTL1} =2.7V,
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V



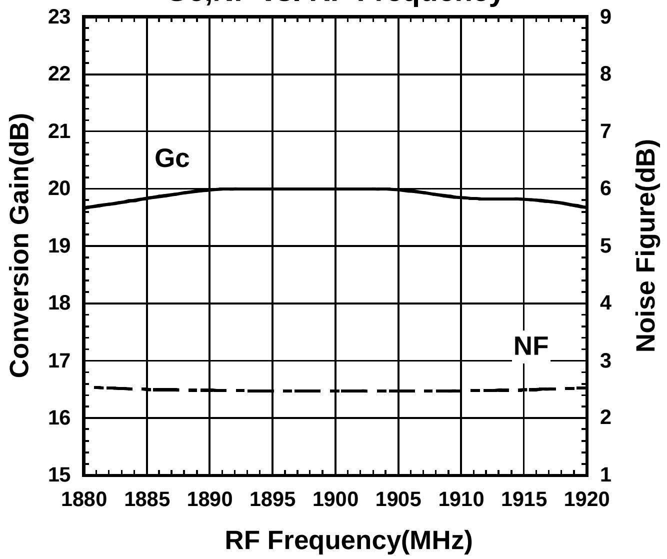
Condition
f_{RF}=1900MHz(π/4DQPSK)
P_{OUT}=+20.2dBm
V_{BB}=Const. (@I_{CC}=150mA,Ta=+25°C)
V_{CC}=3.0V, V_{CTL1} =2.7V,
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V



Condition
f_{RF}=1900MHz(CW)
Ta=-40~+90 °C
V_{BB}=Const. (@I_{CC}=150mA,Ta=+25°C)
V_{CC}=3.0V, V_{CTL1} =2.7V,
V_{CTL2}=V_{LNA}=V_{MIX}=V_{LO}=0V

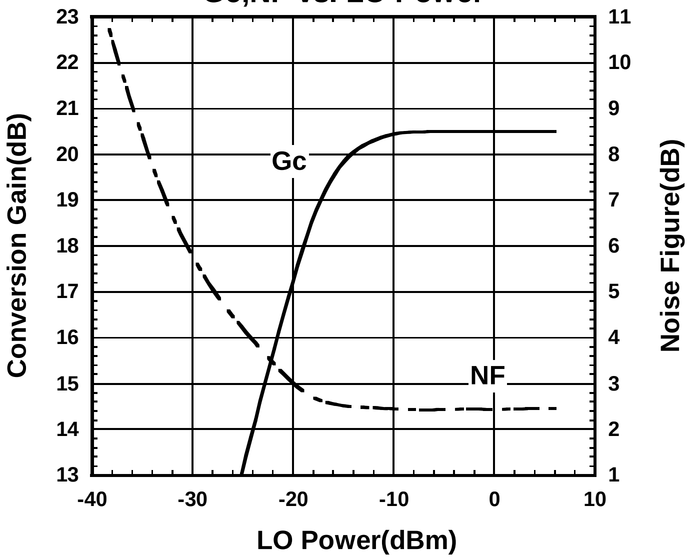
■ TYPICAL CHARACTERISTICS (RX: ANT SW + LNA + MIXER SECTION)

Gc,NF vs. RF Frequency



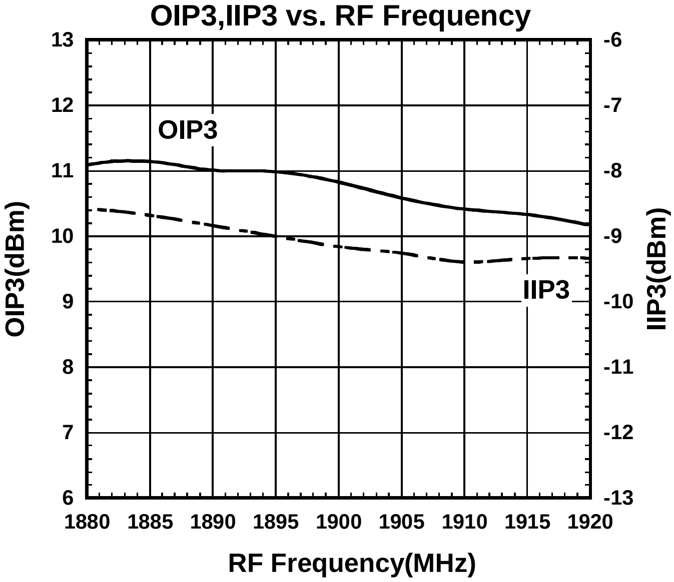
Condition
f_{IF}=240MHz
f_{RF}=1880~1920MHz, P_{RF}=-45dBm
Lower LOCAL, P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

Gc,NF vs. LO Power



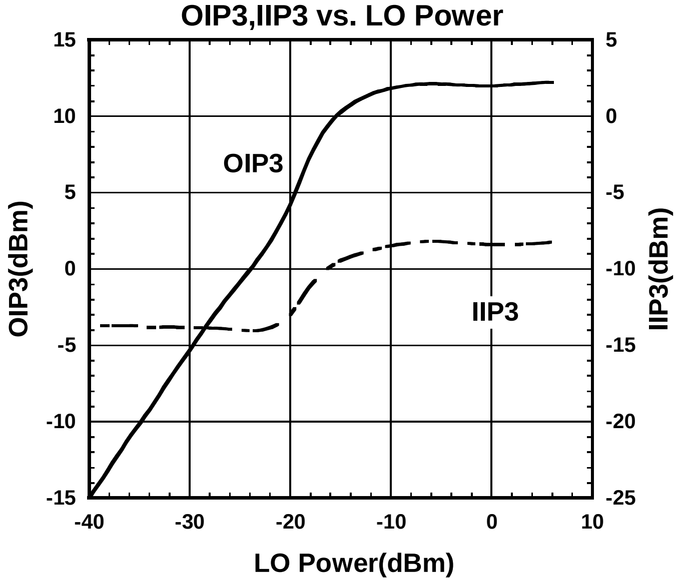
Condition
f_{IF}=240MHz
f_{RF}=1900MHz, P_{RF}=-45dBm
f_{LO}=1660MHz
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

OIP3,IIP3 vs. RF Frequency



Condition
f_{IF}=240MHz
f_{RF}=1880~1920MHz, P_{RF}=-40dBm
$f_{RF\ OFFSET}$=600kHz
Lower LOCAL, P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

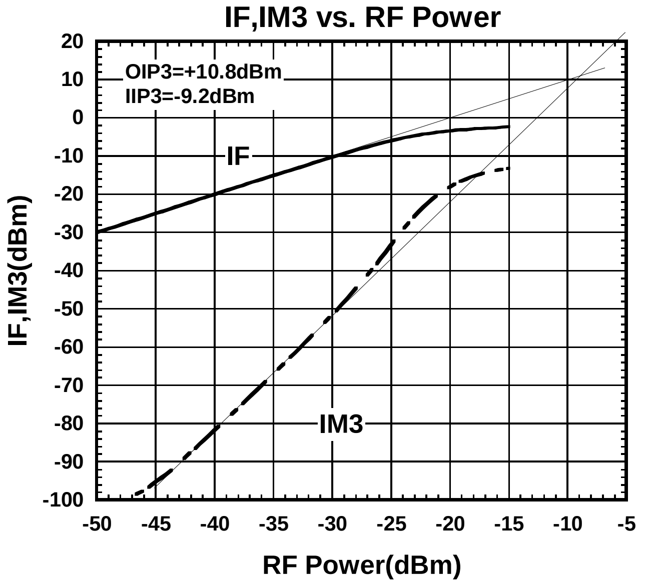
OIP3,IIP3 vs. LO Power



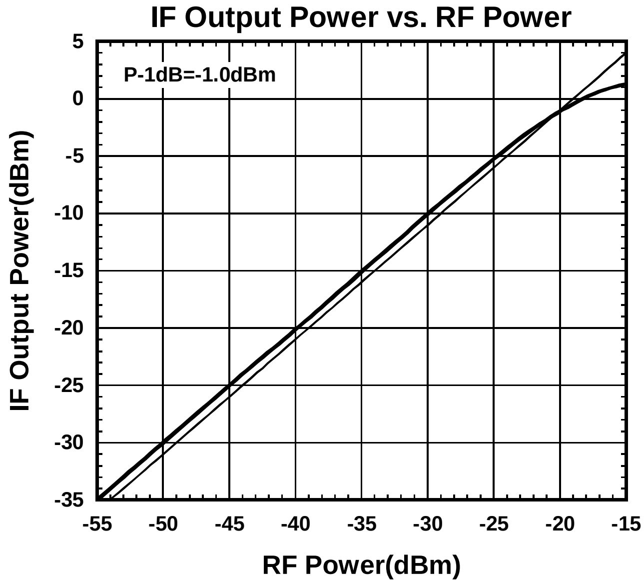
Condition
f_{IF}=240MHz
f_{RF}=1900.0+1900.6MHz, P_{RF}=-40dBm
f_{LO}=1660MHz
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

OIP3=(3xIF-IM3)/2
IIP3=OIP3-Gc

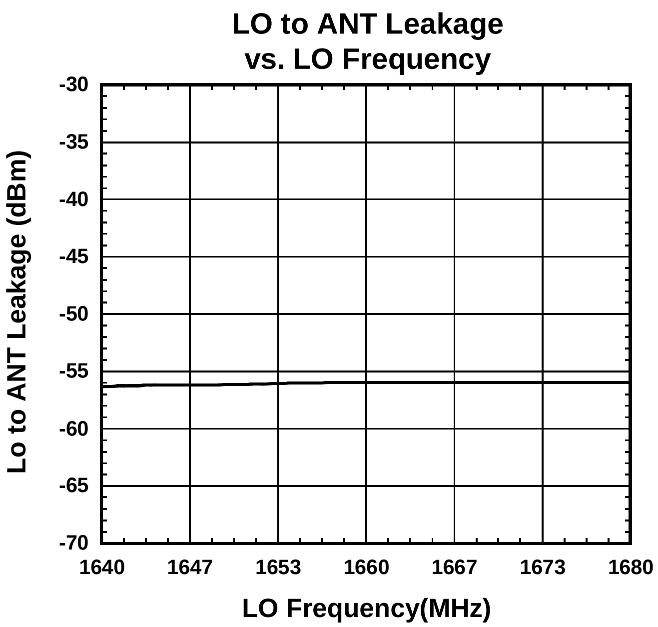
■ TYPICAL CHARACTERISTICS (RX: ANT SW + LNA + MIXER SECTION)



Condition
f_{IF}=240MHz
f_{RF}=1900.0+1900.6MHz
f_{LO}=1660MHz, P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

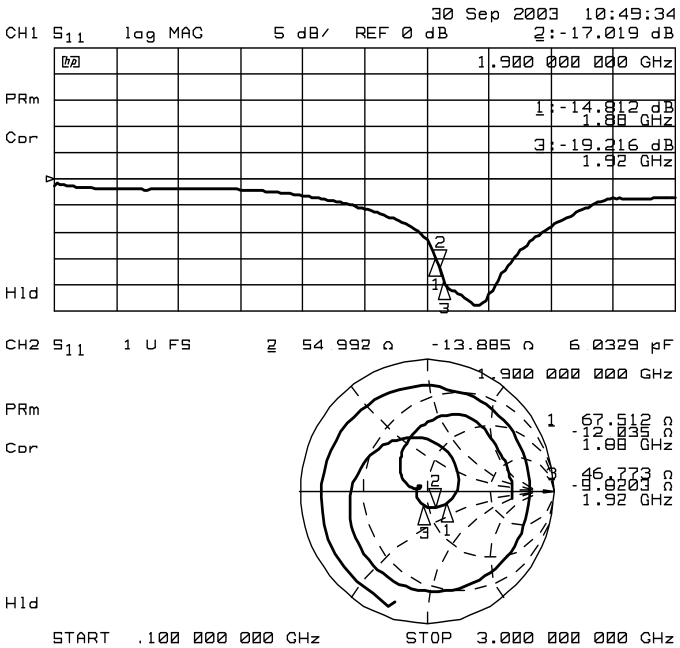


Condition
f_{IF}=240MHz
f_{RF}=1900MHz
f_{LO}=1660MHz, P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

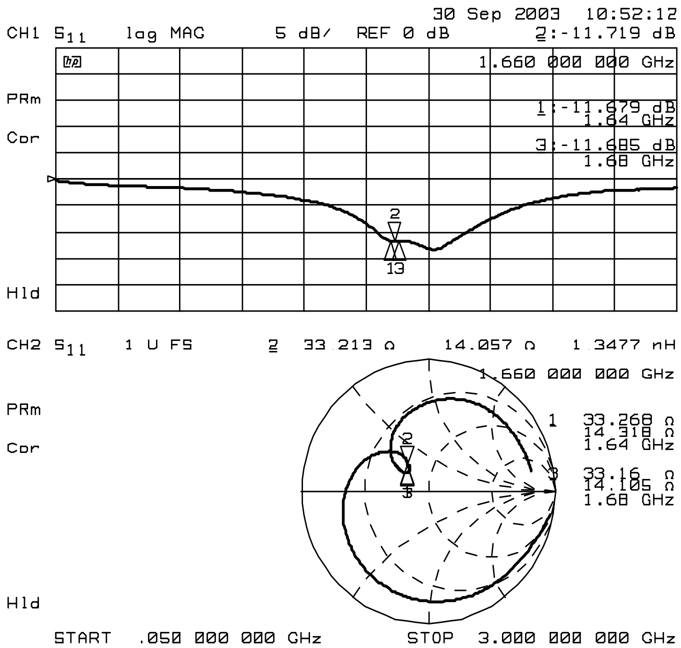


Condition
IF OUT 50Ω term
P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

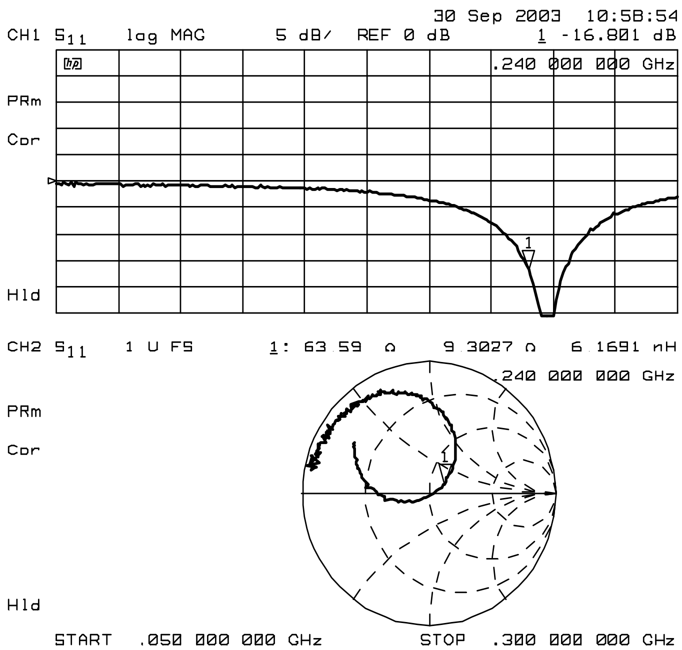
■ TYPICAL CHARACTERISTICS (RX: ANT SW + LNA + MIXER SECTION)



ANT Impedance
Condition
P_{LO}=-15dBm
IF OUT 50Ω term
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

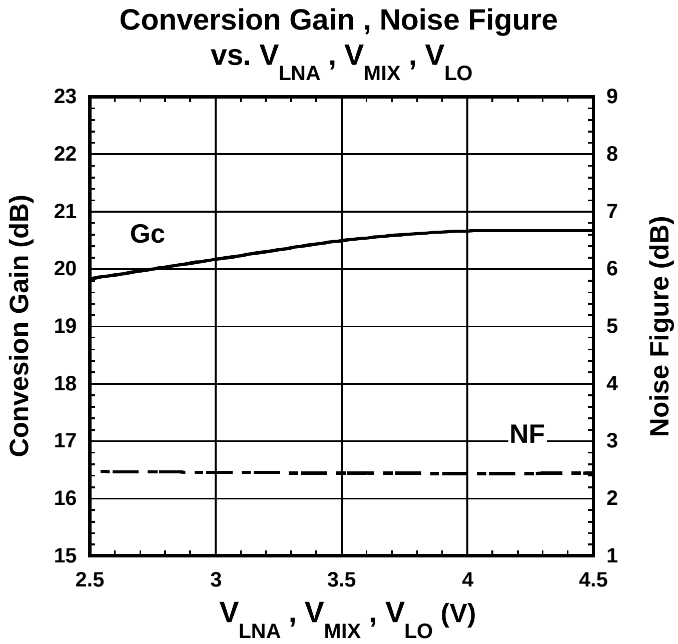


LOCAL IN Impedance
Condition
ANT, IF OUT 50Ω term
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

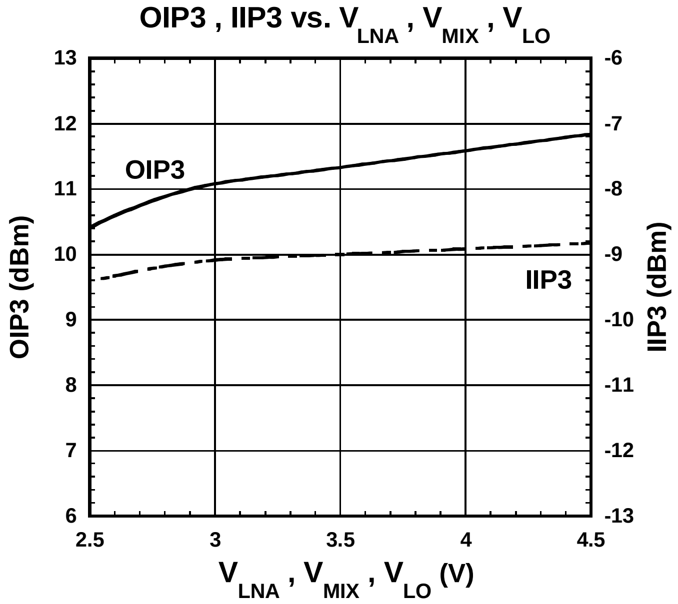


IF OUT Impedance
Condition
P_{LO}=-15dBm
ANT 50Ω term
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

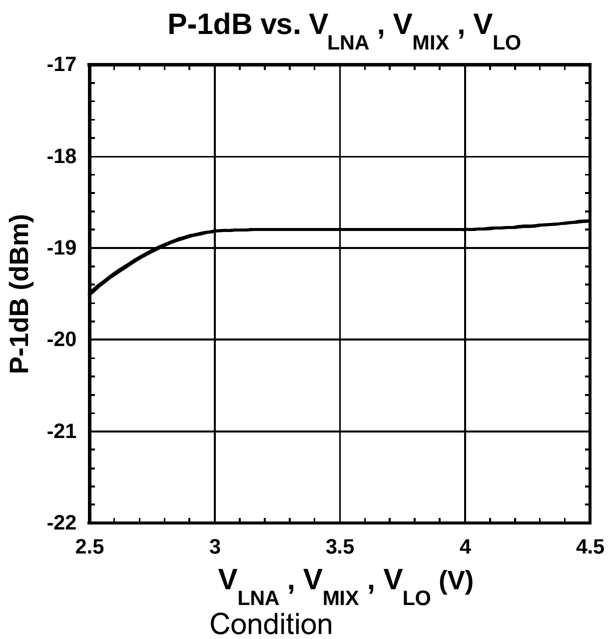
■ **TYPICAL CHARACTERISTICS (RX: ANT SW + LNA + MIXER SECTION)**



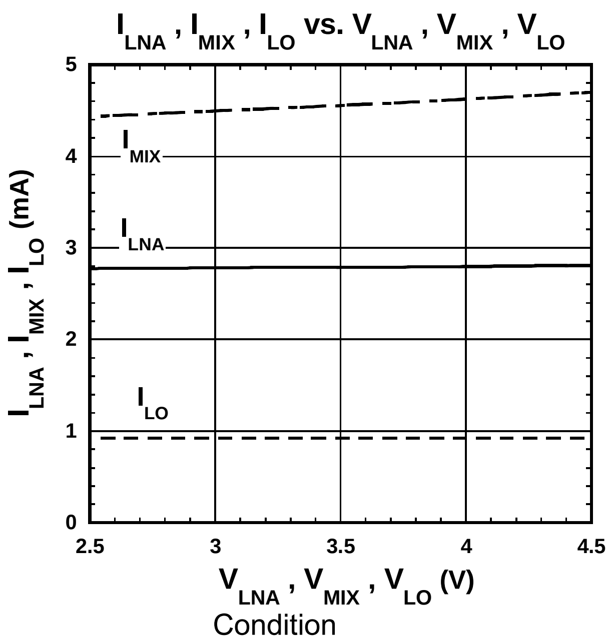
Condition
f_{IF}=240MHz
f_{RF}=1900MHz, P_{RF}=-45dBm
f_{LO}=1660MHz, P_{LO}=-15dBm
V_{CTL1}=0V



Condition
f_{IF}=240MHz
f_{RF}=1900MHz, P_{RF}=-40dBm
f_{LO}=1660MHz, P_{LO}=-15dBm
V_{CTL1}=0V



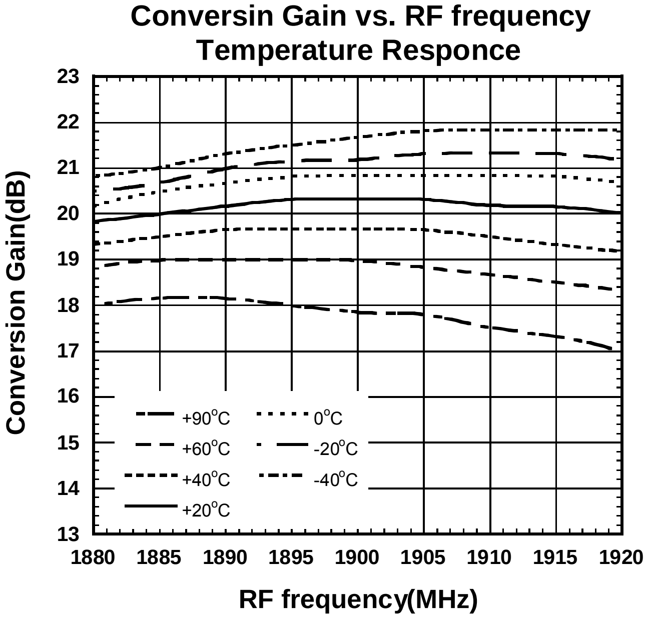
Condition
f_{IF}=240MHz
f_{RF}=1900MHz, P_{RF}=-45dBm
f_{LO}=1660MHz, P_{LO}=-15dBm
V_{CTL1}=0V



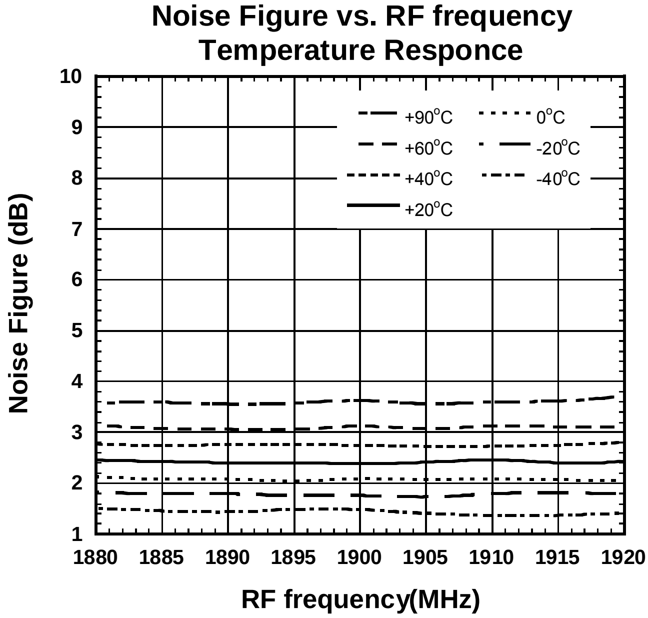
Condition
f_{IF}=240MHz
f_{RF}=1900MHz, P_{RF}=-45dBm
f_{LO}=1660MHz, P_{LO}=-15dBm
V_{CTL1}=0V

OIP3=(3xIF-IM3)/2
IIP3=OIP3-Gc

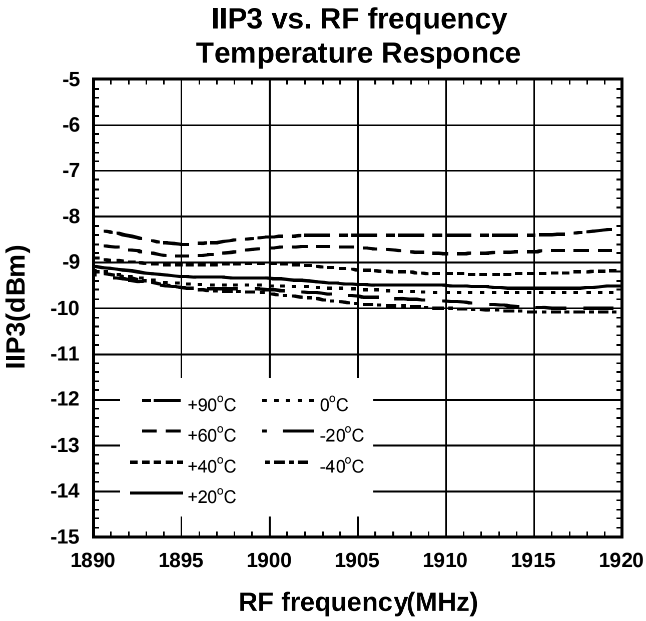
■ TYPICAL CHARACTERISTICS (RX: ANT SW + LNA + MIXER SECTION)



Condition
f_{IF}=240MHz
f_{RF}=1880~1920MHz, P_{RF}=-45dBm
Lower LOCAL, P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V



Condition
f_{IF}=240MHz
f_{RF}=1880~1920MHz
Lower LOCAL, P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

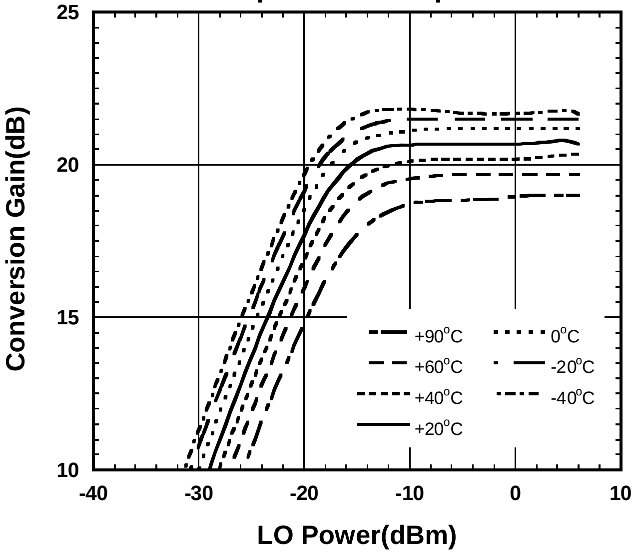


Condition
f_{IF}=240MHz
f_{RF}=1880~1920MHz, P_{RF}=-40dBm
$f_{RF\ OFFSET}$=600kHz
Lower LOCAL, P_{LO}=-15dBm
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

OIP3=(3xIF-IM3)/2
IIP3=OIP3-Gc

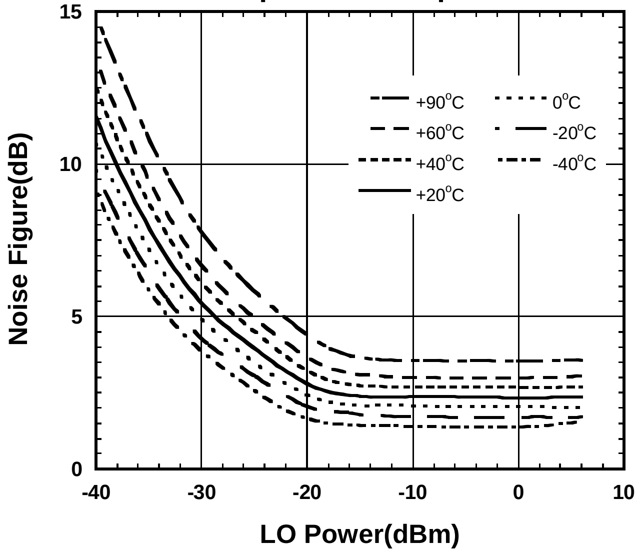
■ TYPICAL CHARACTERISTICS (RX: ANT SW + LNA + MIXER SECTION)

**Conversion Gain vs. LO Power
Temperature Responce**



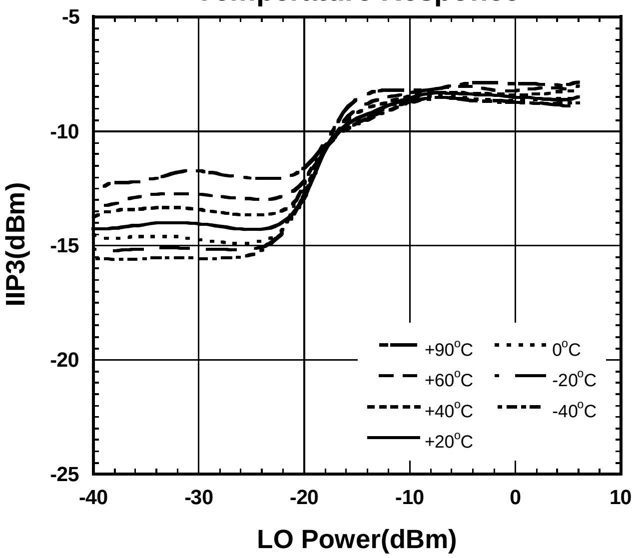
Condition
f_{IF}=240MHz
f_{RF}=1900MHz, P_{RF}=-45dBm
f_{LO}=1660MHz
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

**Noise Figure vs. LO Power
Temperature Responce**



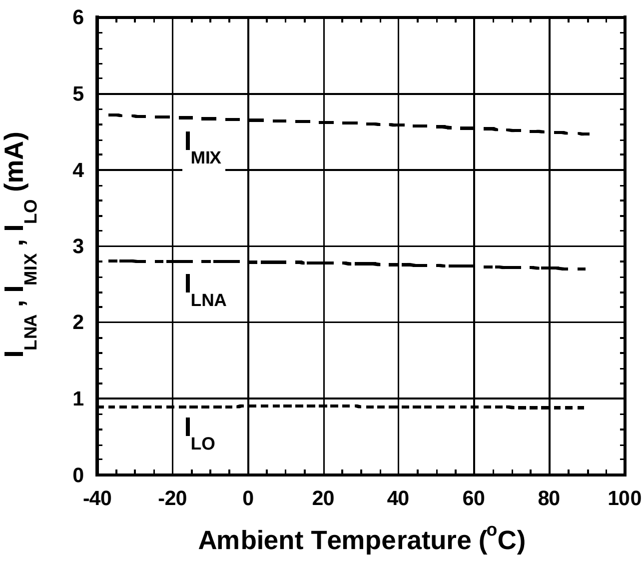
Condition
f_{IF}=240MHz
f_{RF}=1900MHz
f_{LO}=1660MHz
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

**IIP3 vs. LO Power
Temperature Responce**



Condition
f_{IF}=240MHz
f_{RF}=1900MHz, P_{RF}=-40dBm
$f_{RF\ OFFSET}$=600kHz
f_{LO}=1660MHz
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

I_{LNA} , I_{MIX} , I_{LO} vs. Temperature

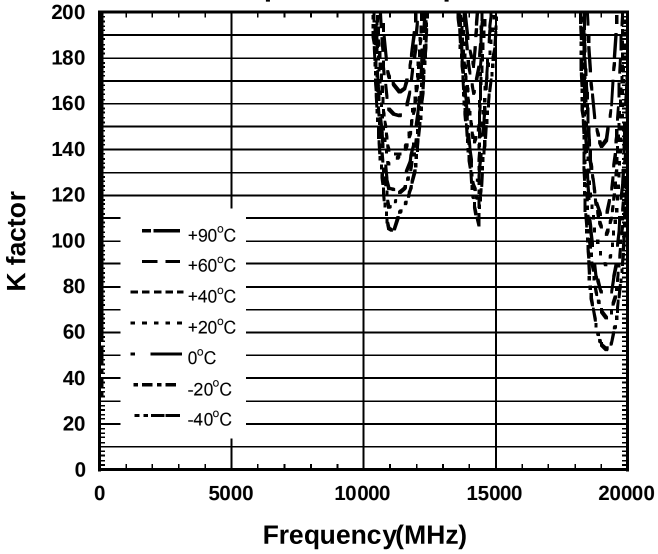


Condition
V_{LNA}=V_{MIX}=V_{LO}=2.7V

OIP3=(3xIF-IM3)/2
IIP3=OIP3-Gc

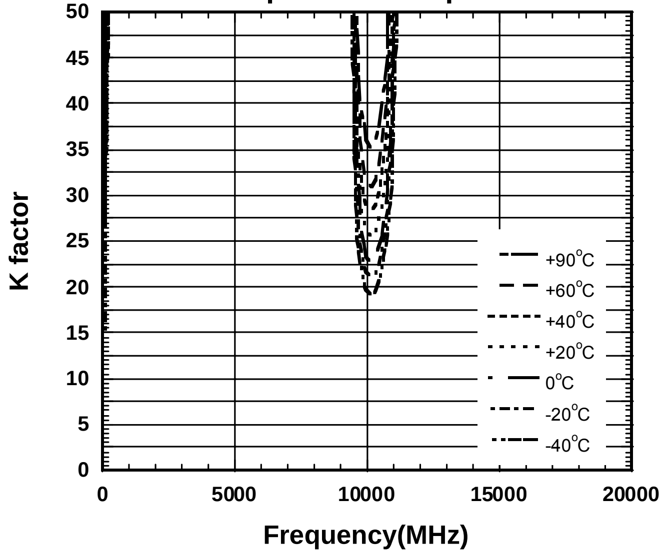
■ TYPICAL CHARACTERISTICS (RX: ANT SW + LNA + MIXER SECTION)

ANT to LOCAL IN K factor vs. Frequency
Temperature Responce



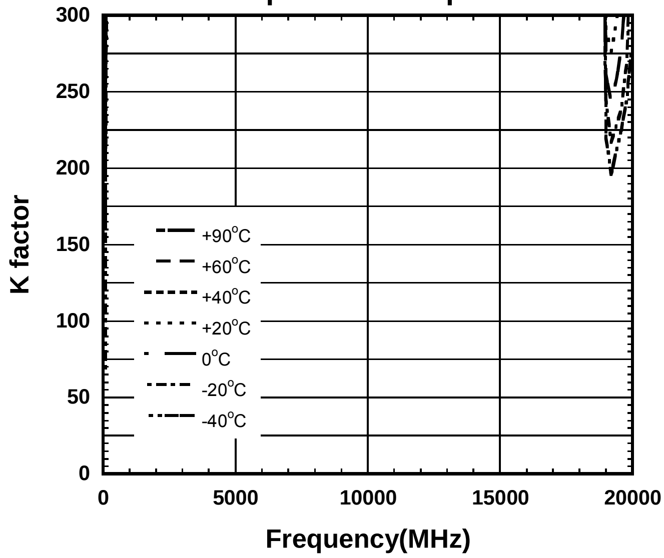
Condition
IF OUT 50Ω term
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

LOCAL IN to IF OUT K factor vs. Frequency
Temperature Responce



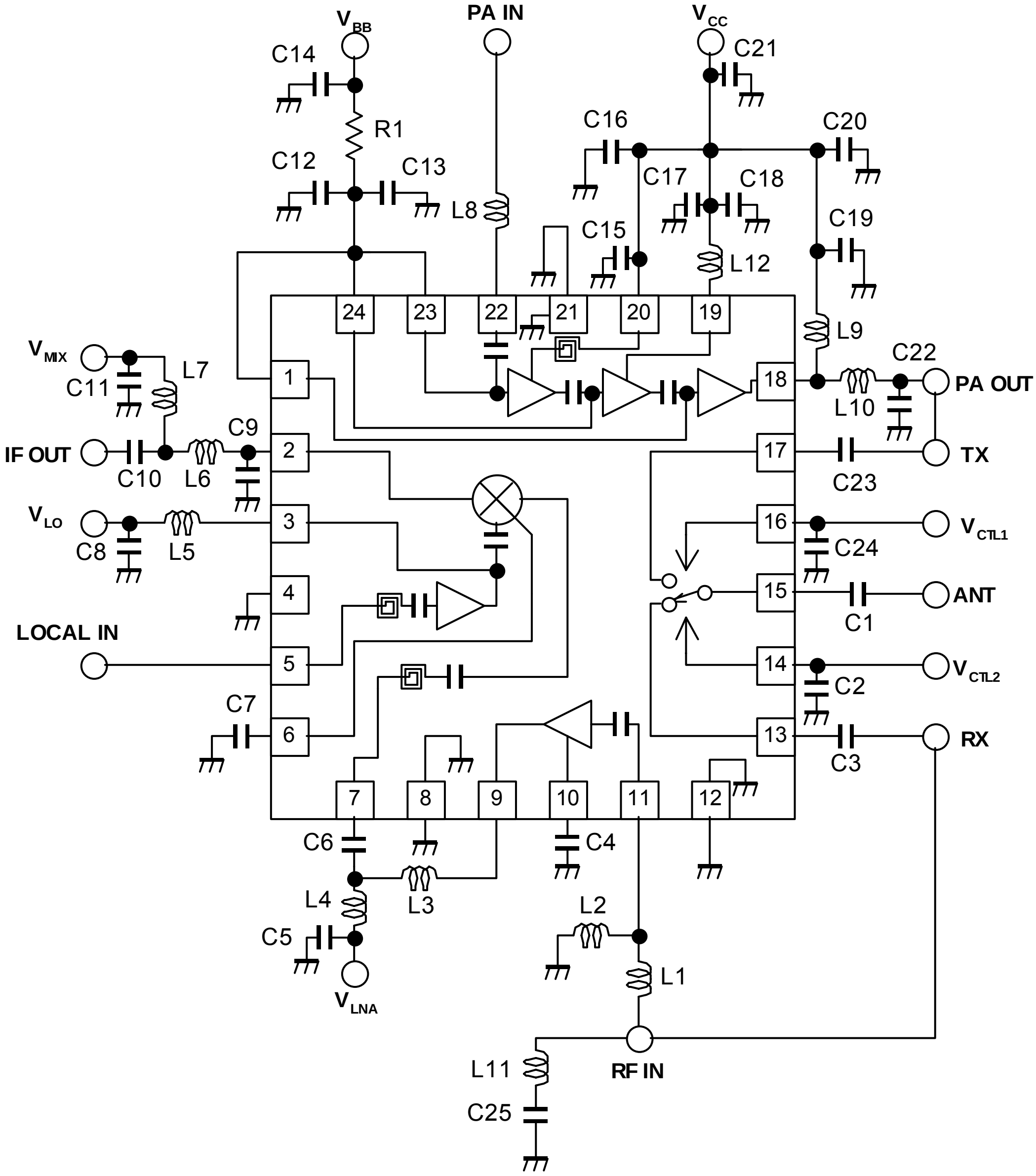
Condition
ANT 50Ω term
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

ANT to IF OUT K factor vs. Frequency
Temperature Responce



Condition
LOCAL IN 50Ω term
V_{CTL1}=0V, V_{CTL2}=2.7V
V_{LNA}=V_{MIX}=V_{LO}=2.7V

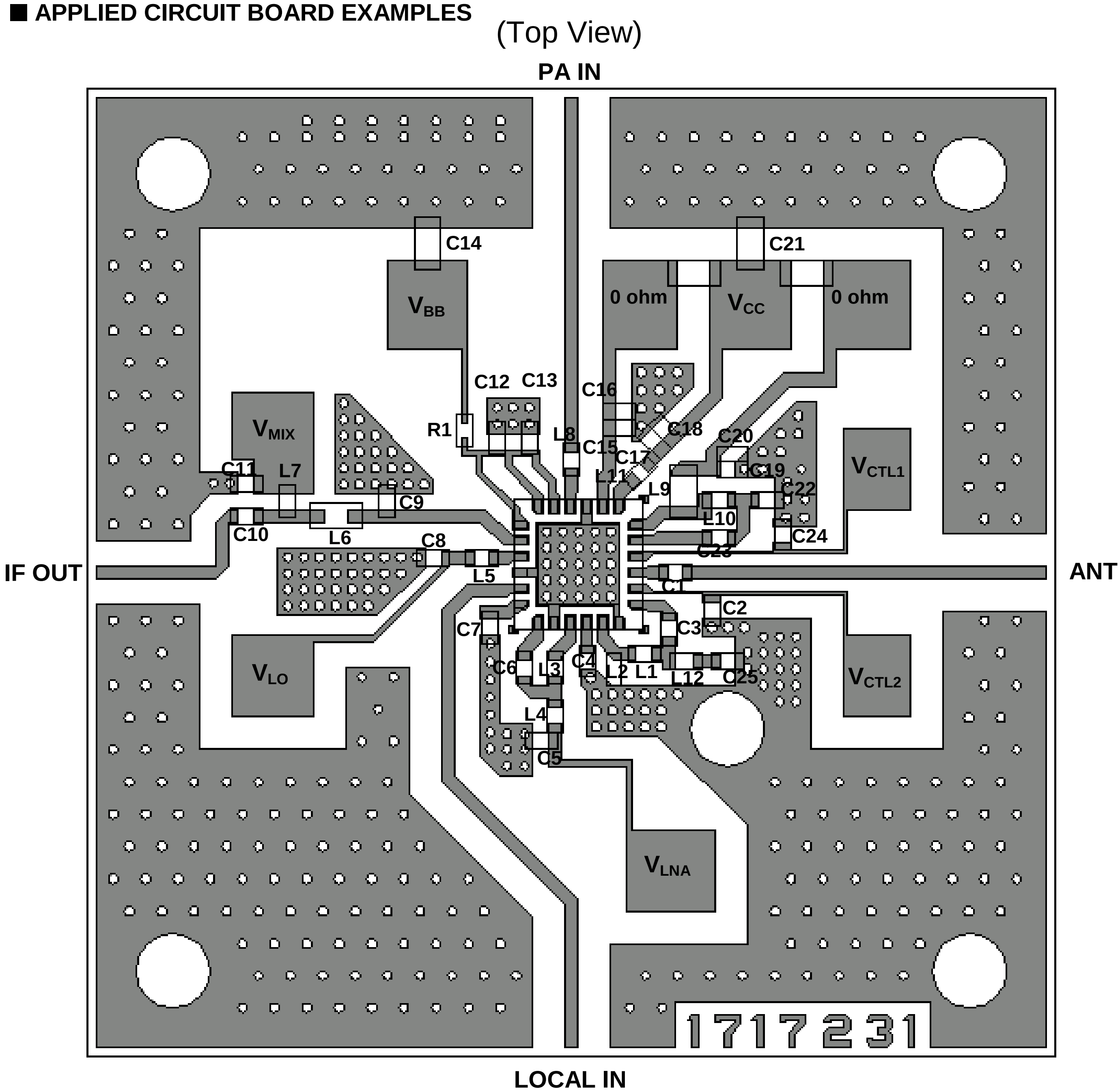
■ TEST CIRCUIT



■ PARTS LIST

PART ID	1900MHzBAND Lower LOCAL f_{LO}=1660MHz, f_{IF}=240MHz	REMARKS
L1	6.8nH	TAIYO-YUDEN (HK1005)
L2	22nH	TAIYO-YUDEN (HK1005)
L3	3.9nH	TAIYO-YUDEN (HK1005)
L4	1.5nH	TAIYO-YUDEN (HK1005)
L5	6.8nH	TAIYO-YUDEN (HK1005)
L6	39nH	TAIYO-YUDEN (HK1608)
L7	22nH	TAIYO-YUDEN (HK1005)
L8	4.7nH	TAIYO-YUDEN (HK1005)
L9	18nH	TAIYO-YUDEN (HK1608)
L10	1nH	TAIYO-YUDEN (HK1005)
L11	6.8nH	TAIYO-YUDEN (HK1005)
L12	1.2nH	TAIYO-YUDEN (HK1005)
C1	56pF	MURATA (GRP15)
C2	10pF	MURATA (GRP15)
C3	56pF	MURATA (GRP15)
C4	1000pF	MURATA (GRP15)
C5	1000pF	MURATA (GRP15)
C6	4pF	MURATA (GRP15)
C7	1000pF	MURATA (GRP15)
C8	0.01μF	MURATA (GRP15)
C9	6pF	MURATA (GRP15)
C10	1000pF	MURATA (GRP15)
C11	0.01μF	MURATA (GRP15)
C12	33pF	MURATA (GRP15)
C13	0.1μF	MURATA (GRP15)
C14	1μF	MURATA (GRM18)
C15	33pF	MURATA (GRP15)
C16	0.01μF	MURATA (GRP15)
C17	33pF	MURATA (GRP15)
C18	0.01μF	MURATA (GRP15)
C19	33pF	MURATA (GRP15)
C20	0.01μF	MURATA (GRP15)
C21	1μF	MURATA (GRM18)
C22	2pF	MURATA (GRP15)
C23	56pF	MURATA (GRP15)
C24	10pF	MURATA (GRP15)
C25	2pF	MURATA (GRP15)
R1	150Ω	1005SIZE

■ APPLIED CIRCUIT BOARD EXAMPLES



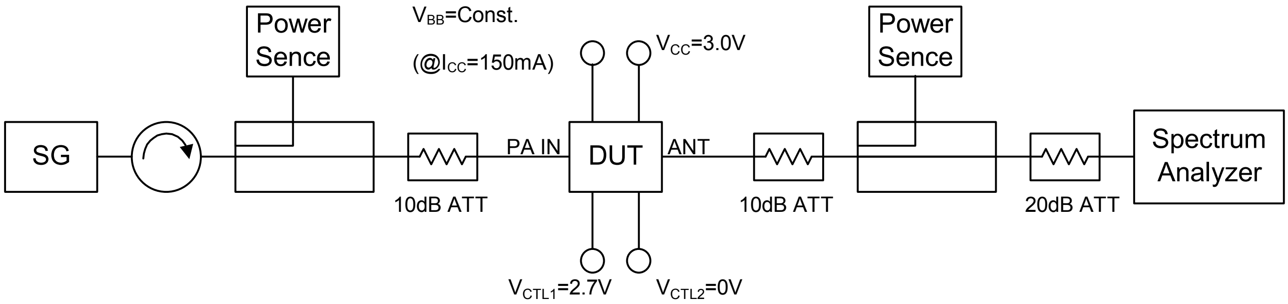
PCB (FR-4), t=0.2mm

MICROSTRIP LINE WIDTH=0.4mm(Z_O=50Ω)

PRECAUTIONS

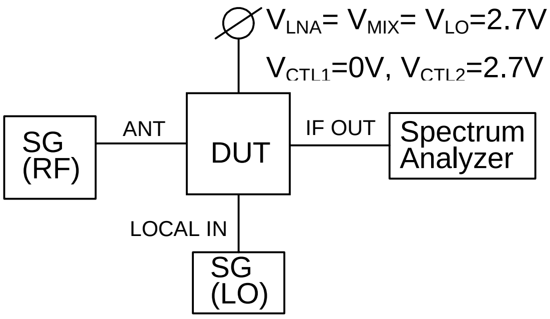
1. Please locate L1 close to LNAIN terminal (11).
2. Please locate C4 close to LNACAP terminal (10).
3. Please locate L5 close to VLO terminal (3).
4. Please locate C8 close to L5.
5. Please connect exposed GND PAD (bottom side of IC) to PCB GND using through holes as many as possible.
6. Please design the PCB structure that the dielectric thickness between the surface layer and the GND layer (directly under) is set to 0.2mm or more, about PCB of this device and external parts. However, the terminal of TAB GND of this device and the GND of external parts does not have these restrictions. Please design the GND layer pattern that can reduce a parasitic GND inductance as much as possible.

■ MEASUREMENT BLOCK DIAGRAM (TX: PA + ANT SW SECTION)

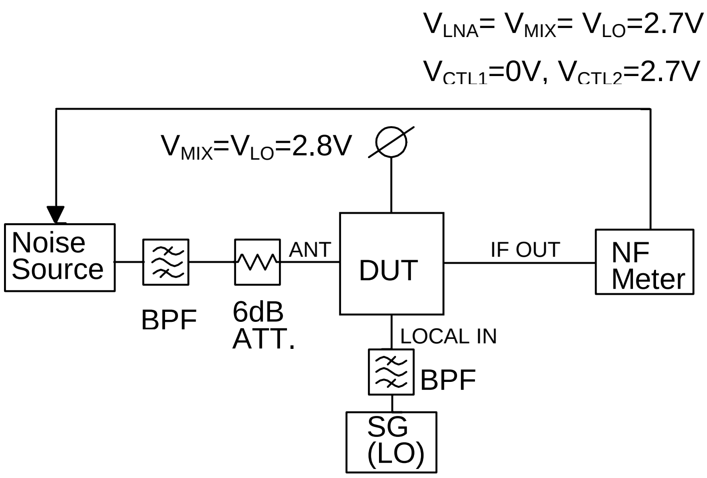


Tx mode (PA+ANT SW) Measurement Block Diagram

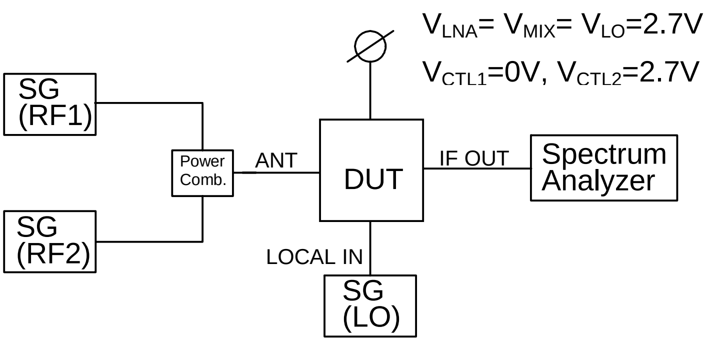
■ MEASUREMENT BLOCK DIAGRAM (RX: ANT SW + LNA + MIXER SECTION)



Conversion Gain Measurement Block Diagram

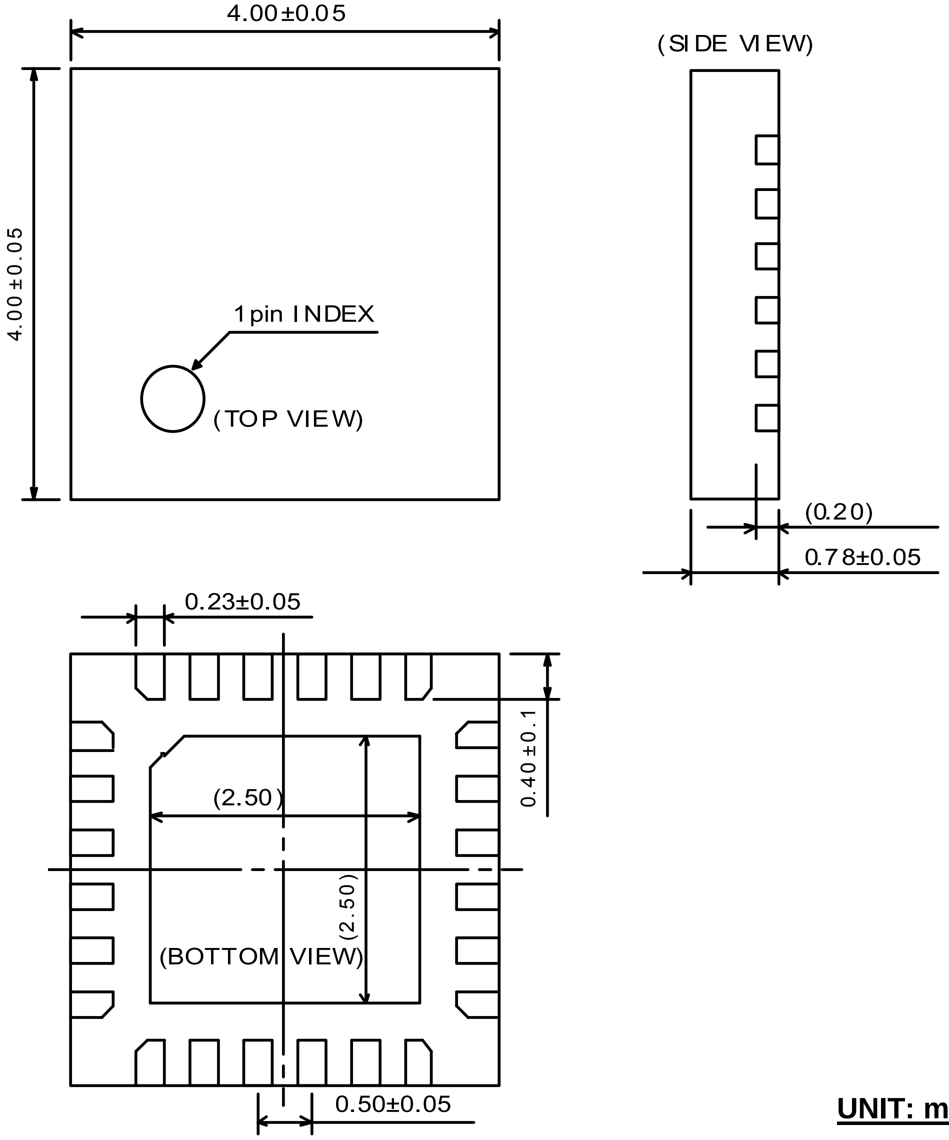


Noise Figure Measurement Block Diagram



IF and IM3 measurement Block Diagram for IIP3

■**PACKAGE OUTLINE** (QFN24-T2: 0.5pitch)



UNIT: mm

Cautions on using this product
This product contains Gallium-Arsenide (GaAs) which is a harmful material.
- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]
The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.