

Version:0.1

TECHNICAL	SPECIFICATION

MODEL NO: PD050VL1

☐Customer's Confirmation		
Customer		
Date		
Ву		
☐PVI's Confirmation		

Dep	FAE	Panel		Electronic	Mechanical	Mechanical Product	
		D	esign	Design	Design	Verification	by
SIGN	劉 豐	多个歌	课程来》	楊文朝 在建立	1 9/1 d	是我们	英老品

The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.

Page:1



TECHNICAL SPECIFICATION

CONTENTS

NO.	ITEM	PAGE
-	Cover	1
-	Contents	1
1	Application	3
2	Features	3
3	Mechanical Specifications	3
4	Mechanical Drawing of TFT-LCD module	4
5	Input Terminals	6
6	Absolute Maximum Ratings	8
7	Electrical Characteristics	8
8	Pixel Arrangement	9
9	Display Color and Gray Scale Reference	10
10	Block Diagram	11
11	Interface Timing	12
12	Power On Sequence	15
13	Optical Characteristics	15
14	Handling Cautions	19
15	Reliability Test	20
16	Packing Diagram	20
-	Revision History	21



1. Application

This product applies computer peripheral, industrial meter, image communication and multi-media. If you must use in severe reliability environment, please don't extend over PVI's reliability test conditions.

2. Features

. Support the DENB mode, Sync mode (Hsync+Vsync)

. Pixel in stripe configuration

. Slim and compact

. Display Colors: 262,144 colors

. Image Reversion : Up/Down and Left/Right

. Viewing Direction: 6 o'clock

. Amorphous silicon TFT LCD panel with LED B/L

. LVDS transmission interface

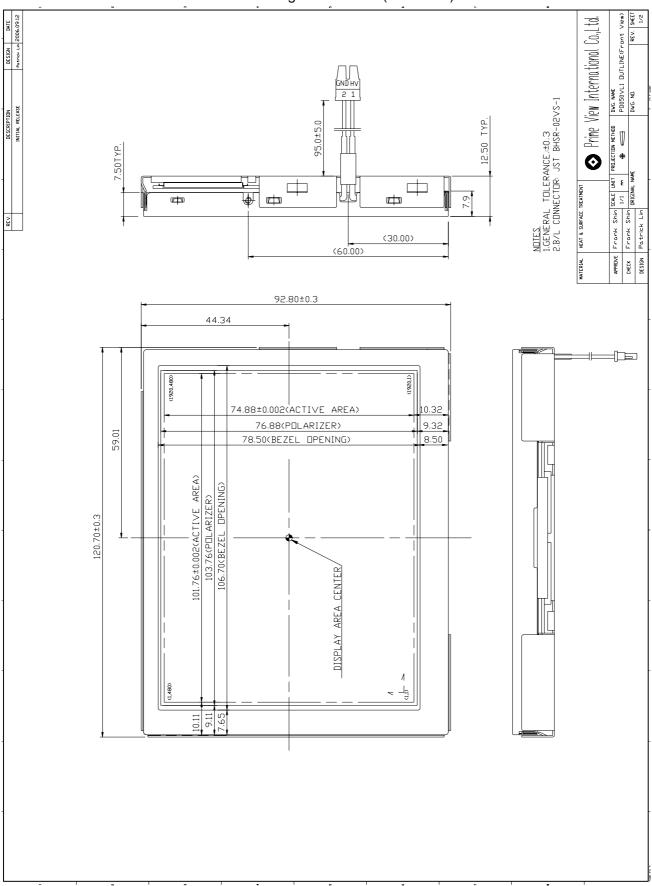
3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5(diagonal)	inch
Display Format	640×(R,G,B)×480	dot
Active Area	101.76 (H)×74.88(V)	mm
Pixel Pitch	0.159(H)×0.156(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	120.7(H)×92.8(V)×12.5(D) (Typ.)	mm
Weight	TBD	g



4.Mechanical Drawing of TFT-LCD Module

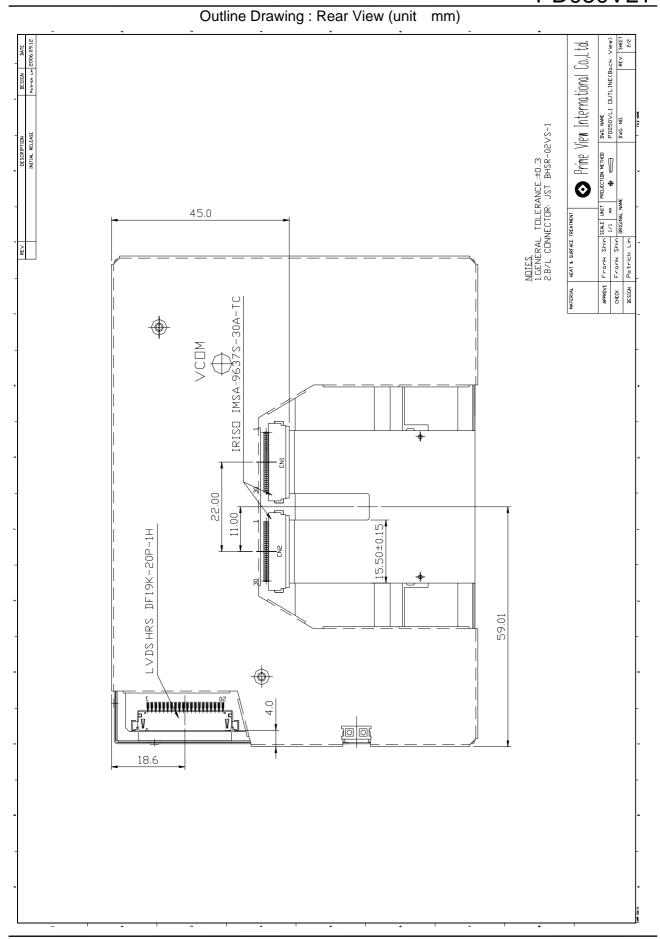
Outline Drawing : Front View (unit mm)



The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.

Page:4





The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.

Page:5



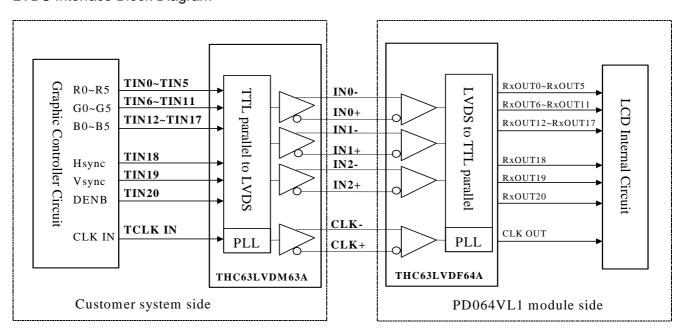
5.Input Terminals

5-1) TFT-LCD Panel Driving

Connector type: DFL19K-20P-1H(HRS)

Pin No.	Symbol	Function	Remark
1	Vcc	+3.3V Power Supply	
2	Vcc	+3.3V Power Supply	
3	GND	Ground	
4	GND	Ground	
5	INO-	LVDS receiver signal channel 0	
6	INO+	LVDS receiver signal channel 0	
7	GND	Ground	
8	IN1-	LVDS receiver signal channel 1	
9	IN1+	LVDS receiver signal channel 1	
10	GND	Ground	
11	IN2-	LVDS receiver signal channel 2	
12	IN2+	LVDS receiver signal channel 2	
13	GND	Ground	
14	CLK-	LVDS receiver signal clock	
15	CLK+	LVDS receiver signal clock	
16	GND	Ground	
17	NC	No connection	
18	NC	No connection	
19	GND	Ground	
20	GND	Ground	

LVDS Interface Block Diagram



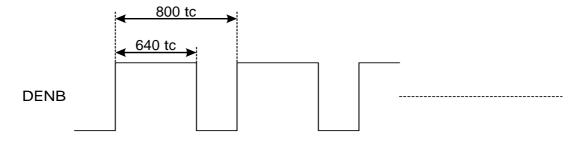


Recommended Transmitter (THC63LVDM63A Thane) to PD050VL1 interface Assignment:

THC63LVDIVI63A		Gr	aphic controller output signal	Output signal symbol	To PM070WL1 interface terminal (Symbol)
Symbol	No.	Symbol	Function		
TIN0	44	R0	Red pixel data (LSB)	`	
TIN1	45	R1	Red pixel data		
TIN2	47	R2	Red pixel data	Tout0-	— No.5 : IN0-
TIN3	48	R3	Red pixel data	>	
TIN4	1	R4	Red pixel data	Tout0+	─No.6 : IN0+
TIN5	3	R5	Red pixel data(MSB)		
TIN6	4	G	Green pixel data (LSB)	ノ	
TIN7	6	G1	Green pixel data	/	
TIN8	7	G2	Green pixel data		
TIN9	9	G3	Green pixel data	Tout1- —	—No.8 : IN1-
TIN10	10	G4	Green pixel data	>	
TIN11	12	G5	Green pixel data(MSB)	Tout1+ —	─No.9 : IN1+
TIN12	13	B0	Blue pixel data(LSB)		
TIN13	15	B1	Blue pixel data	J	
TIN14	16	B2	Blue pixel data	7	
TIN15	18	В3	Blue pixel data		
TIN16	19	B4	Blue pixel data	Tout2-	─ No.11 : IN2-
TIN17	20	B5	Blue pixel data(MSB)	>	
TIN18	22	Hsync	Horizontal Synchronous Signal	Tout2+	─ N0.12 : IN2+
TIN19	23	Vsync	Vertical Synchronous Signal		
TIN20	25	DENB	Compound Synchronization signal		
CLK in	26	CLK	Data sampling clock	TCLK out- TCLK out+	No.14 : CLK - No.15 : CLK +

DENB input signal.

If customer wanted to off the DENB mode , you must keep the DENB always High or Low.



(tc: the period of sampling clock)



6. Absolute Maximum Ratings:

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

GND=0V, Ta=25

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{CC}	-0.3	+7.0	V	
Input Signals Voltage	V_{sig}	-0.3	V _{CC} +0.3	V	Note 6-1

Note 6-1: Input signals include CLK, Hsync, Vsync, DENB, R[0:5], G[0:5] and B[0:5].

7. Electrical Characteristics

7-1) Recommended Operating Conditions:

GND = 0V, Ta = 25

ltem	Symbol	Min.	Тур.	Max.	Unit	Remark
Supply Voltage	Vcc	3.0	3.3	3.6	V	
Current Dissipation	Icc	-	TBD	-	mΑ	Note 7-1
LVDS Differential input high threshold	VTH	-	TBD	-	mV	Note7-2
LVDS Differential input low threshold	VTL	-	-	-		Note 1-2

Note 7-1: To test the current dissipation of VCC using the "color bars" testing pattern shown as below

1	2	3	4	5	6	7	8
---	---	---	---	---	---	---	---

Idd current dissipation testing pattern

- White
- 2. Yellow

- Green
 Magenta
 Red
- 7. Blue
- **Black**

Note7-2: Please refers to THC63LVDF64A specification by THINE Corporation. This LCD module conforms to LVDS standard.



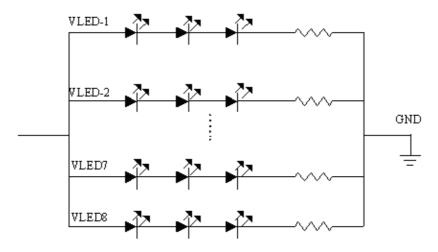
7-2) Recommended driving condition for LED backlight

GND = 0V, Ta = 25

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V_{LED}	9.0	9.9	12	V	$I_L = 20 \text{mA}$
Supply current of LED backlight	I _{LED1}	_	20	_	mA	Note 7-3
Supply current of LLD backlight	of LED backlight V_{LED} 9.0 9.9 of LED backlight I_{LED1} - 20	_	шл	Note 7-3		
Backlight Power Consumption	P_{LED}	TBD	TBD	TBD	mW	Note 7-4

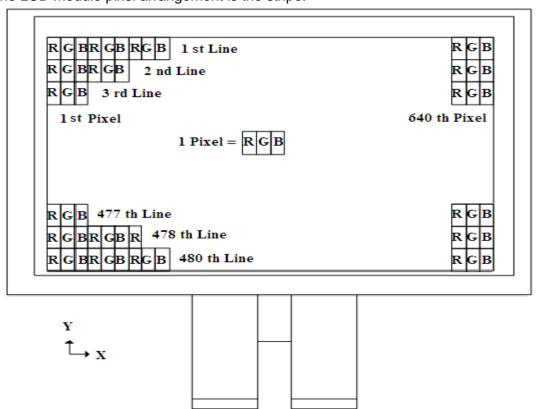
Note 7-3: LED B/L applied information, please refer to the appendix at the end.

Note 7-4:
$$P_{LED} = V_{LED1} * I_{LED1} + V_{LED2} * I_{LED2} + V_{LED7} * I_{LED7} + V_{LED8} * I_{LED8}$$



8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.



The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.

Page:9



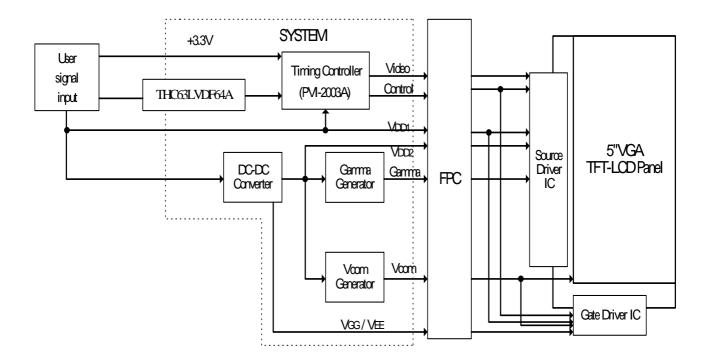
9. Display Color and Gray Scale Reference

								I	npu	t Cc	lor	Data	3						
С	olor			Re	ed			Green					Blue						
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B 5	B 4	В3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
Red																			
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
Green																			
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
Blue																			
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0		0		0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0		0			0			0			0	1	1	1	1	1	1



10. Block Diagram

10-1) TFT-module Block Diagram



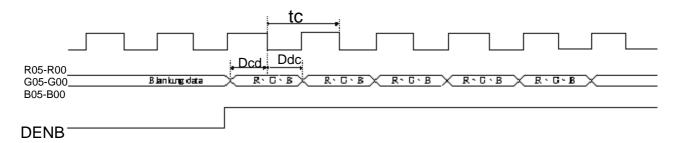


11. Interface Timing 11-1) Timing Parameters

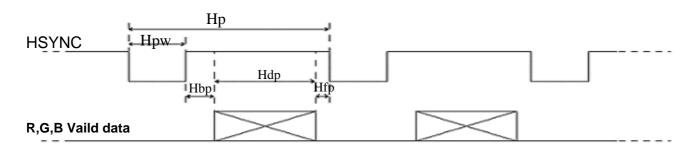
		Symbol	Min.	Тур.	Max.	Unit
Power supply		VCC	3.0	3.3	3.6	V
CLK	Fraguency	1/tc	-	25	-	MHz
	Frequency	tc	-	40	-	ns
	Period	Нр	-	32	-	us
	renou		-	800	-	tc
	Display period	Hdp	-	640	-	tc
	Pulse width	Hpw	-	96	-	tc
HSYNC	Back-porch	Hbp	-	46	-	tc
	Front-porch	Hfp	-	18	-	tc
	Hpw+Hbp		-	142	-	tc
	Hsync-CLK	Hhc	10	-	Tc-10	ns
	Vsync-Hsync	Hvh	0	0	200	tc
	Period	Vp	-	16.8	-	ms
	Fenou		-	525	-	Нр
	Display period	Vdp	-	480	-	Нр
VSYNC	Pulse width	Vpw	-	2	-	Нр
	Back-porch	Vbp	-	33	-	Нр
	Front-porch	Vfp	-	10	-	Нр
	Vpw+Vbp		-	35	-	Нр
	Horizontal scanning period	T1	-	800	-	tc
DENB	Horizontal display period	T2	-	640	-	tc
	Vertical display period	Т3	-	480	-	T1
	Frame cycling period	T4	520	525	800	T1
D G P	CLK-DATA	Dcd	10	-	-	ns
R,G,B	DATA-CLK	Ddc	8	-	-	ns



11-2) The Timing Diagram a.1 Input signal range



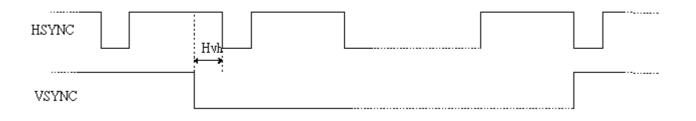
a.2 HSYNC timing



a.3 CLK, HSYNC relationship

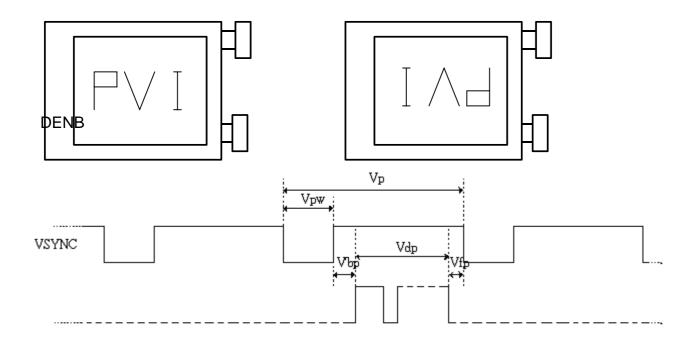


a.4 HSYNC, VSYNC relationship

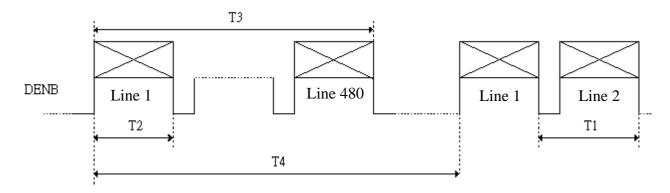




a.5 VSYNC timing



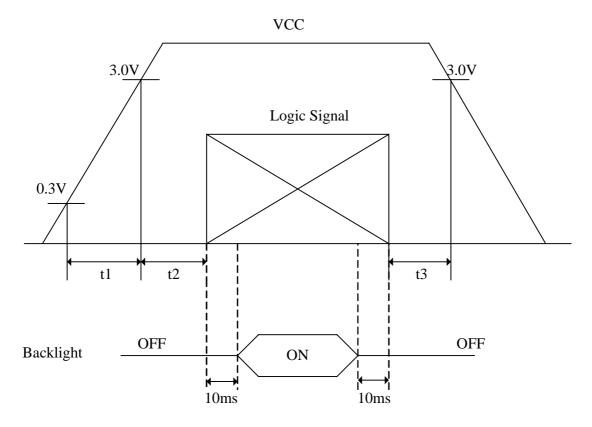
a.6 DENB timing



11-3) Control Board Dip Switch Format

TBD

12. Power On Sequence



- 1. 0 < t1 20ms
- 2. 0 < t2 50ms
- 3. 0 < t3 1s

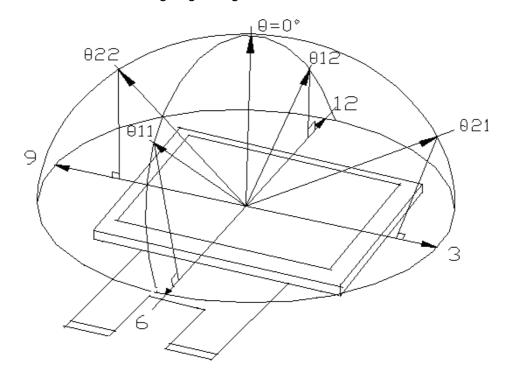
13. Optical Characteristics

13-1) Specification:

Ta=25

Para	Parameter Sym		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Hor	izontal	21, 22		55	60	-	deg	
	Vertical		12	CR > 10	35	40	-	deg	Note 13-1
			11		50	55	-	deg	
Contrast Ratio		CR	At optimized Viewing angle	-	TBD	-	-	Note 13-2	
Response time —		Rise	Tr	=0°	-	15	30	ms	Note 13-4
		Fall	Tf	=0	-	25	50	ms	
Brightness		L	=0°	450	500	-	cd/m²	Note 13-3	
Uniformity		U		70	75	-	%	Note 13-5	
Cross Talk		-	=0°	-	-	3.5	%	Note 13-6	
White Chromaticity		Х	=0°	-	TBD	-	-	Note 13-3	
		у	=0	-	TBD	-	-		
LED Life Time		+25	20,000	30,000	-	hrs			

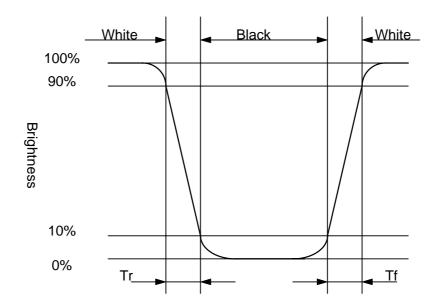
Note 13-1: The definitions of viewing angle diagrams:



Note 13-2: CR = Luminance when LCD is White
Luminance when LCD is Black
Contrast Ratio is measured in optimum common electrode voltage.

Note 13-3: Topcon BM-7 (fast) luminance meter 1°field of view is used in the testing (after 20~30 minutes operation).

Note 13-4: The definitions of response time Tr and Tr:





Note 13-5: The uniformity of LCD is defined as

U = The Minimum Brightness of the 9 testing Points
The Maximum Brightness of the 9 testing Points

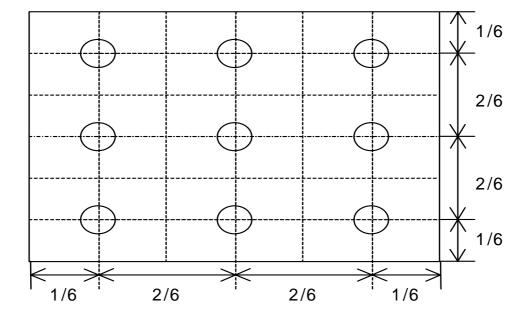
Luminance meter: BM-5A or BM-7 fast (TOPCON)

Measurement distance: 500 mm +/- 50 mm

Ambient illumination: < 1 Lux

Measuring direction: Perpendicular to the surface of module

The test pattern is white (Gray Level 63).





Note 13-6: Cross Talk (CTK) =
$$\frac{|YA-YB|}{YA} \times 100\%$$

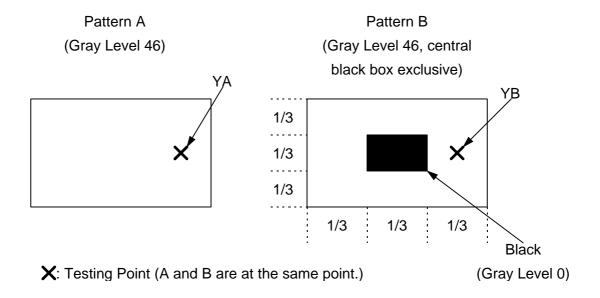
YA: Brightness of Pattern A YB: Brightness of Pattern B

Luminance meter: BM 5A or BM-7 fast (TOPCON)

Measurement distance: 500 mm +/- 50 mm

Ambient illumination: < 1 Lux

Measuring direction: Perpendicular to the surface of module





14. Handling Cautions

14-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 - 1. The noise from the backlight unit will increase.
 - 2. The output from inverter circuit will be unstable.
 - 3.In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirts. It is recommended to peel off the laminator before use and taking care of static electricity.

14-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

14-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.



15. Reliability Test

No	Test Item	Test Condition		
1	High Temperature Storage Test	Ta = +90 , 240 hrs		
2	Low Temperature Storage Test	Ta = -40 , 240 hrs		
3	High Temperature Operation Test	Ta = +80 , 240 hrs		
4	Low Temperature Operation Test	Ta = -30 , 240 hrs		
5	High Temperature & High Humidity Operation Test	Ta = +60 , 90%RH, 240 hrs		
6	Thermal Cycling Test	-30 +80 , 200 Cycles		
0	(non-operating)	30 min 30 min		
7	Vibration Test (non-operating)	Frequency: 10 ~ 55 H _z		
		Amplitude: 1 mm		
'		Sweep time: 11 mins		
		Test Period: 6 Cycles for each direction of X, Y, Z		
8	Shock Test (non-operating)	100G, 6ms		
		Direction: ±X, ±Y, ±Z		
		Cycle: 3 times		
9	Electrostatic Discharge Test (non-operating)	150pF, 330		
		Air: ±15KV; Contact: ±8KV		
		10 times/point, 9 points/panel face		

Ta: ambient temperature [Criteria]

- 1. Main LCD should normally work under the normally condition no defect of function, screen quality and appearance (including : mura ,line defect ,no image).
- 2. After the vibration and shock test, can't be find chip broken.

16. Packing Diagram TBD



Revision History

Rev.	Issued Date	Revised Contents	
0.1	Sep.12 ,2006	Preliminary	