# 3.3 V, 100 Mbps, Half- and Full-Duplex, High Speed M-LVDS Transceivers

Data Sheet **ADN4690E/ADN4692E/ADN4694E/ADN4695E**

## FEATURES

- Multipoint LVDS transceivers (low voltage differential signaling driver and receiver pairs)
- Switching rate: 100 Mbps (50 MHz)
- Supported bus loads: 30 Ω to 55 Ω
- Choice of 2 receiver types
  - Type 1 (ADN4690E/ADN4692E): hysteresis of 25 mV
  - Type 2 (ADN4694E/ADN4695E): threshold offset of 100 mV for open-circuit and bus-idle fail-safe
- Conforms to TIA/EIA-899 standard for M-LVDS
- Glitch-free power-up/power-down on M-LVDS bus
- Controlled transition times on driver output
- Common-mode range: −1 V to +3.4 V, allowing communication with 2 V of ground noise
- Driver outputs high-Z when disabled or powered off
- Enhanced ESD protection on bus pins
  - ±15 kV HBM (human body model), air discharge
  - ±8 kV HBM (human body model), contact discharge
  - ±10 kV IEC 61000-4-2, air discharge
  - ±8 kV IEC 61000-4-2, contact discharge
- Operating temperature range: −40°C to +85°C
- Available in 8-lead (ADN4690E/ADN4694E) and 14-lead (ADN4692E/ADN4695E) SOIC packages

## APPLICATIONS

- Backplane and cable multipoint data transmission
- Multipoint clock distribution
- Low power, high speed alternative to shorter RS-485 links
- Networking and wireless base station infrastructure

## FUNCTIONAL BLOCK DIAGRAMS

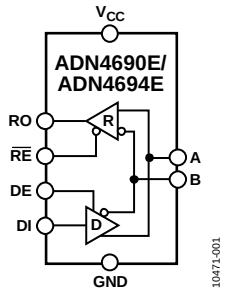



*Figure 1.*

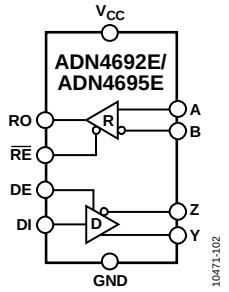



*Figure 2.*

## GENERAL DESCRIPTION

The ADN4690E/ADN4692E/ADN4694E/ADN4695E are multipoint, low voltage differential signaling (M-LVDS) transceivers (driver and receiver pairs) that can operate at up to 100 Mbps (50 MHz). Slew rate control is implemented on the driver outputs. The receivers detect the bus state with a differential input of as little as 50 mV over a common-mode voltage range of −1 V to +3.4 V. ESD protection of up to ±15 kV is implemented on the bus pins. The parts adhere to the TIA/EIA-899 standard for M-LVDS and complement TIA/EIA-644 LVDS devices with additional multipoint capabilities.

The ADN4690E/ADN4692E are Type 1 receivers with 25 mV of hysteresis, so that slow-changing signals or loss of input does not lead to output oscillations. The ADN4694E/ADN4695E are Type 2 receivers exhibiting an offset threshold, guaranteeing the output state when the bus is idle (bus-idle fail-safe) or the inputs are open (open-circuit fail-safe).

The parts are available as half-duplex in an 8-lead SOIC package (the ADN4690E/ADN4694E) or as full-duplex in a 14-lead SOIC package (the ADN4692E/ADN4695E). A selection table for the ADN469xE parts is shown in Table 1.

**Table 1. ADN469xE Selection Table**

| Part No. | Receiver | Data Rate | SOIC | Duplex |
|---|---|---|---|---|
| ADN4690E | Type 1 | 100 Mbps | 8-lead | Half |
| ADN4691E | Type 1 | 200 Mbps | 8-lead | Half |
| ADN4692E | Type 1 | 100 Mbps | 14-lead | Full |
| ADN4693E | Type 1 | 200 Mbps | 14-lead | Full |
| ADN4694E | Type 2 | 100 Mbps | 8-lead | Half |
| ADN4695E | Type 2 | 100 Mbps | 14-lead | Full |
| ADN4696E | Type 2 | 200 Mbps | 8-lead | Half |
| ADN4697E | Type 2 | 200 Mbps | 14-lead | Full |

**Rev. A**


One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

# TABLE OF CONTENTS



## REVISION HISTORY

**3/12—Rev. 0 to Rev. A**

Added ADN4694E and ADN4695E ... Universal
Change to Features Section, General Description Section, and Table 1 ... 1
Added Type 2 Receiver Parameters, Table 2 ... 3
Added Table 4, Renumbered Sequentially ... 5
Added Type 2 Receiver Parameters, Table 5 ... 5
Changes to Table 8 ... 7
Added Table 13 ... 14
Changes to Receiver Input Thresholds/Fail-Safe Section and Figure 35 ... 15
Changes to Figure 36 and Figure 37 and Their Captions ... 16
Changes to Ordering Guide ... 18

**1/12—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V; $R_L$ = 50 Ω; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.[1]

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DRIVER | | | | | | |
| Differential Outputs | | | | | | |
| Differential Output Voltage Magnitude | $\|V_{OD}\|$ | 480 | | 650 | mV | See Figure 18 |
| $\Delta\|V_{OD}\|$ for Complementary Output States | $\Delta\|V_{OD}\|$ | −50 | | +50 | mV | See Figure 18 |
| Common-Mode Output Voltage (Steady State) | $V_{OC(SS)}$ | 0.8 | | 1.2 | V | See Figure 19, Figure 22 |
| $\Delta V_{OC(SS)}$ for Complementary Output States | $\Delta V_{OC(SS)}$ | −50 | | +50 | mV | See Figure 19, Figure 22 |
| Peak-to-Peak $V_{OC}$ | $V_{OC(PP)}$ | | | 150 | mV | See Figure 19, Figure 22 |
| Maximum Steady-State Open-Circuit Output Voltage | $V_{A(O)}$, $V_{B(O)}$, $V_{Y(O)}$, or $V_{Z(O)}$ | 0 | | 2.4 | V | See Figure 20 |
| Voltage Overshoot | | | | | | |
| Low to High | $V_{PH}$ | | | $1.2V_{SS}$ | V | See Figure 23, Figure 26 |
| High to Low | $V_{PL}$ | $-0.2V_{SS}$ | | | V | See Figure 23, Figure 26 |
| Output Current | | | | | | |
| Short Circuit | $\|I_{OS}\|$ | | | 24 | mA | See Figure 21 |
| High Impedance State, Driver Only | $I_{OZ}$ | −15 | | +10 | µA | −1.4 V ≤ ($V_Y$ or $V_Z$) ≤ 3.8 V, other output = 1.2 V |
| Power Off | $I_{O(OFF)}$ | −10 | | +10 | µA | −1.4 V ≤ ($V_Y$ or $V_Z$) ≤ 3.8 V, other output = 1.2 V, 0 V ≤ $V_{CC}$ ≤ 1.5 V |
| Output Capacitance | $C_Y$ or $C_Z$ | | 3 | | pF | $V_I$ = 0.4 sin(30$e^6$πt) V + 0.5 V,[2] other output = 1.2 V, DE = 0 V |
| Differential Output Capacitance | $C_{YZ}$ | | | 2.5 | pF | $V_{AB}$ = 0.4 sin(30$e^6$πt) V,[2] DE = 0 V |
| Output Capacitance Balance ($C_Y/C_Z$) | $C_{Y/Z}$ | 0.99 | | 1.01 | | |
| Logic Inputs (DI, DE) | | | | | | |
| Input High Voltage | $V_{IH}$ | 2 | | $V_{CC}$ | V | |
| Input Low Voltage | $V_{IL}$ | GND | | 0.8 | V | |
| Input High Current | $I_{IH}$ | 0 | | 10 | µA | $V_{IH}$ = 2 V to $V_{CC}$ |
| Input Low Current | $I_{IL}$ | 0 | | 10 | µA | $V_{IL}$ = GND to 0.8 V |
| RECEIVER | | | | | | |
| Differential Inputs | | | | | | |
| Differential Input Threshold Voltage | | | | | | |
| Type 1 Receiver (ADN4690E, ADN4692E) | $V_{TH}$ | −50 | | +50 | mV | See Table 3, Figure 35 |
| Type 2 Receiver (ADN4694E, ADN4695E) | $V_{TH}$ | 50 | | 150 | mV | See Table 4, Figure 35 |
| Input Hysteresis | | | | | | |
| Type 1 Receiver (ADN4690E, ADN4692E) | $V_{HYS}$ | | 25 | | mV | |
| Type 2 Receiver (ADN4694E, ADN4695E) | $V_{HYS}$ | | 0 | | mV | |
| Differential Input Voltage Magnitude | $\|V_{ID}\|$ | 0.05 | | $V_{CC}$ | V | |
| Input Capacitance | $C_A$ or $C_B$ | | 3 | | pF | $V_I$ = 0.4 sin(30$e^6$πt) V + 0.5 V,[2] other input = 1.2 V |
| Differential Input Capacitance | $C_{AB}$ | | | 2.5 | pF | $V_{AB}$ = 0.4 sin(30$e^6$πt) V[2] |
| Input Capacitance Balance ($C_A/C_B$) | $C_{A/B}$ | 0.99 | | 1.01 | | |
| Logic Output RO | | | | | | |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −8 mA |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| High Impedance Output Current | $I_{OZ}$ | −10 | | +15 | µA | $V_O$ = 0 V or 3.6 V |
| Logic Input $\overline{RE}$ | | | | | | |
| Input High Voltage | $V_{IH}$ | 2 | | $V_{CC}$ | V | |
| Input Low Voltage | $V_{IL}$ | GND | | 0.8 | V | |
| Input High Current | $I_{IH}$ | −10 | | 0 | µA | $V_{IH}$ = 2 V to $V_{CC}$ |
| Input Low Current | $I_{IL}$ | −10 | | 0 | µA | $V_{IL}$ = GND to 0.8 V |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| BUS INPUT/OUTPUT | | | | | | |
| Input Current | | | | | | |
| A (Receiver or Transceiver with Driver Disabled) | $I_A$ | 0 | | 32 | μA | $V_B$ = 1.2 V, $V_A$ = 3.8 V |
| | | −20 | | +20 | μA | $V_B$ = 1.2 V, $V_A$ = 0 V or 2.4 V |
| | | −32 | | 0 | μA | $V_B$ = 1.2 V, $V_A$ = −1.4 V |
| B (Receiver or Transceiver with Driver Disabled) | $I_B$ | 0 | | 32 | μA | $V_A$ = 1.2 V, $V_B$ = 3.8 V |
| | | −20 | | +20 | μA | $V_A$ = 1.2 V, $V_B$ = 0 V or 2.4 V |
| | | −32 | | 0 | μA | $V_A$ = 1.2 V, $V_B$ = −1.4 V |
| Differential (Receiver or Transceiver with Driver Disabled) | $I_{AB}$ | −4 | | +4 | μA | $V_A = V_B$, 1.4 ≤ $V_A$ ≤ 3.8 V |
| Power-Off Input Current | | | | | | 0 V ≤ $V_{CC}$ ≤ 1.5 V |
| A (Receiver or Transceiver) | $I_{A(OFF)}$ | 0 | | 32 | μA | $V_B$ = 1.2 V, $V_A$ = 3.8 V |
| | | −20 | | +20 | μA | $V_B$ = 1.2 V, $V_A$ = 0 V or 2.4 V |
| | | −32 | | 0 | μA | $V_B$ = 1.2 V, $V_A$ = −1.4 V |
| B (Receiver or Transceiver) | $I_{B(OFF)}$ | 0 | | 32 | μA | $V_A$ = 1.2 V, $V_B$ = 3.8 V |
| | | −20 | | +20 | μA | $V_A$ = 1.2 V, $V_B$ = 0 V or 2.4 V |
| | | −32 | | 0 | μA | $V_A$ = 1.2 V, $V_B$ = −1.4 V |
| Differential (Receiver or Transceiver) | $I_{AB(OFF)}$ | −4 | | +4 | μA | $V_A = V_B$, 1.4 V ≤ $V_A$ ≤ 3.8 V |
| Input Capacitance (Transceiver with Driver Disabled) | $C_A$ or $C_B$ | | 5 | | pF | $V_I$ = 0.4 sin(30e$^6$πt) V + 0.5 V,[2] other input = 1.2 V, DE = 0 V |
| Differential Input Capacitance (Transceiver with Driver Disabled) | $C_{AB}$ | | | 3 | pF | $V_{AB}$ = 0.4 sin(30e$^6$πt) V,[2] DE = 0 V |
| Input Capacitance Balance ($C_A$/$C_B$) (Transceiver with Driver Disabled) | $C_{A/B}$ | 0.99 | | 1.01 | | DE = 0 V |
| POWER SUPPLY | | | | | | |
| Supply Current | $I_{CC}$ | | | | | |
| Only Driver Enabled | | | 13 | 22 | mA | DE, $\overline{RE}$ = $V_{CC}$, $R_L$ = 50 Ω |
| Both Driver and Receiver Disabled | | | 1 | 4 | mA | DE = 0 V, $\overline{RE}$ = $V_{CC}$, $R_L$ = no load |
| Both Driver and Receiver Enabled | | | 16 | 24 | mA | DE = $V_{CC}$, $\overline{RE}$ = 0 V, $R_L$ = 50 Ω |
| Only Receiver Enabled | | | 4 | 13 | mA | DE, $\overline{RE}$ = 0 V, $R_L$ = 50 Ω |
| Total Power Dissipation | $P_D$ | | | 94 | mW | $R_L$ = 50 Ω, input (DI) = 50 MHz, 50% duty cycle square wave; DE = $V_{CC}$; $\overline{RE}$ = 0 V; $T_A$ = 85°C |

[1] All typical values are given for $V_{CC}$ = 3.3 V and $T_A$ = 25°C.
[2] HP4194A impedance analyzer (or equivalent).

## RECEIVER INPUT THRESHOLD TEST VOLTAGES

$\overline{RE}$ = 0 V, H = high, L = low.

**Table 3. Test Voltages for Type 1 Receiver**

| Applied Voltages | | Input Voltage, Differential | Input Voltage, Common Mode | Receiver Output |
|---|---|---|---|---|
| $V_A$ (V) | $V_B$ (V) | $V_{ID}$ (V) | $V_{IC}$ (V) | RO |
| 2.4 | 0 | 2.4 | 1.2 | H |
| 0 | 2.4 | −2.4 | 1.2 | L |
| 3.425 | 3.375 | 0.05 | 3.4 | H |
| 3.375 | 3.425 | −0.05 | 3.4 | L |
| −0.975 | −1.025 | 0.05 | −1 | H |
| −1.025 | −0.975 | −0.05 | −1 | L |

**Table 4. Test Voltages for Type 2 Receiver**

| Applied Voltages | | Input Voltage, Differential | Input Voltage, Common Mode | Receiver Output |
|---|---|---|---|---|
| $V_A$ (V) | $V_B$ (V) | $V_{ID}$ (V) | $V_{IC}$ (V) | RO |
| 2.4 | 0 | 2.4 | 1.2 | H |
| 0 | 2.4 | −2.4 | 1.2 | L |
| 3.475 | 3.325 | 0.15 | 3.4 | H |
| 3.425 | 3.375 | 0.05 | 3.4 | L |
| −0.925 | −1.075 | 0.15 | −1 | H |
| −0.975 | −1.025 | 0.05 | −1 | L |

## TIMING SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V; $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.[1]

**Table 5.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DRIVER | | | | | | |
| Maximum Data Rate | | 100 | | | Mbps | |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | 2 | 2.5 | 3.5 | ns | See Figure 23, Figure 26 |
| Differential Output Rise/Fall Time | $t_R$, $t_F$ | 2 | 2.6 | 3.2 | ns | See Figure 23, Figure 26 |
| Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$ | $t_{SK}$ | | 30 | 150 | ps | See Figure 23, Figure 26 |
| Part-to-Part Skew | $t_{SK(PP)}$ | | | 0.9 | ns | See Figure 23, Figure 26 |
| Period Jitter, rms (One Standard Deviation)[2] | $t_{J(PER)}$ | | 2 | 3 | ps | 50 MHz clock input[3] (see Figure 25) |
| Peak-to-Peak Jitter[2, 4] | $t_{J(PP)}$ | | | 150 | ps | 100 Mbps $2^{15}$ − 1 PRBS input[5] (see Figure 28) |
| Disable Time from High Level | $t_{PHZ}$ | | 4 | 7 | ns | See Figure 24, Figure 27 |
| Disable Time from Low Level | $t_{PLZ}$ | | 4 | 7 | ns | See Figure 24, Figure 27 |
| Enable Time to High Level | $t_{PZH}$ | | 4 | 7 | ns | See Figure 24, Figure 27 |
| Enable Time to Low Level | $t_{PZL}$ | | 4 | 7 | ns | See Figure 24, Figure 27 |
| RECEIVER | | | | | | |
| Propagation Delay | $t_{RPLH}$, $t_{RPHL}$ | 2 | | 6 | ns | $C_L$ = 15 pF (see Figure 29, Figure 32) |
| Rise/Fall Time | $t_R$, $t_F$ | 1 | | 2.3 | ns | $C_L$ = 15 pF (see Figure 29, Figure 32) |
| Pulse Skew $\lvert t_{RPHL} - t_{RPLH} \rvert$ | | | | | | $C_L$ = 15 pF (see Figure 29, Figure 32) |
| Type 1 Receiver (ADN4690E, ADN4692E) | $t_{SK}$ | | 100 | 300 | ps | |
| Type 2 Receiver (ADN4694E, ADN4695E) | $t_{SK}$ | | 300 | 500 | ps | |
| Part-to-Part Skew[6] | $t_{SK(PP)}$ | | | 1 | ns | $C_L$ = 15 pF (see Figure 29, Figure 32) |
| Period Jitter, rms (One Standard Deviation)[2] | $t_{J(PER)}$ | | 4 | 7 | ps | 50 MHz clock input[3] (see Figure 31) |
| Peak-to-Peak Jitter[2, 4] | | | | | | 100 Mbps $2^{15}$ − 1 PRBS input[5] (see Figure 34) |
| Type 1 Receiver (ADN4690E, ADN4692E) | $t_{J(PP)}$ | | 200 | 700 | ps | |
| Type 2 Receiver (ADN4694E, ADN4695E) | $t_{J(PP)}$ | | 225 | 800 | ps | |
| Disable Time from High Level | $t_{RPHZ}$ | | 6 | 10 | ns | See Figure 30, Figure 33 |
| Disable Time from Low Level | $t_{RPLZ}$ | | 6 | 10 | ns | See Figure 30, Figure 33 |
| Enable Time to High Level | $t_{RPZH}$ | | 10 | 15 | ns | See Figure 30, Figure 33 |
| Enable Time to Low Level | $t_{RPZL}$ | | 10 | 15 | ns | See Figure 30, Figure 33 |

[1] All typical values are given for $V_{CC}$ = 3.3 V and $T_A$ = 25°C.
[2] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.
[3] $t_R = t_F$ = 0.5 ns (10% to 90%), measured over 30,000 samples.
[4] Peak-to-peak jitter specifications include jitter due to pulse skew ($t_{SK}$).
[5] $t_R = t_F$ = 0.5 ns (10% to 90%), measured over 100,000 samples.
[6] HP4194A impedance analyzer or equivalent.

# ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 6.**

| Parameter | Rating |
|---|---|
| $V_{CC}$ | −0.5 V to +4 V |
| Digital Input Voltage (DE, $\overline{RE}$, DI) | −0.5 V to +4 V |
| Receiver Input (A, B) Voltage | |
| Half-Duplex (ADN4690E, ADN4694E) | −1.8 V to +4 V |
| Full-Duplex (ADN4692E, ADN4695E) | −4 V to +6 V |
| Receiver Output Voltage (RO) | −0.3 V to +4 V |
| Driver Output (A, B, Y, Z) Voltage | −1.8 V to +4 V |
| ESD Rating (A, B, Y, Z Pins) | |
| HBM (Human Body Model) | |
| Air Discharge | ±15 kV |
| Contact Discharge | ±8 kV |
| IEC 61000-4-2, Air Discharge | ±10 kV |
| IEC 61000-4-2, Contact Discharge | ±8 kV |
| ESD Rating (Other Pins, HBM) | ±4 kV |
| ESD Rating (All Pins) | |
| FICDM | ±1.25 kV |
| Machine Model | ±400 V |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 7. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 8-Lead SOIC | 121 | °C/W |
| 14-Lead SOIC | 86 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

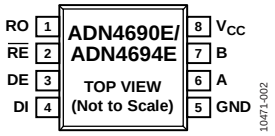



*Figure 3. ADN4690E/ADN4694E Pin Configuration*

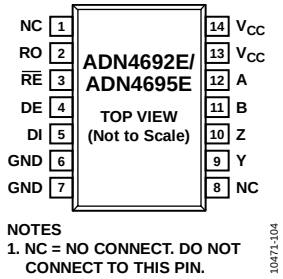



*Figure 4. ADN4692E/ADN4695E Pin Configuration*

**Table 8. Pin Function Descriptions**

| ADN4690E/ ADN4694E Pin No. | ADN4692E/ ADN4695E Pin No. | Mnemonic | Description |
|---|---|---|---|
| 1 | 2 | RO | Receiver Output. Type 1 receiver (ADN4690E/ADN4692E), when enabled:<br>If A − B ≥ 50 mV, then RO = logic high. If A − B ≤ −50 mV, then RO = logic low.<br>Type 2 receiver (ADN4694E/ADN4695E), when enabled:<br>If A − B ≥ 150 mV, then RO = logic high. If A − B ≤ 50 mV, then RO = logic low.<br>Receiver output is undefined outside these conditions. |
| 2 | 3 | $\overline{RE}$ | Receiver Output Enable. A logic low on this pin enables the receiver output, RO.<br>A logic high on this pin places RO in a high impedance state. |
| 3 | 4 | DE | Driver Output Enable. A logic high on this pin enables the driver differential outputs.<br>A logic low on this pin places the driver differential outputs in a high impedance state. |
| 4 | 5 | DI | Driver Input. Half-duplex (ADN4690E/ADN4694E), when enabled:<br>A logic low on DI forces A low and B high, whereas a logic high on DI forces A high and B low.<br>Full-duplex (ADN4692E/ADN4695E), when enabled:<br>A logic low on DI forces Y low and Z high, whereas a logic high on DI forces Y high and Z low. |
| 5 | 6, 7 | GND | Ground. |
| N/A | 9 | Y | Noninverting Driver Output Y. |
| N/A | 10 | Z | Inverting Driver Output Z. |
| 6 | N/A | A | Noninverting Receiver Input A and Noninverting Driver Output A. |
| N/A | 12 | A | Noninverting Receiver Input A. |
| 7 | N/A | B | Inverting Receiver Input B and Inverting Driver Output B. |
| N/A | 11 | B | Inverting Receiver Input B. |
| 8 | 13, 14 | $V_{CC}$ | Power Supply (3.3 V ± 0.3 V). |
| N/A | 1, 8 | NC | No Connect. Do not connect to these pins. |

# TYPICAL PERFORMANCE CHARACTERISTICS

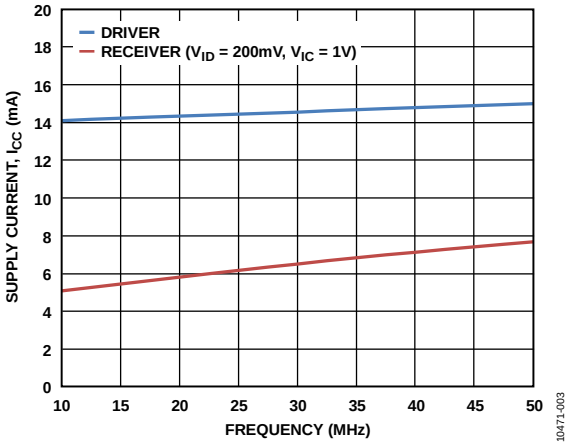



*Figure 5. Power Supply Current vs. Frequency ($V_{CC}$ = 3.3 V, $T_A$ = 25°C)*

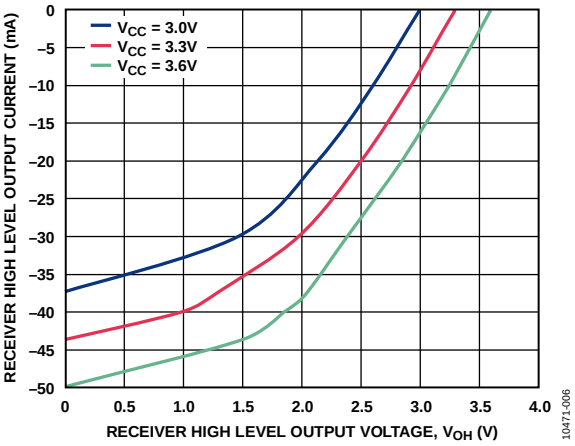



*Figure 8. Receiver Output Current vs. Output Voltage (Output High) ($T_A$ = 25°C)*

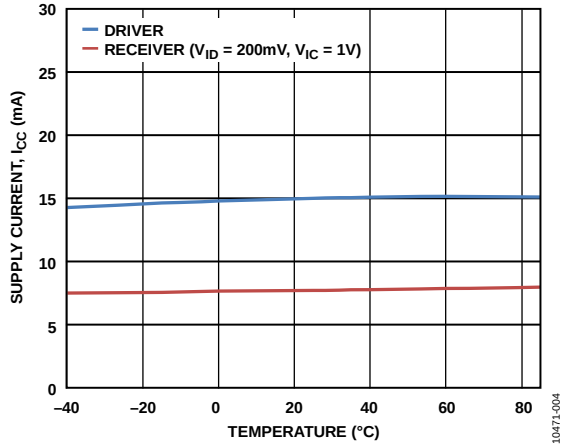



*Figure 6. Power Supply Current vs. Temperature (Data Rate = 100 Mbps, $V_{CC}$ = 3.3 V)*

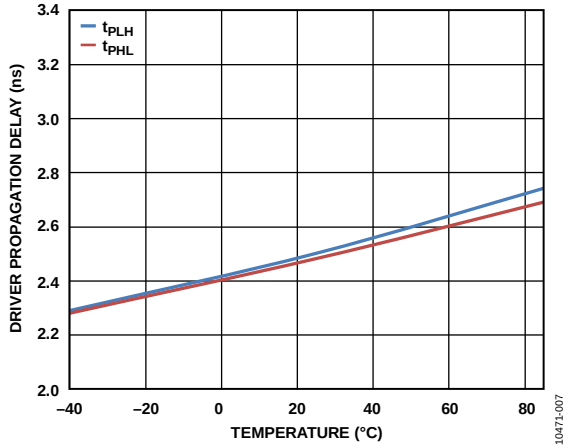



*Figure 9. Driver Propagation Delay vs. Temperature (Data Rate = 2 Mbps, $V_{CC}$ = 3.3 V, $R_L$ = 50 Ω)*

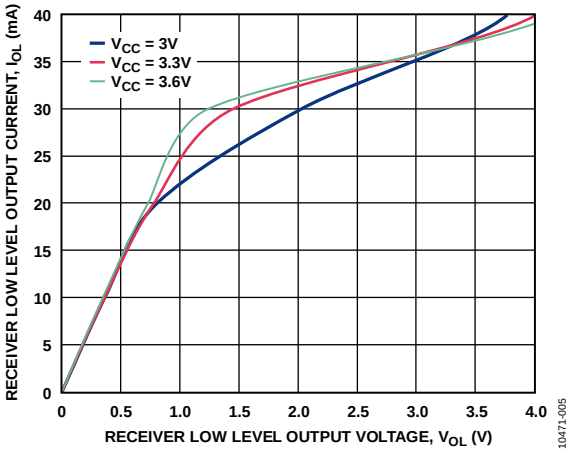



*Figure 7. Receiver Output Current vs. Output Voltage (Output Low) ($T_A$ = 25°C)*

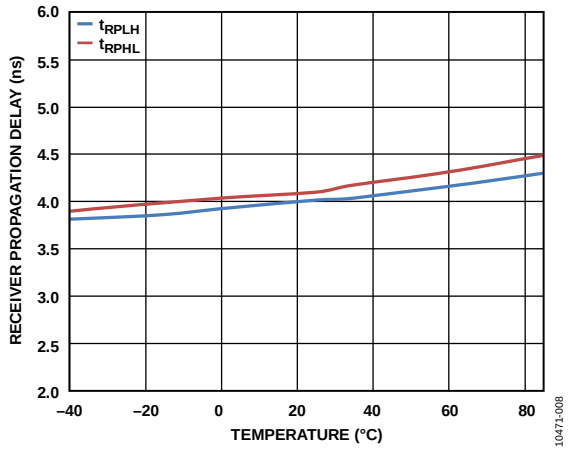



*Figure 10. Receiver Propagation Delay vs. Temperature (Data Rate = 2 Mbps, $V_{CC}$ = 3.3 V, $V_{ID}$ = 200 mV, $V_{IC}$ = 1 V, $C_L$ = 15 pF)*

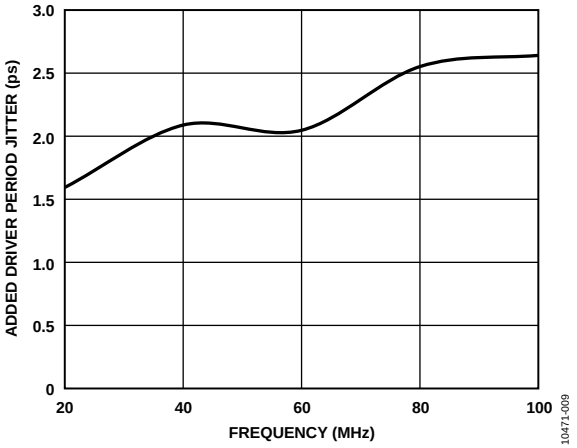



*Figure 11. Driver Jitter (Period) vs. Frequency ($V_{CC}$ = 3.3 V, $T_A$ = 25°C, Clock Input)*

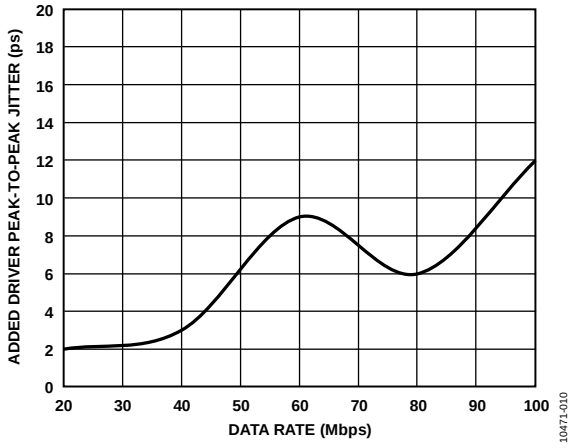



*Figure 12. Driver Jitter (Peak-to-Peak) vs. Data Rate ($V_{CC}$ = 3.3 V, $T_A$ = 25°C, PRBS $2^{15}$ − 1 NRZ Input)*

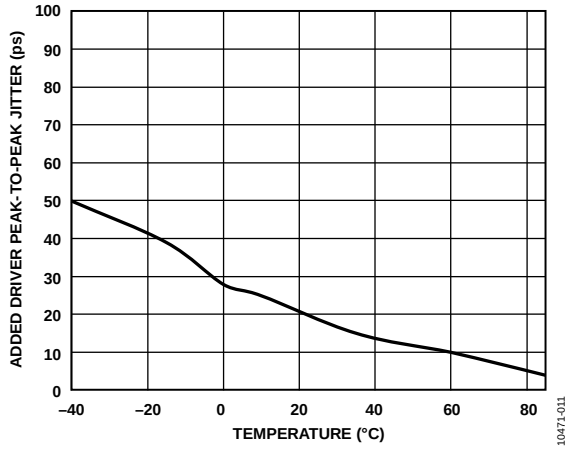



*Figure 13. Driver Jitter (Peak-to-Peak) vs. Temperature (Data Rate = 100 Mbps, $V_{CC}$ = 3.3 V, $T_A$ = 25°C, PRBS $2^{15}$ − 1 NRZ Input)*

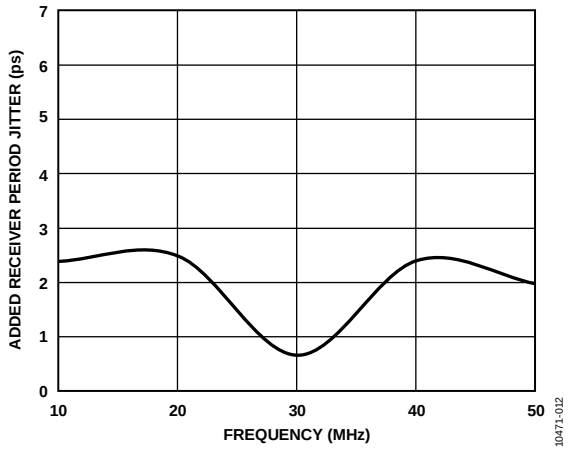



*Figure 14. Receiver Jitter (Period) vs. Frequency ($V_{CC}$ = 3.3 V, $T_A$ = 25°C, $V_{IC}$ = 1 V, Clock Input)*

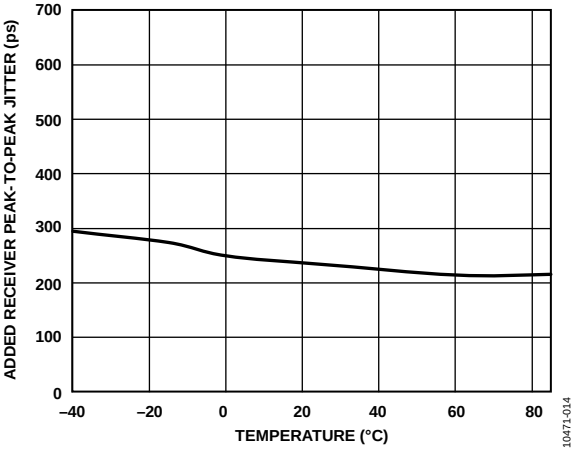



*Figure 15. Receiver Jitter (Peak-to-Peak) vs. Temperature ($V_{CC}$ = 3.3 V, $V_{IC}$ = 1 V, PRBS $2^{15}$ − 1 NRZ Input)*

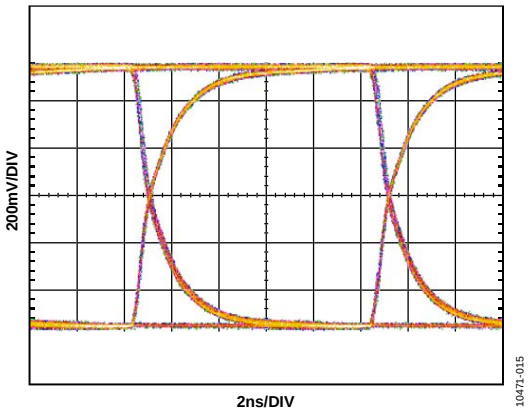



*Figure 16. ADN4690E Driver Output Eye Pattern (Data Rate = 100 Mbps, PRBS $2^{15} - 1$ Input, $R_L = 50\ \Omega$)*

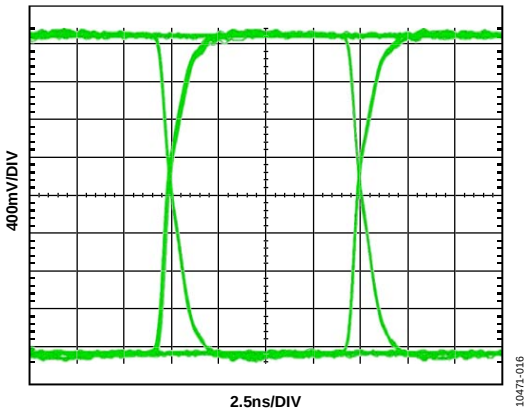
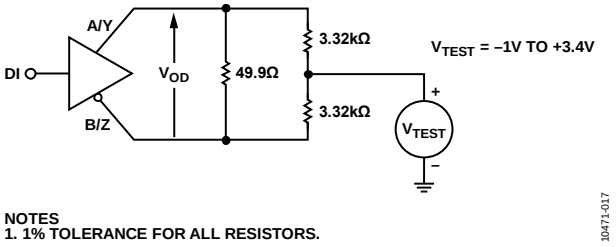



*Figure 17. ADN4690E Receiver Output Eye Pattern (Data Rate = 100 Mbps, PRBS $2^{15} - 1$, $C_L = 15$ pF)*

# TEST CIRCUITS AND SWITCHING CHARACTERISTICS

## DRIVER VOLTAGE AND CURRENT MEASUREMENTS




NOTES
1. 1% TOLERANCE FOR ALL RESISTORS.

*Figure 18. Driver Voltage Measurement over Common-Mode Range*

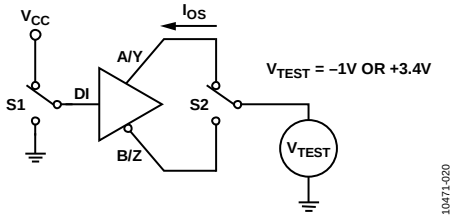
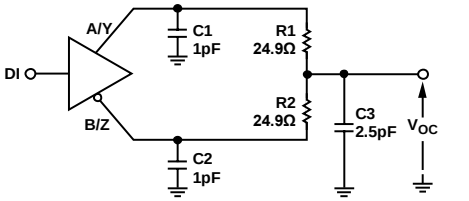
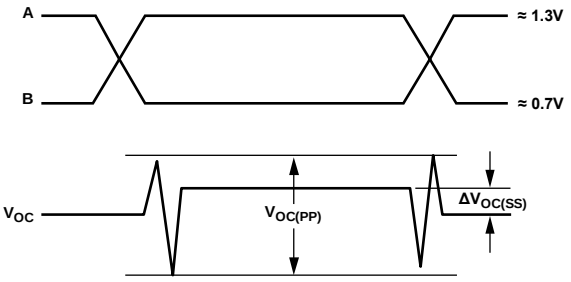



*Figure 21. Driver Short Circuit*




NOTES
1. C1, C2, AND C3 ARE 20% AND INCLUDE PROBE/STRAY CAPACITANCE < 2cm FROM DUT.
2. R1 AND R2 ARE 1%, METAL FILM, SURFACE MOUNT, <2cm FROM DUT.

*Figure 19. Driver Common-Mode Output Voltage Measurement*




NOTES
1. INPUT PULSE GENERATOR: 1MHz; 50% ± 5% DUTY CYCLE; $t_R$, $t_F$ ≤ 1ns.
2. $V_{OC(PP)}$ MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 1GHz.

*Figure 22. Driver Common-Mode Output Voltage (Steady State)*

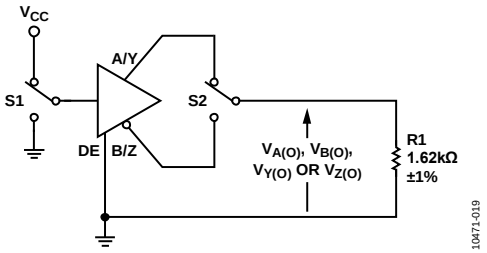
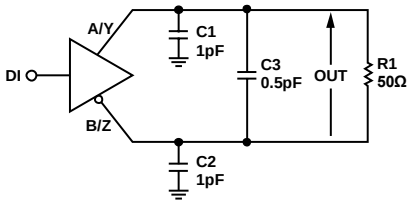



*Figure 20. Maximum Steady-State Output Voltage Measurement*

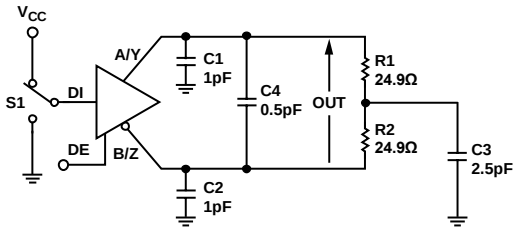
## DRIVER TIMING MEASUREMENTS




NOTES
1. C1, C2, AND C3 ARE 20% AND INCLUDE PROBE/STRAY CAPACITANCE < 2cm FROM DUT.
2. R1 IS 1%, METAL FILM, SURFACE MOUNT, <2cm FROM DUT.

10471-022

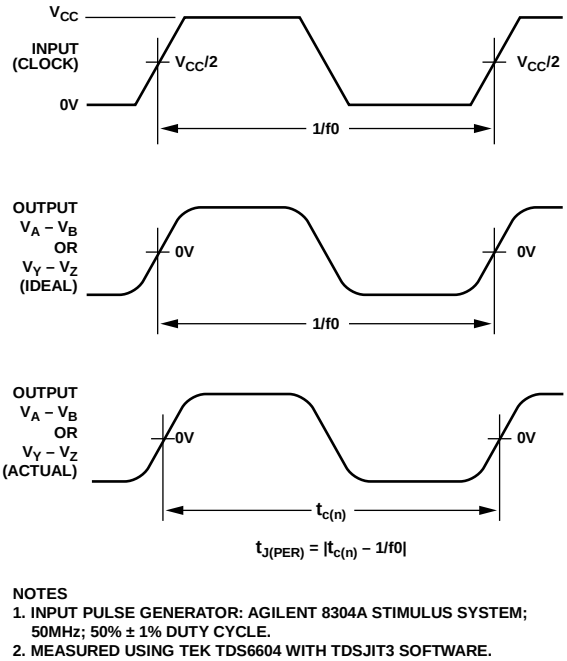
*Figure 23. Driver Timing Measurement*




NOTES
1. C1, C2, C3, AND C4 ARE 20% AND INCLUDE PROBE/STRAY CAPACITANCE < 2cm FROM DUT.
2. R1 AND R2 ARE 1%, METAL FILM, SURFACE MOUNT, <2cm FROM DUT.

10471-023

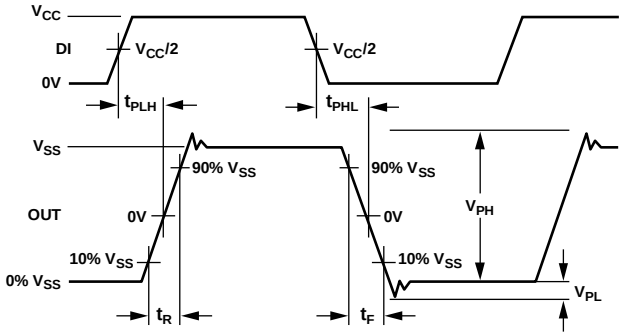
*Figure 24. Driver Enable/Disable Time Test Circuit*




NOTES
1. INPUT PULSE GENERATOR: AGILENT 8304A STIMULUS SYSTEM; 50MHz; 50% ± 1% DUTY CYCLE.
2. MEASURED USING TEK TDS6604 WITH TDSJIT3 SOFTWARE.

10471-024

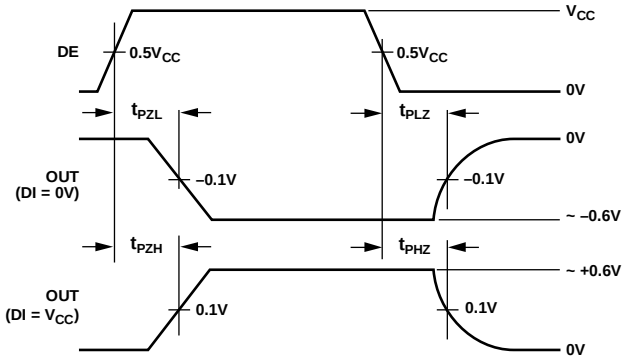
*Figure 25. Driver Period Jitter Characteristics*




NOTES
1. INPUT PULSE GENERATOR: 1MHz; 50% ± 5% DUTY CYCLE; $t_R$, $t_F$ ≤ 1ns.
2. MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 1GHz.

10471-025

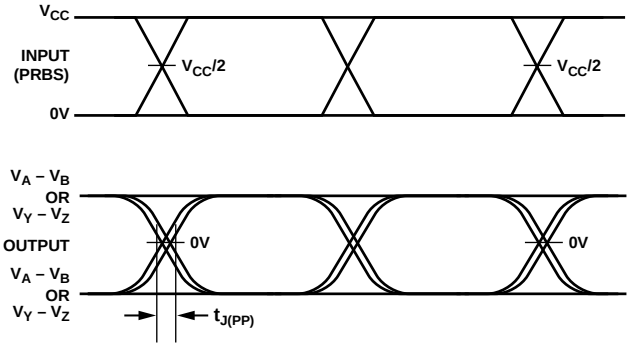
*Figure 26. Driver Propagation, Rise/Fall Times and Voltage Overshoot*




NOTES
1. INPUT PULSE GENERATOR: 1MHz; 50% ± 5% DUTY CYCLE; $t_R$, $t_F$ ≤ 1ns.
2. MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 1GHz.

10471-026

*Figure 27. Driver Enable/Disable Times*

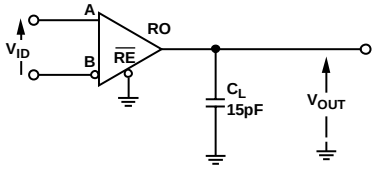



NOTES
1. INPUT PULSE GENERATOR: AGILENT 8304A STIMULUS SYSTEM; 100Mbps; $2^{15}$ – 1PRBS.
2. MEASURED USING TEK TDS6604 WITH TDSJIT3 SOFTWARE.

10471-027

*Figure 28. Driver Peak-to-Peak Jitter Characteristics*

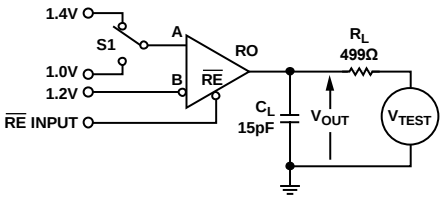
## RECEIVER TIMING MEASUREMENTS




NOTES
1. $C_L$ IS 20%, CERAMIC, SURFACE MOUNT, AND INCLUDES PROBE/STRAY CAPACITANCE < 2cm FROM DUT.

10471-028

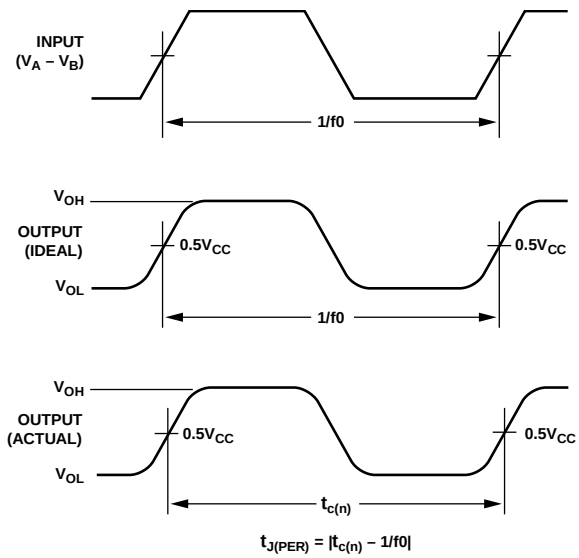
*Figure 29. Receiver Timing Measurement*




NOTES
1. $C_L$ IS 20% AND INCLUDES PROBE/STRAY CAPACITANCE < 2cm FROM DUT.
2. $R_L$ IS 1% METAL FILM, SURFACE MOUNT, <2cm FROM DUT.

10471-029

*Figure 30. Receiver Enable/Disable Time*

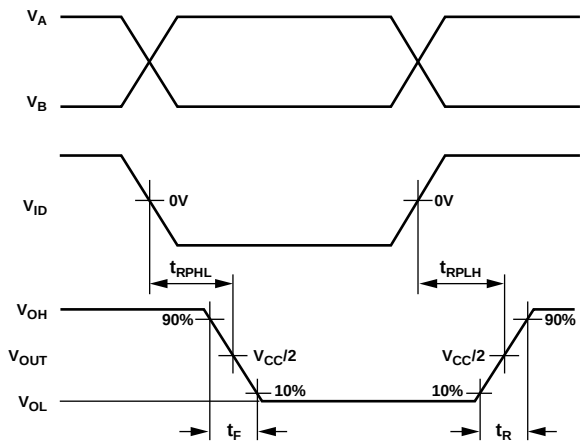



$t_{J(PER)} = |t_{C(n)} - 1/f0|$

NOTES
1. INPUT PULSE GENERATOR: AGILENT 8304A STIMULUS SYSTEM; 50MHz; 50% ± 1% DUTY CYCLE.
2. MEASURED USING TEK TDS6604 WITH TDSJIT3 SOFTWARE.

10471-030

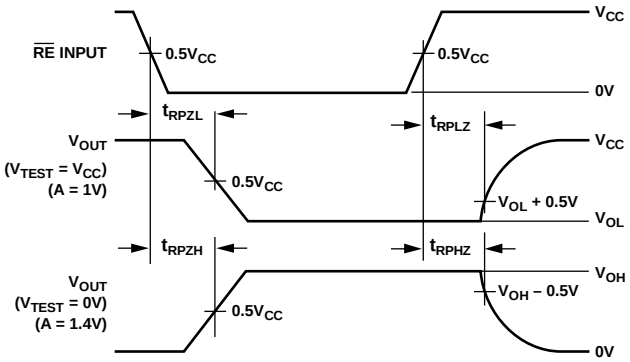
*Figure 31. Receiver Period Jitter Characteristics*




NOTES
1. INPUT PULSE GENERATOR: 1MHz; 50% ± 5% DUTY CYCLE; $t_R$, $t_F$ ≤ 1ns.
2. MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 1GHz.

10471-031

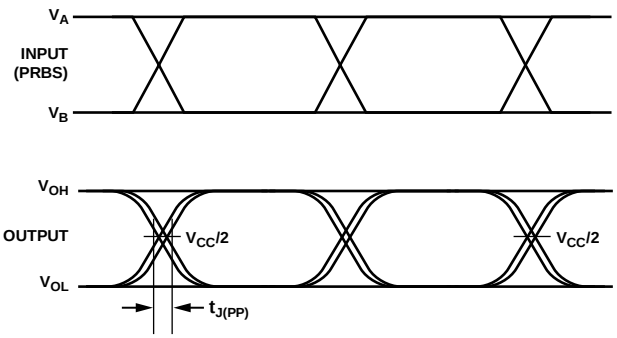
*Figure 32. Receiver Propagation and Rise/Fall Times*




NOTES
1. INPUT PULSE GENERATOR: 1MHz; 50 ± 5% DUTY CYCLE; $t_R$, $t_F$ ≤ 1ns.

10471-032

*Figure 33. Receiver Enable/Disable Times*




NOTES
1. INPUT PULSE GENERATOR: AGILENT 8304A STIMULUS SYSTEM; 100Mbps; $2^{15}$ – 1PRBS.
2. MEASURED USING TEK TDS6604 WITH TDSJIT3 SOFTWARE.

10471-033

*Figure 34. Receiver Peak-to-Peak Jitter Characteristics*

# THEORY OF OPERATION

The ADN4690E/ADN4692E/ADN4694E/ADN4695E are transceivers for transmitting and receiving multipoint, low voltage differential signaling (M-LVDS) at high speed (data rates up to 100 Mbps). Each device has a differential line driver and a differential line receiver, allowing each device to send and receive data.

Multipoint LVDS expands on the established LVDS low voltage differential signaling method by allowing bidirectional communication between more than two nodes. Up to 32 nodes can be connected on an M-LVDS bus.

## HALF-DUPLEX/FULL-DUPLEX OPERATION

Half-duplex operation allows a transceiver to transmit or receive, but not both at the same time. However, with full-duplex operation, a transceiver can transmit and receive simultaneously. The ADN4690E/ADN4694E are half-duplex devices in which the driver and the receiver share differential bus terminals. The ADN4692E/ADN4695E are full-duplex devices that have dedicated driver output and receiver input pins. Figure 36 and Figure 37 show typical half- and full-duplex bus topologies, respectively, for M-LVDS.

## THREE-STATE BUS CONNECTION

The outputs of the device can be placed in a high impedance state by disabling the driver or receiver. This allows several driver outputs to be connected to a single M-LVDS bus. Note that, on each bus line, only one driver can be enabled at a time, but many receivers can be enabled at the same time.

The driver can be enabled or disabled using the driver enable pin (DE). DE enables the driver outputs when taken high; when taken low, DE puts the driver outputs into a high impedance state. Similarly, an active low receiver enable pin ($\overline{RE}$) controls the receiver. Taking this pin low enables the receiver, whereas taking it high puts the receiver outputs into a high impedance state.

Truth tables for driver and receiver output states under various conditions are shown in Table 10, Table 11, Table 12, and Table 13.

## TRUTH TABLES

**Table 9. Truth Table Abbreviations**

| Abbreviation | Description |
|---|---|
| H | High level |
| L | Low level |
| X | Don't care |
| I | Indeterminate |
| Z | High impedance (off) |
| NC | Disconnected |

### *Driver, Half Duplex (ADN4690E/ADN4694E)*

**Table 10. Transmitting (see Table 9 for Abbreviations)**

| | Inputs | | Outputs | |
|---|---|---|---|---|
| Power | DE | DI | A | B |
| Yes | H | H | H | L |
| Yes | H | L | L | H |
| Yes | H | NC | L | H |
| Yes | L | X | Z | Z |
| Yes | NC | X | Z | Z |
| ≤1.5 V | X | X | Z | Z |

### *Driver, Full Duplex (ADN4692E/ADN4695E)*

**Table 11. Transmitting (see Table 9 for Abbreviations)**

| | Inputs | | Outputs | |
|---|---|---|---|---|
| Power | DE | DI | Y | Z |
| Yes | H | H | H | L |
| Yes | H | L | L | H |
| Yes | H | NC | L | H |
| Yes | L | X | Z | Z |
| Yes | NC | X | Z | Z |
| ≤1.5 V | X | X | Z | Z |

### *Type 1 Receiver (ADN4690E/ADN4692E)*

**Table 12. Receiving (see Table 9 for Abbreviations)**

| | Inputs | | Output |
|---|---|---|---|
| Power | A – B | $\overline{RE}$ | RO |
| Yes | ≥50 mV | L | H |
| Yes | ≤−50 mV | L | L |
| Yes | −50 mV < A – B < 50 mV | L | I |
| Yes | NC | L | I |
| Yes | X | H | Z |
| Yes | X | NC | Z |
| No | X | X | Z |

### *Type 2 Receiver (ADN4694E/ADN4695E)*

**Table 13. Receiving (see Table 9 for Abbreviations)**

| | Inputs | | Output |
|---|---|---|---|
| Power | A – B | $\overline{RE}$ | RO |
| Yes | ≥150 mV | L | H |
| Yes | ≤50 mV | L | L |
| Yes | 50 mV < A – B < 150 mV | L | I |
| Yes | NC | L | L |
| Yes | X | H | Z |
| Yes | X | NC | Z |
| No | X | X | Z |

## GLITCH-FREE POWER-UP/POWER-DOWN

To minimize disruption to the bus when adding nodes, the M-LVDS outputs of the device are kept glitch-free when the device is powering up or down. This feature allows insertion of devices onto a live M-LVDS bus because the bus outputs are not switched on before the device is fully powered. In addition, all outputs are placed in a high impedance state when the device is powered off.

## FAULT CONDITIONS

The ADN4690E/ADN4692E/ADN4694E/ADN4695E contain short-circuit current protection that protects the part under fault conditions in the case of short circuits on the bus. This protection limits the current in a fault condition to 24 mA at the transmitter outputs for short-circuit faults between −1 V and +3.4 V. Any network fault must be cleared to avoid data transmission errors and to ensure reliable operation of the data network and any devices that are connected to the network.

## RECEIVER INPUT THRESHOLDS/FAIL-SAFE

Two receiver types are available, both of which incorporate protection against short circuits.

The Type 1 receivers of the ADN4690E/ADN4692E incorporate 25 mV of hysteresis. This ensures that slow-changing signals or a loss of input does not result in oscillation of the receiver output. Type 1 receiver thresholds are ±50 mV; therefore, the state of the receiver output is indeterminate if the differential between A and B is about 0 V. This state occurs if the bus is idle (approximately 0 V on both A and B), with no drivers enabled on the attached nodes.

Type 2 receivers (ADN4694E/ADN4695E) have an open circuit and bus-idle fail-safe. The input threshold is offset by 100 mV so that a logic low is present on the receiver output when the bus is idle or when the receiver inputs are open.

The different receiver thresholds for the two receiver types are illustrated in Figure 35. See Table 12 and Table 13 for receiver output states under various conditions.

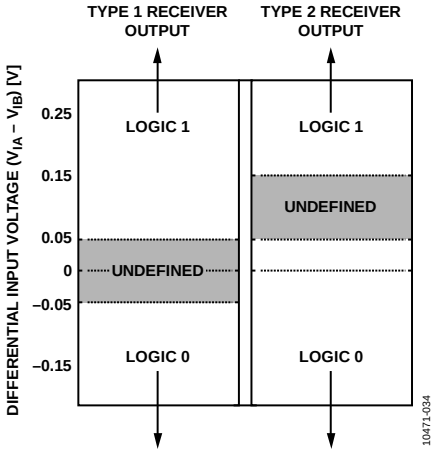



*Figure 35. Input Threshold Voltages*

# APPLICATIONS INFORMATION

M-LVDS extends the low power, high speed, differential signaling of LVDS (low voltage differential signaling) to multipoint systems where multiple nodes are connected over short distances in a bus topology network.

With M-LVDS, a transmitting node drives a differential signal across a transmission medium such as a twisted pair cable. The transmitted differential signal allows other receiving nodes that are connected along the bus to detect a differential voltage that can then be converted back into a single-ended logic signal by the receiver.

The communication line is typically terminated at both ends by resistors ($R_T$), the value of which is chosen to match the characteristic impedance of the medium (typically 100 Ω).

For half-duplex multipoint applications such as the one shown in Figure 36, only one driver can be enabled at any time. Full-duplex nodes allow a master slave topology, as shown in Figure 37. In this configuration, a master node can concurrently send and receive data to/from slave nodes. At any time, only one slave node can have its driver enabled to concurrently transmit data back to the master node.

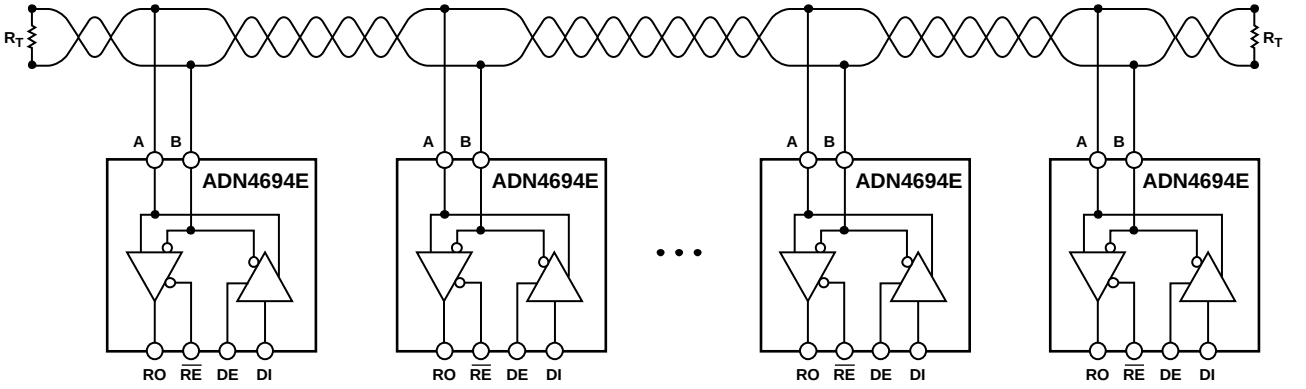



*Figure 36. ADN4694E Typical Half-Duplex M-LVDS Network (Type 2 Receivers with Threshold Offset for Bus-Idle Fail-Safe)*

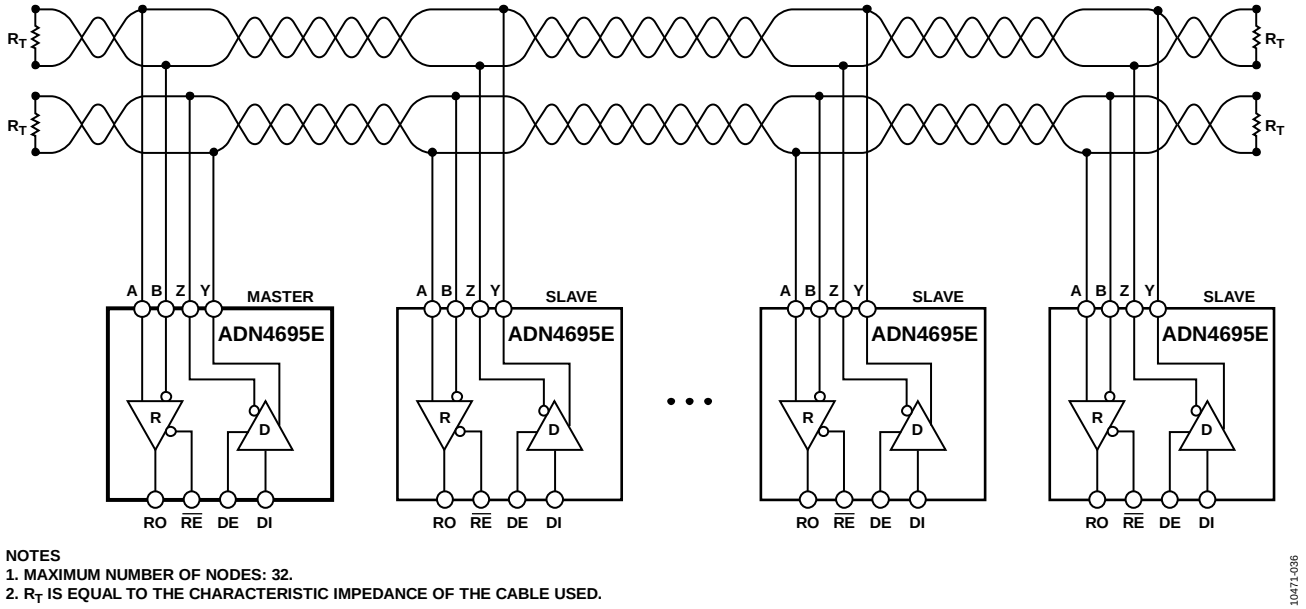
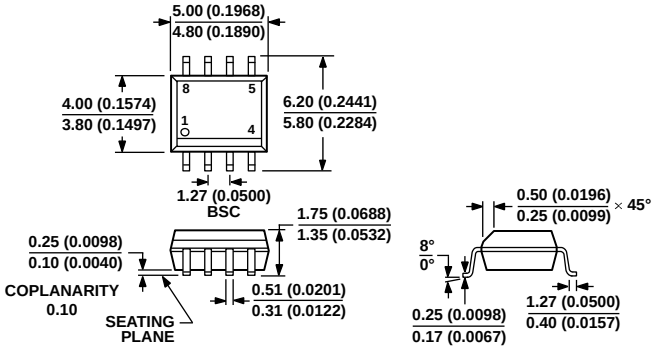



*Figure 37. ADN4695E Typical Full-Duplex M-LVDS Master-Slave Network (Type 2 Receivers with Threshold Offset for Bus-Idle Fail-Safe)*

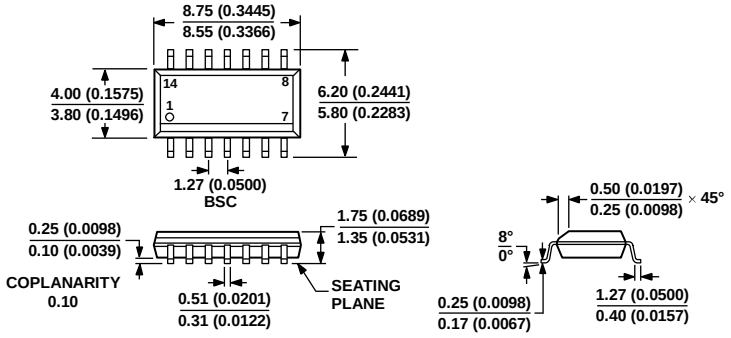
# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

*Figure 38. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*




COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

*Figure 39. 14-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-14)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADN4690EBRZ | –40°C to +85°C | 8-Lead Standard Small Outline Package (SOIC_N) | R-8 |
| ADN4690EBRZ-RL7 | –40°C to +85°C | 8-Lead Standard Small Outline Package (SOIC_N) | R-8 |
| ADN4692EBRZ | –40°C to +85°C | 14-Lead Standard Small Outline Package (SOIC_N) | R-14 |
| ADN4692EBRZ-RL7 | –40°C to +85°C | 14-Lead Standard Small Outline Package (SOIC_N) | R-14 |
| ADN4694EBRZ | –40°C to +85°C | 8-Lead Standard Small Outline Package (SOIC_N) | R-8 |
| ADN4694EBRZ-RL7 | –40°C to +85°C | 8-Lead Standard Small Outline Package (SOIC_N) | R-8 |
| ADN4695EBRZ | –40°C to +85°C | 14-Lead Standard Small Outline Package (SOIC_N) | R-14 |
| ADN4695EBRZ-RL7 | –40°C to +85°C | 14-Lead Standard Small Outline Package (SOIC_N) | R-14 |
| EVAL-ADN469xEHDEBZ | | Evaluation Board for Half-Duplex M-LVDS (ADN4690E, ADN4694E) | |
| EVAL-ADN469xEFDEBZ | | Evaluation Board for Full-Duplex M-LVDS (ADN4692E, ADN4695E) | |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES

## NOTES


D10471-0-3/12(A)