

KS54AHCT 125/126
KS74AHCT

Quad 3-State Buffers T-52-07

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

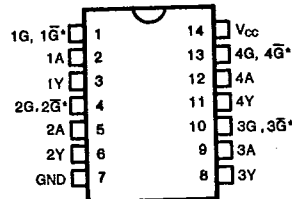
DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

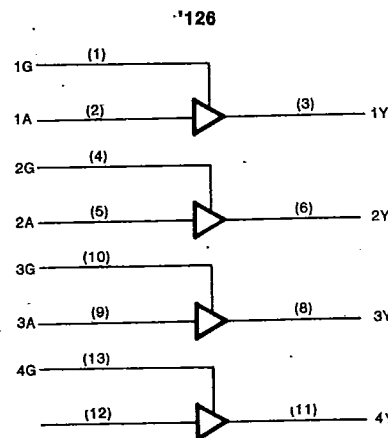
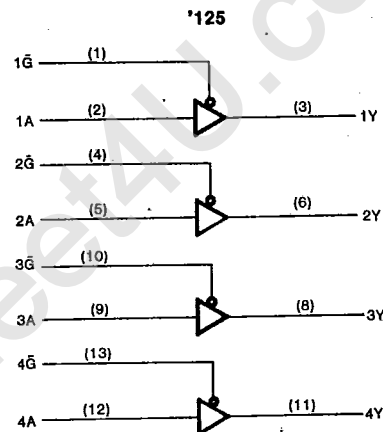
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



* \bar{G} for '125; G for '126

LOGIC DIAGRAMS



FUNCTION TABLES

'125

Inputs		Output
A	\bar{G}	Y
H	L	H
L	L	L
X	H	Z

'126

Inputs		Output
A	G	Y
H	H	H
L	H	L
X	L	Z

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KS74AHCT

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} ... -65°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}
 Operating Temperature
 Range KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
 Input Rise & Fall Times, t_r , t_f Max 500 ns
 * Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable = V_{IH} $V_{OUT}=V_{CC}$ or GND		± 0.5	± 5.0	± 10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT125, AHCT126

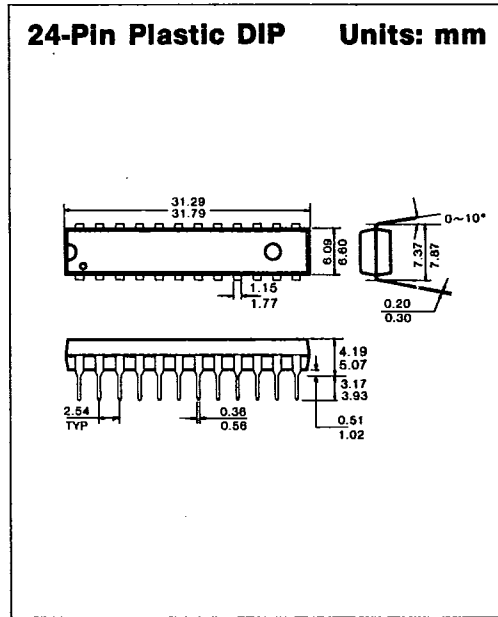
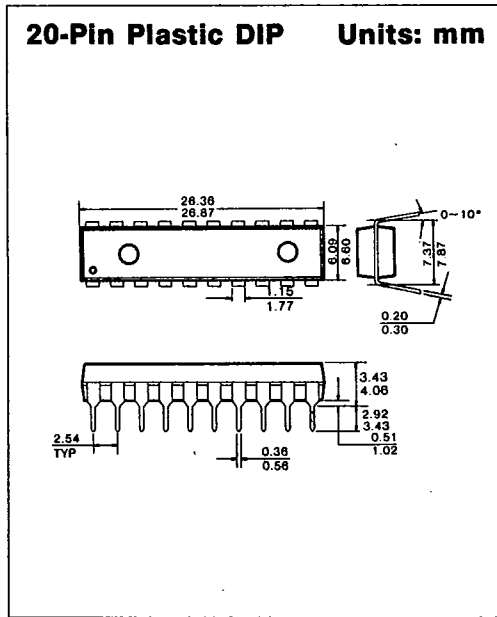
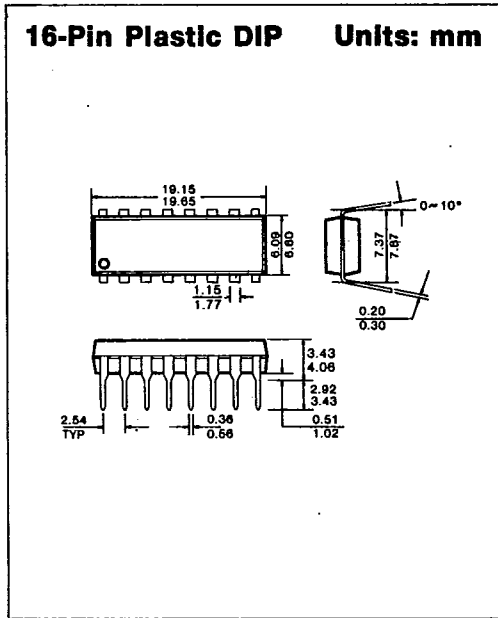
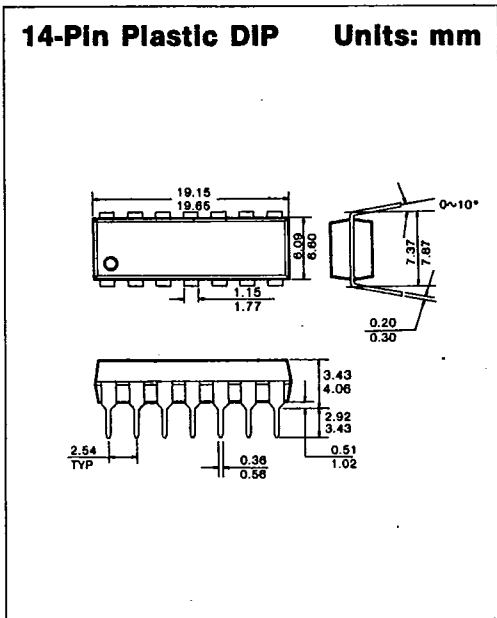
Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay, A to Y	t _{PLH}	C _L = 50pF	6		10		12	ns
		C _L = 150pF	9		15		18	
	t _{PHL}	C _L = 50pF	6		10		12	
		C _L = 150pF	9		15		18	
Output Enable Time Enable to Y	t _{PZH}	C _L = 50pF	11		18		22	ns
		C _L = 150pF	14		23		28	
	t _{PZL}	C _L = 50pF	11		18		22	
		C _L = 150pF	14		23		28	
Output Disable-Time, Enable to Y	t _{PHZ}	R _L = 1kΩ	13		18		22	ns
	t _{PLZ}	C _L = 50pF	13		18		22	
Input Capacitance	C _{IN}		5					pF
Output Capacitance	C _{OUT}	Output disabled	10					pF
Power Dissipation Capacitance* (per stage)	C _{PD}	G or $\bar{G} = V_{CC}$	5					pF
		G or $\bar{G} = \text{GND}$	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
 † For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES



7



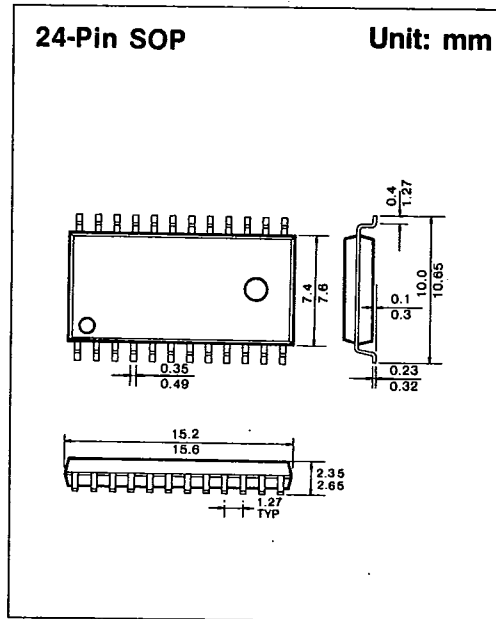
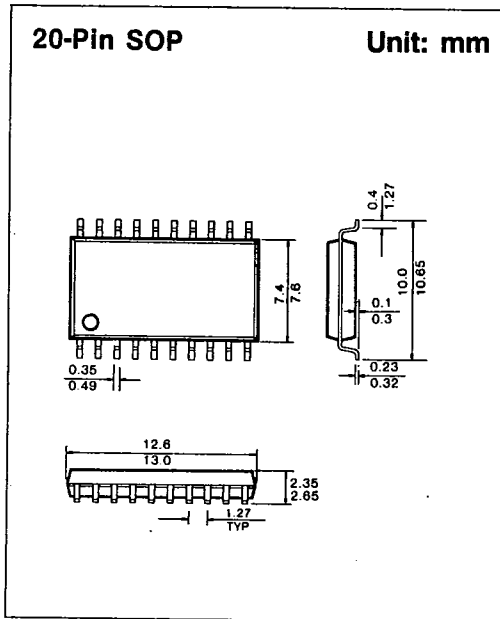
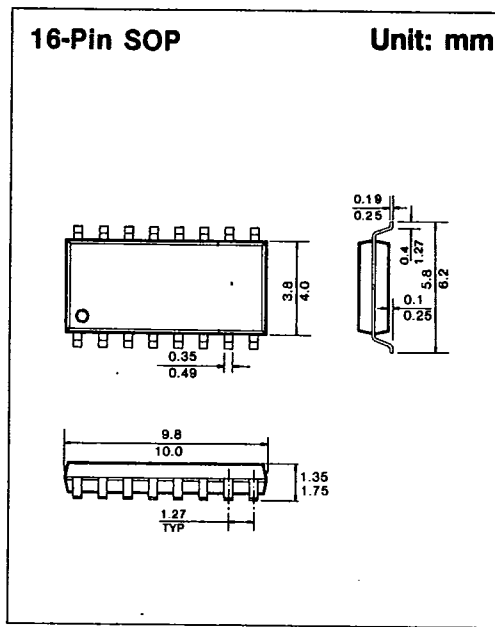
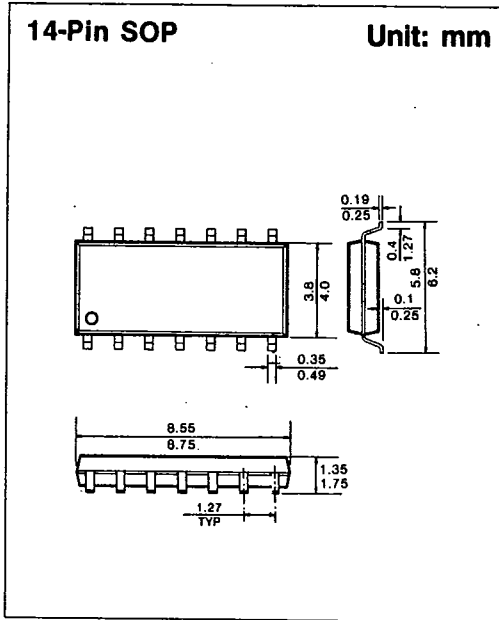
SAMSUNG SEMICONDUCTOR

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PACKAGE DIMENSIONS

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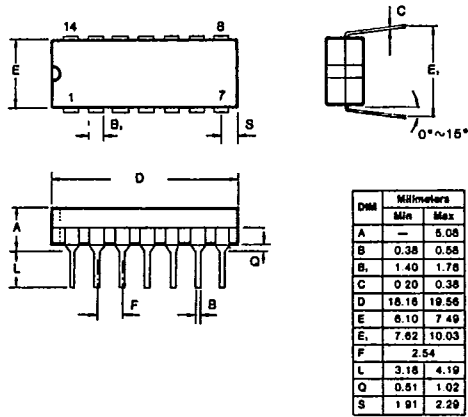


PACKAGE DIMENSIONS

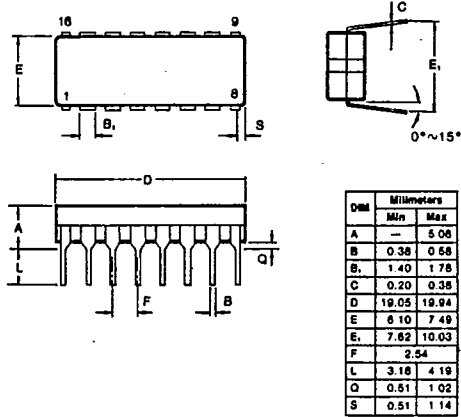
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2. CERAMIC PACKAGES

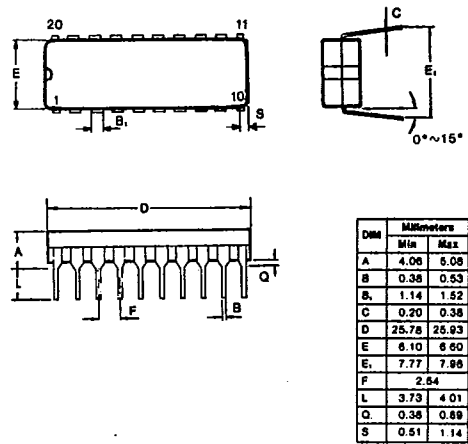
14-Pin Ceramic DIP Units: mm



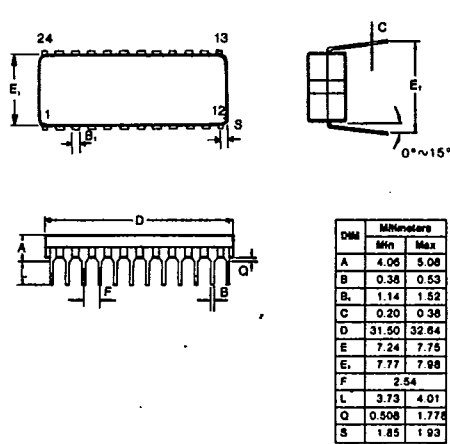
16-Pin Ceramic DIP Units: mm



20-Pin Ceramic DIP Units: mm



24-Pin Ceramic DIP Units: mm



7